Feasibility of Successive Approximation Register ADC in Ultra Low Power Biomedical Applications

Suhaib Ahmed [#1], Saima Bashir [*2], Bisma Bilal [#3], Vipan Kakkar [#4]

[#] Department of Electronics and Communication Engineering,
Shri Mata Vaishno Devi University, Katra, India
[1] sabatt@outlook.com
[3] bismabilal21@gmail.com
[4] vipan.kakar@smvdu.ac.in

[*] Department of Electronics and Communication Engineering,
National Institute of Technology, Srinagar, India
[2] amiasbashir@gmail.com

***Abstract*—Analog-to-Digital Converter (ADC) is a critical block of the sensing unit of an implant and for measurements of various biophysiological signals, such as Electrocardiogram (ECG), Electroencephalogram (EEG) and Electromyogram (EMG) that covers the distinct portions of the frequency spectrum and signal bandwidths. ADC consumes about 30~35% of the total power of the device which is very high. Hence, for biomedical implants which require ultra low power consumption and low complexity to reduce the size and cost of the devices, there is a need of energy-efficient ADCs that conform to these restraints. This paper presents a study on the feasibility of ultra low power Successive Approximation Register (SAR) ADC in these biomedical applications. Various SAR ADC architectures proposed in the past decade to achieve ultra low power consumption have been investigated and their performances have been compared with respect to the parameters such as resolution, sampling frequency, signal–to-noise and distortion ratio, figure of merit among others. This paper also discusses the different switching schemes proposed to reduce the switching power consumed by the DAC. Finally, the future research scope and areas to further achieve ultra low power consumption without degrading the overall performance of the ADC has also been presented.**

Keyword-ADC, Biomedical Applications, SAR, Ultra Low Power Electronics

I. INTRODUCTION

There is a rapid positive growth in the industry of medical device especially in wearable and implantable biomedical systems. Hence, it has become a hub for the research activity in the past few years. Due to its vastness, the study of its related areas like pharmaceutics, bioengineering, electronics, biophysics etc. possesses a potential to find better and patient-friendly solutions to medical problems at minimal costs and has enabled progressive research in cardiac and neural disorders, chronic problems and cancer detection to list a few. To add on it has become possible to positively affect the cellular processes at sub-micron scales initiated upon implantation, due to the advancements in the field of micro and nanotechnology [1].

This intensive integration of system-on-chip and the growth of portable applications market drives the research of solutions alternative to standard circuit design that can be capable to further reduce the power consumption of the entire electronic system. Next to general low power circuits, there is an emerging product application area characterized by even stronger power requirements, the so-called Ultra Low Power Electronics [2].

Figure 1 shows a generalized block diagram of an acquisition system of EEG, ECG, EMG and other bioelectric signals. It consists of an analog front end (AFE) which senses these bioelectric signals by using electrodes or microelectrode arrays. The sensed signal is first pre-amplified and filtered to remove the noise, if any. The analog-to-digital converter (ADC) then digitizes the signal which is then processed by the digital signal processor at the back end. In some applications, a transmitting antenna is used for wireless transmission of sensed data from implants to a monitoring system or a base-station.

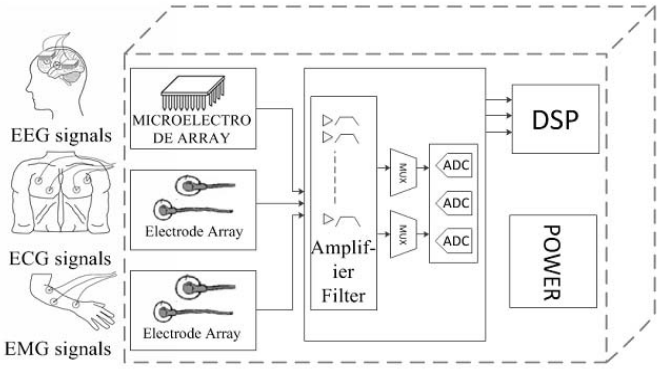

Fig. 1. General block diagram of a bioelectric signal acquisition system [3]

It is observed from Table 1 that different neural signals are usually spread over a narrow range of amplitudes and frequencies ranging from few Hz to 200Hz and μV to mV except for spike signal which can have the maximum frequency of 7 kHz, whereas ECG is a very weak signal with an amplitude range of 1–5 mV at very low frequencies of 0.05–100 Hz [4, 5]. Since these signals are low level hence they require low noise operation which makes it a difficult task to design a biomedical sensor interfaces for these biophysiological signals.

TABLE I Amplitude and frequency ranges of various electrical signals from the brain [4]

Biosignal Type	Description	Attributes of Signal
Spike	Recording of signals generated from individual neurons by extracellular microelectrode inside cortex	500 μV 0.1 - 7 kHz
LFP	Recording of signals generated from multiple nearby neurons by extracellular microelectrode inside cortex	< 1 mV < 200 Hz
ECoG	Cerebral cortex activity monitoring and recording using disk electrodes placed on the exposed surface of the brain	0.01 – 5 mV < 200 Hz
EEG	Recording of non-inactive electric activity from the brain	5 – 300 μV < 100 Hz

Hence to capture these signals accurately the acquisition system has to incorporate a low noise amplifier with desirable gain as shown in figure 1 along with a band-pass filter to lower the d.c. offset and noise of input signal and an ADC with resolution greater than or equal to 8 bits along with minimizing the power consumption to prolong the battery lifetime.

An ADC circuit that can acquire and isolate these neural and cardiac signals while maintaining ultra low power and low noise performance over all the ranges of operations offers obvious advantage over the one that is tailored to for a specific signal. It is desired to maintain low noise and ultra low power performance over all the ranges of operations. Various topologies of ADCs such as Sigma-Delta, Pipelined, Cyclic, etc. have been investigated over the years for Ultra Low Power operation in biomedical applications. However, one topology that has stood out of them for ULP applications is Successive Approximation Register (SAR) ADC due to its small active area and minimal requirement for active analog circuits. It is observed from fig. 2 that SAR topology delivers high performance on lower end applications such as biomedical, sensors etc. which operate at lower sampling rates from few kHz to few GHz. The reason behind its popularity in low speed applications are its ability to operate completely in dynamic manner which leads to almost zero static power consumption and the fact that CMOS technology is able to provide the switching speed required for sequential conversion of the analog signal.

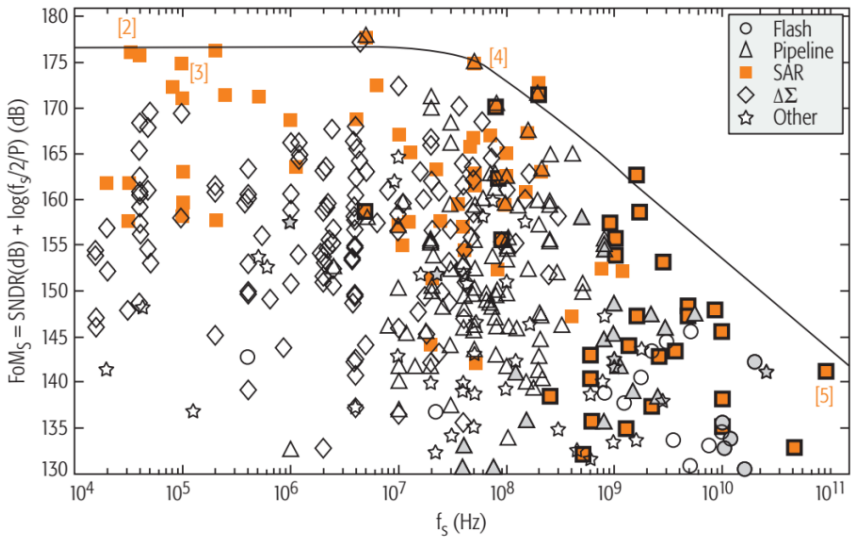

Fig. 2. Plot of ADC power efficiency vs. sampling frequency (fs) of some recently reported ADCs [6].

II. SUCCESSIVE APPROXIMATION +REGISTER ADC

The function of sampling and holding an externally input analog signal is done by a Sample and Hold Amplifier (SHA) in a Successive Approximation Register (SAR) Analog-to-Digital Converter. This is shown in figure 3. Along with the SAR logic circuit, a comparator is also used for comparing a level of an analog signal corresponding to 'N' bits and generating a comparison signal according to the result as shown in figure 4. This is used for generation of digital signal from sequentially generating a digital signal from a Most Significant Bit (MSB) to a Least Significant Bit (LSB) in response to the comparison signal and a Digital-to-Analog Converter (DAC) for providing the analog signal to the comparator, and an output/code register for holding the sequentially generated digital signal from the MSB to the LSB to generate an N-bit digital signal, wherein, upon externally receiving a START signal, the SAR logic circuit generates a digital signal of a MSB having a 1-bit phase delay compared to the START signal [7] [8].

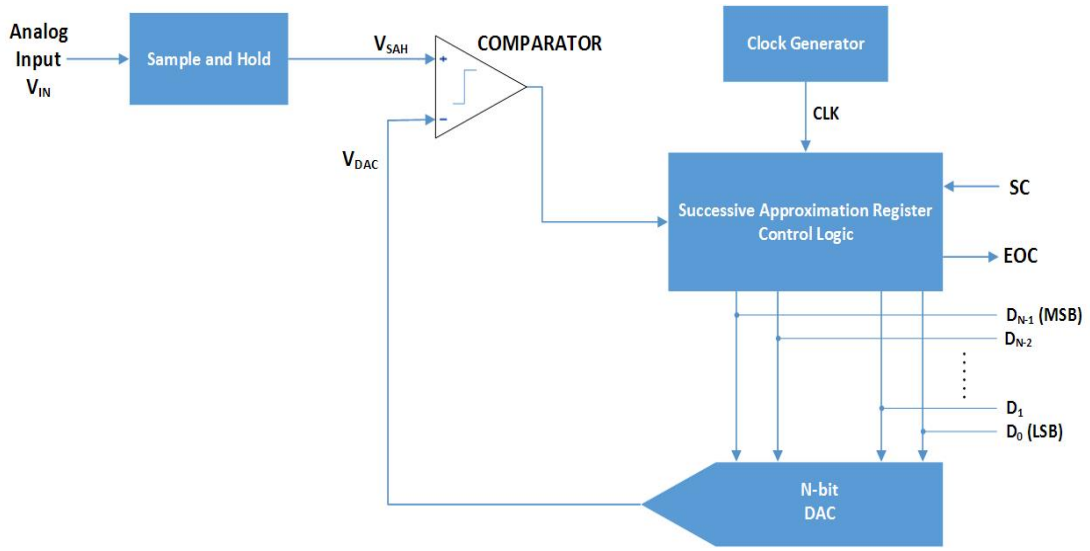

Fig. 3. General architecture of SAR ADC

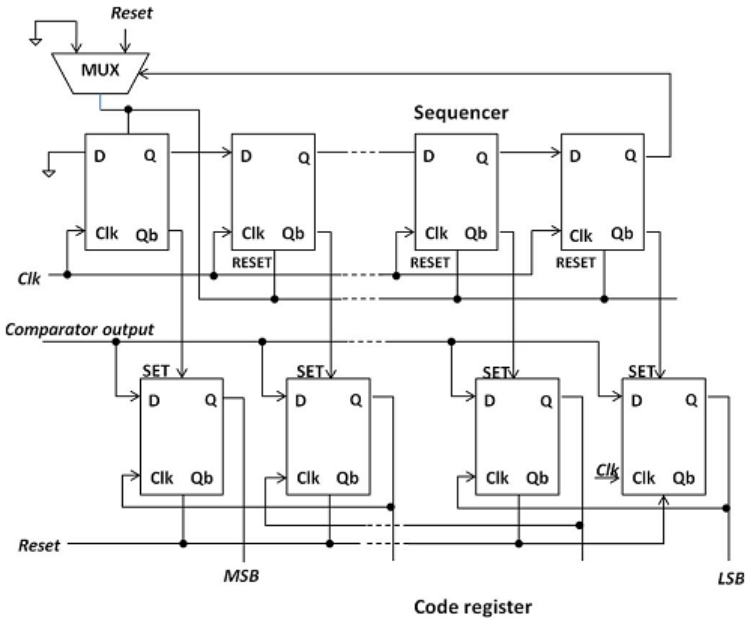

Fig. 4. SAR logic block diagram

III. ULTRA LOW POWER SAR ADC

This section presents a state-of-the-art survey of the Ultra Low Power SAR ADC designs and techniques investigated in the past decade in chronological order, for application in biomedical applications including Pacemaker and Deep Brain Stimulation (DBS).

A single-chip highly integrated low power mixed-signal IC has been proposed for Implantable Pacemaker Application in [9], to sense the heart rate and deliver electrical stimulation, instead of using several analog ICs. The primary goal is focused around low-power analog and digital design techniques to prolong single battery operations. An 8-bit SAR-ADC has been used in the sensing system of the proposed IC to digitize the input ECG signal. In this ADC, power is mainly consumed by Sample and Hold Amplifier (SHA), DAC and comparator. To minimize this power, binary weighted capacitor array for DAC has been utilized along with integrated single op-amp which consists of three class-AB amplifiers or inverters that have been used for both S/H and comparator. At a supply voltage of 2V the current consumption of the ADC is around 150 nA and the power dissipated by the entire system is 8 μW when fabricated in a 0.5 μm two-poly three-metal multi-Vt process.

Binary search algorithm architecture has been proposed in a traditional SAR ADC to replace its conventional DAC to significantly reduce the system area and power consumption for biomedical instruments in [10]. It has variable resolution and eliminates the need for resistors and a high current reference source. A digital flip-flop is employed as storage device for the output of the comparator and the amount of digital logic involved is minimal which results in the elimination of cross-talk between analog and digital components and reduces the complexity of the layout process. With a conventional battery supply of 2V, the power consumed by the proposed ADC is 22.2 μW with a very high resolution of 16 bits, which is almost 52% lower than conventional SAR ADC power consumption. Hence it is a possible solution in applications where size and low power operations are necessary such as in portable biomedical devices.

The proposed design in [11] is a biomedical signal acquisition IC which consists of low noise instrumentation amplifier with DC rejection, an 11 bit SAR ADC, other auxiliary circuits and still consumes only 2.3 microwatt of power at supply voltage of 1V. The ADC proposed for the IC does not have a dedicated S/H in order to conserve power. It however consists of the output stage of low noise OTA as a pseudo S/H circuit and it also uses a dynamic comparator with negligible power consumption when inactive.

One of the techniques used to save power is to reduce the consumption at charging and discharging of capacitor array. Using the binary search based operation, the SAR architecture has been modified in terms of power in [12]. A switching technique has been proposed for saving energy in this paper, which is combined with capacitor splitting technique and splits MSB/2 capacitor into the binary weighted sub capacitor array. This technique lowers the power consumption during the up paths of each switching phase. At the supply voltage of around 1V, the power dissipation using this technique has been reduced to 7.75 μW, i.e. around 56% saving in energy in comparison to conventional ADCs. Whereas the switching energy required in the conventional ADCs increase with the length of output code, using this technique however the switching energy remains constant.

An SAR ADC which employs splitting comparator and energy saving capacitor array, suitable for wireless sensor networks and biomedical applications at low power consumption has been proposed in [13]. The coarse and fine comparison in the splitting comparator is done by two comparison paths consisting of detector and two topology comparators. This is shown in Figure 5. This comparator acts like a hysteresis comparator to select the adjustable window size path. A fully dynamic regenerative latch is used in the coarse comparator architecture whereas fine comparator is an output offset storage comparator. Using this proposed architecture 42 µW of power is dissipated at the supply voltage of 1V.

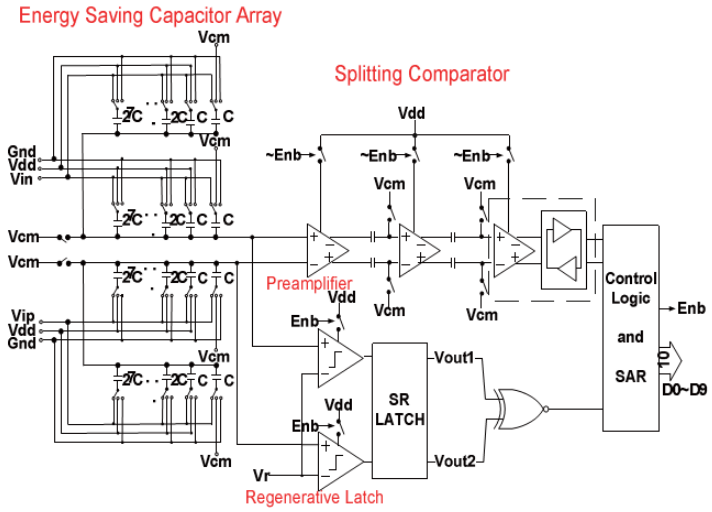

Fig. 5. Energy saving capacitor array SAR ADC architecture [13]

A system on chip has been proposed for the feature detection and to detect the onset of seizures of EEG channel and hence convert these analog EEG signals to digital domain in [14]. For feature vector streaming, the Instrumentation Amplifier (I-amp), which amplifies the 10-50 µV EEG Signal from the passive scalp electrodes, an ADC, a processor for feature extraction and a low power parallel-serial interface, has been integrated into a single central device. It further employs a control gate to ensure that static bias remains ON for the period of conversion. A 12 bit ADC used in this architecture uses a 6-bit main ADC and a 6-bit sub ADC Architecture and works at the sampling rate of 100 kS/s to achieve the power consumption of 25 µW at 1V supply.

Addressing the low power consumption requirement in the growing area of portable bio-potential acquisition systems, an ultra low power, low noise and small chip area SAR ADC has been proposed in [15]. Compared to the conventional SAR, the proposed SAR has additional auto-zeroed preamplifier to suppress offset voltage, is placed before the latch which is offset calibrated by adding unbalanced capacitors to conserve power. Also to address the problem of low kick-back noise, a low kick-back noise latch is proposed in this paper which has four additional transistors compared to the conventional latch and hence there are very less glitches in the output. The chip was fabricated in 0.18 µm CMOS process and the power consumed by this design is only 455 nW for a supply voltage of 1.8V and a resolution of 12 bits. Although this ADC was designed for bio-potential acquisition system, it can also be used in other high resolution and low speed applications with a very low power consumption requirement.

The authors in [5] have proposed system architecture of current mode ADC with an aim to achieve ultra low power consumption and small die area for pacemakers which detects the IECG signals. Current mode SAR ADC has been has been used because it does not use operational amplifiers and its power consumption is directly proportional to the full scale current input, as shown in figure 6. To achieve small area, unary-weighted current source array has been used as DAC instead of using capacitors. The 8-bit design is simulated using IBM 0.13 µm CMOS technology parameters and the temperature is set to 37 ˚C as that of human body and. The total power consumed by the proposed 8-bit current mode SAR ADC is 255 nW, designed using 0.13 µm CMOS technology and a supply voltage of 1V and simulated at 37 ˚C. For IECG applications this power consumption is almost 50% of the lowest reported ADC for similar design specifications.

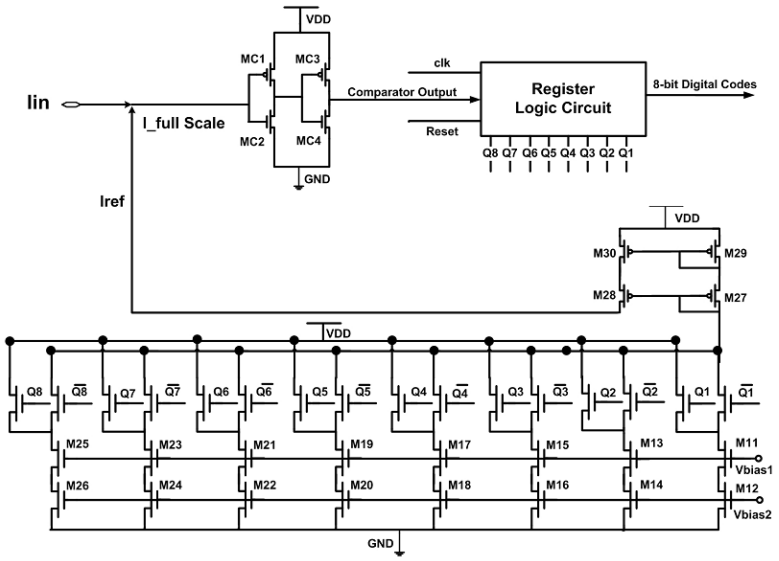

Fig. 6. Current mode unary weighted SAR ADC [4]

[16] proposes a leakage reduced CMOS switch for 10 bit SAR ADC working at a sampling rate of 1 kS/s taking into account its various design constraints. The emphasis is on sampling circuit which during the operation of ADC introduces various linear and non-linear effects and hence degrades the accuracy of the ADC. It is observed that high VDD is favorable but it increases power dissipation and decrease of sampling frequency provides large margin for jitter reduction and bandwidth design but it introduces reverse voltage droop. The total power dissipation of this SAR ADC is 64 nW at a supply voltage of 1V of which 34 nW (53%) is consumed by SAR logic and 28 nW (44%) by capacitor array.

A highly integrated analog front-end (AFE) IC design for monitoring brain-heart biosignals such as Diffuse Optical Tomography (DOT), Electrocardiography (ECG) and Electroencephalography (EEG) has been presented in [17]. It features a fully integrated eight-channel design for low power operation in which each channel shares a common ADC which is employed in conjunction with an analog multiplier to select the particular bioelectric signal for digitization. The IC employs a 10-bit SAR ADC as it is advantageous in terms of area and power. To improve the SNR of the ADC, a parallel configuration based comparator has been used which also increases the common mode range whereas, a split capacitor based DAC has been proposed which is deprived of any capacitor scaling and thus achieves lower power consumption. The total power consumed by the IC is 506.36 μW of which only 8.27 μW is consumed by the proposed ADC when operated at a sampling frequency of 100 kS/s and supply voltage of 1.8 V. Hence this IC design achieves the goal of low power operations while maintaining low noise.

In [18], an SAR ADC that utilizes a common mode resetting tri-level switching scheme and a time domain comparator with redundant algorithm is presented for applications like wearable sensor nodes and implantable medical devices powered by batteries or wireless charging, as shown in figure 7. The requirement of low power consumption has been achieved by reducing the static and switching power consumed by the ADC, where the switching activity and power is reduced by the proposed common mode resetting tri-level switching scheme and the time domain comparator has been used due to its low voltage operation ability and zero static power consumption. The SAR ADC consumes only 400 nW power at a 1V supply voltage of which 52% of the power is consumed by the comparator, 23% by SAR logic, 23% by the capacitor array and rest by the clock buffer.

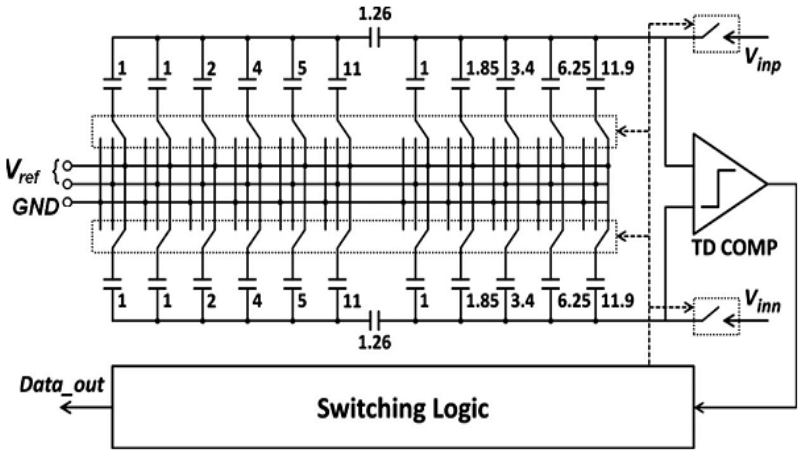

Fig. 7. Tri-level switching based SAR ADC [18] [15]

With the focus to reduce the battery lifetime, a power efficient Successive Approximation technique based ADC has been used to digitize the ECG signals acquired by the wavelet based ECG detector, for monitoring the heart-beat rate and its rhythm in a low power and energy efficient Implantable Pacemaker Integrated Circuit (IPIC) proposed in [19]. This SAR-ADC achieves lower power consumption by using voltage scaling and clock gating technique. Due to low sampling rate of IPIC and relatively faster conversion speed of the ADC, large portion of ADC is inactive most of the time, hence switch-attached ON/OFF time controlled comparator and time interleaved passive S/H with no static current has been implemented which further reduces the static power consumption of the SAR-ADC. The proposed test chip when fabricated at 0.35 μm CMOS technology achieves a low power consumption of 19.02 μW with a supply voltage of 3V of which 5.4 μW (~29%) is consumed by the SAR-ADC.

With the goal to reduce the power consumption and reduce noise to improve the signal-to-noise ratio, this paper presents a new of architecture of SAR ADC in [3]. The accuracy is determined by the DAC which is its core component, hence an energy efficient binary capacitor array has been used in this design and the capacitance is almost halved compared to the conventional DAC. Dynamic latched comparator has been designed along with synchronous SAR logic to save energy and a dynamic amplifier has been inserted between the DAC to reduce the kick-back noise and accelerate the speed. Generally, for EEG acquisition system an ADC with 10-bit resolution is preferred to achieve better accuracy. For a supply voltage of 1.2V the power consumption is 120 nW and 2.96 μW for 1 kS/s and 30 kS/s sampling frequency respectively. For a supply voltage of 1.8 V the power consumption is 270 nW and 6.32 μW for 1 kS/s and 30 kS/s sampling frequency respectively. Hence the proposed 10-bit SAR ADC can be used for biomedical devices which require ultra low power consumption and low speed.

An SAR ADC has been proposed in [20] for biomedical signals which are particularly very low frequency signals in nature. Power efficiency in SAR ADC has been achieved by reducing the total capacitance of DAC and the speed of its operation whereas the S/H uses a capacitor and an analog switch to connect or isolate from the input. To reduce the area, the 10-bit DAC has been sub-divided into two 5-bit DACs and is implanted using split-array capacitive charge redistribution architecture. For a supply voltage of 1.8V, the power dissipated by the proposed ADC is only 1.502 μW with a higher resolution compared to other ADCs for the same design specifications.

An ASIC for single chamber leadless pacemaker at ultra-low power (sub μW) consumption centered at high quality ECG signal acquisition and classification has been proposed to readout and extract the information from the ECG signal using QRS complex extractor in[21]. In order to reduce the consumption of power, feature extraction is performed in analog domain followed by digitization where an ADC converts both time domain ECG signal (ECGout) and feature extracted signal (FEout) before feeding the signals to DSP. This architecture contains a 9-bit capacitor array, which is used as sampling capacitor, as well as feedback DAC. With the supply voltage varying from 1.3-1.8 V, the current consumptions of channels is 350 nA (44%), that of ADC is 110 nA (17%) and other supporting circuits consume 220 nA (32%), thus the total current consumed is 680 nA.

TABLE II Performance Comparison of recently reported SAR ADCs for Biomedical applications

Paper	CMOS Technology Used (µm)	Supply Voltage (V)	Resolution (bits)	Sampling Rate (KS/s)	SFDR (dB)	SNDR (dB)	INL (LSB)	DNL (LSB)	ENOB	Power Consum-ption	FOM (J/conv)
[5]	0.13	1	8	1	-	-	< 0.63	< 0.61	7.6	225 nW	0.657 p
[9]	0.5	0.5	8	1	>48	-	< 1.5	< 1.5	-	300 nW	-
		2.5	12	0.1			< 2.5	< 2			
[10]	0.18	2	16	0.2	-	-	<± .3	<±0.5	-	22 µW	-
[11]	0.35	1	11	1	-	-	< ± 2	< 1.5		2.3 µW	-
[12]	0.18	1	8	500	62.69	46.92	+0.31/ -0.28	+0.17/ -0.24	7.5	7.75 µW	8.6 f
[13]	0.18	1	10	500	75	58.4	±0.76	±0.76	9.4	42 µW	124 f
[14]	0.18	1	12	100	-	65.3	0.68	0.66	10.55	25 µW	250 p
[15]	0.18	1.8	12	2	78.7	61.8	3 / -3	1.5 / -1	10	455 nW	220 f
[16]	0.13	1	10	1	-	59	-	-	9.5	64 nW	-
[17]	0.18	1.8	10	100-200	75.19	53.72	+1.53/ -1.84	+0.53/ -0.75	8.63	8.27 µW	-
[18]	0.18	1	10	80	61.1	53.28	± 1.5	± 0.7	8.6	400 nW	19.5 f
[19]	0.35	3	8	1.024	54.3	45.4	1.5	1	7.5	5.4 µW	-
[20]	0.18	1.8	10	200	-	57.4	-	-	9.24	1.502 µW	160 f
[3]	0.18	1.2	10	1	72.16	60.524	-0.7	+0.4/ -0.299	9.735	270 nW	138.4 f
		1.8		30					9.773	6.32 µW	
[21]	0.18	1.3	7 – 10 (flexible)	0.512	56.2	55.7	0.79	0.6	8.96	130 nW	-
		1.8								180 nW	-
[22]	0.18	0.6	10	20	67.7	58.3	0.44	0.46	9.4	38 nW	2.8 f
[23]	0.18	1	10	41.6	67.5	56.6	1.14	0.69	9.1	306 nW	14.3 f
[24]	0.09	0.4	10	250	78.5	53.7	0.53	0.47	8.63	200 nW	2.02 f
[25]	0.18	1	8	14000	-	42.69	-	-	6.8	67.91 µW	-

IV. DISCUSSIONS

The operation at a very low supply voltage (1-1.5V) with ultra low power consumption for long battery lifetime are some constraints possessed by the wearable medical devices that are desirable to operate under single micro battery. This arises the need of extremely low input referred noise to pick up these very weak signals. The SAR designs are gaining popularity for ultra low power applications due to the aggressive scaling of unit capacitance, scaling of digital logic with low power leakage and the ability of the comparator to operate in subthreshold region. Some of the recently proposed SAR ADCs for different biomedical applications have been studied and surveyed and the feasibility analysis of these ADCs is done with respect to their performance parameters such as resolution, sampling frequency, SNDR, SNFR, power consumption, effective number of bits (ENOB), integral and differential non-linearity along with the figure of merit (FOM) and can be summarized by Table 2. It is observed that power as low as 38 nW has been achieved by authors in [22] for a 10-bit SAR ADC for use in biomedical implants. The performance of these ADCs indicates that for a resolution of 8-12 bits, SAR topology is feasible enough to achieve ultra low power operation while maintaining the other desired performance parameters. As the resolution is increased beyond 12 bits the power consumption of SAR increases drastically and hence requires new design techniques to reduce the power at higher resolution.

V. CONCLUSION

It is concluded that the input range of all the biophysiological signals lie within the range of 0-50 mV with frequency ranging from near DC to 200 Hz except for the neural spike signals which lies in the range of 0.1-7 kHz. In context to the micro-power medical devices, not speed but ultra low power conversion of these low amplitude and frequency biophysiological signals is paramount. This in conjunction with the accuracy required in the conversion accuracy of these biophysiological signals makes the design and development of ADCs with these specifications a major challenge in order to increase the efficiency of the battery. The main focus of

research heretofore has been on medium resolution (8-12 bits), moderate and particularly high speed applications. Technologies such as optimization of the control logic, new structures for DAC, new switching schemes and designing of comparator have been applied to these SAR ADCs but they remain unexplored in biomedical realm in terms of efficient design methodologies and circuit techniques. Another research aspect that is yet to be explored is the performance degradation of the ultra low power ADCs.

REFERENCES

[1] A. Arsiwala, P. Desai, and V. Patravale, "Recent advances in micro/nanoscale biomedical implants," Journal of Controlled Release, vol. 189, pp. 25-45, 2014.
[2] V. Kakkar, "Feasibility of Ultra Low Energy Devices and Applications," Acta Technica Napocensis, vol. 52, p. 1, 2011.
[3] W. Geng, G. Wang, K.-T. Lin, and K.-T. Tang, "A 10-bit 1kS/s-30kS/s successive approximation register analog-to-digital converter for biological signal acquisition," in Biomedical Engineering and Informatics (BMEI), 2013 6th International Conference on, 2013, pp. 403-407.
[4] M. Mollazadeh, K. Murari, G. Cauwenberghs, and N. Thakor, "From spikes to EEG: Integrated multichannel and selective acquisition of neuropotentials," in Engineering in Medicine and Biology Society, 2008. EMBS 2008. 30th Annual International Conference of the IEEE, 2008, pp. 2741-2744.
[5] S. Al-Ahdab, R. Lotfi, and W. A. Serdijn, "A 1-V 225-nW 1KS/s current successive approximation ADC for pacemakers," in Ph. D. Research in Microelectronics and Electronics (PRIME), 2010 Conference on, 2010, pp. 1-4.
[6] B. Murmann, "The successive approximation register ADC: a versatile building block for ultra-low-power to ultra-high-speed applications," IEEE Communications Magazine, vol. 54, pp. 78-83, 2016.
[7] H.-w. Kang, "Successive approximation register analog-to-digital converter and analog-to-digital conversion method using the same," ed: Google Patents, 2014.
[8] S. Bashir, S. Ali, S. Ahmed, and V. Kakkar, "Analog-to-digital converters: A comparative study and performance analysis," in Computing, Communication and Automation (ICCCA), 2016 International Conference on, 2016, pp. 999-1001.
[9] L. S. Wong, S. Hossain, A. Ta, J. Edvinsson, D. H. Rivas, and H. Naas, "A very low-power CMOS mixed-signal IC for implantable pacemaker applications," IEEE Journal of solid-state circuits, vol. 39, pp. 2446-2456, 2004.
[10] H. Le, J. Singh, L. Hiremath, V. Mallapur, and A. Stojcevski, "Ultra-low-power variable-resolution successive approximation ADC for biomedical application," Electronics letters, vol. 41, pp. 634-635, 2005.
[11] H. Wu and Y. P. Xu, "A 1v 2.3/spl mu/w biomedical signal acquisition ic," in Solid-State Circuits Conference, 2006. ISSCC 2006. Digest of Technical Papers. IEEE International, 2006, pp. 119-128.
[12] Y.-K. Chang, C.-S. Wang, and C.-K. Wang, "A 8-bit 500-KS/s low power SAR ADC for bio-medical applications," in Solid-State Circuits Conference, 2007. ASSCC'07. IEEE Asian, 2007, pp. 228-231.
[13] W.-Y. Pang, C.-S. Wang, Y.-K. Chang, N.-K. Chou, and C.-K. Wang, "A 10-bit 500-KS/s low power SAR ADC with splitting comparator for bio-medical applications," in Solid-State Circuits Conference, 2009. A-SSCC 2009. IEEE Asian, 2009, pp. 149-152.
[14] N. Verma, A. Shoeb, J. Bohorquez, J. Dawson, J. Guttag, and A. P. Chandrakasan, "A micro-power EEG acquisition SoC with integrated feature extraction processor for a chronic seizure detection system," IEEE Journal of Solid-State Circuits, vol. 45, pp. 804-816, 2010.
[15] H. Zhang, Y. Qin, S. Yang, and Z. Hong, "Design of an ultra-low power SAR ADC for biomedical applications," in Solid-State and Integrated Circuit Technology (ICSICT), 2010 10th IEEE International Conference on, 2010, pp. 460-462.
[16] D. Zhang, A. K. Bhide, and A. Alvandpour, "Design of CMOS sampling switch for ultra-low power ADCs in biomedical applications," in NORCHIP, 2010, 2010, pp. 1-4.
[17] C.-H. Tsai, Z.-H. Hsieh, and W.-C. Fang, "A low-power low-noise cmos analog front-end ic for portable brain-heart monitoring applications," in Life Science Systems and Applications Workshop (LiSSA), 2011 IEEE/NIH, 2011, pp. 43-46.
[18] J. H. Cheong, K. L. Chan, P. B. Khannur, K. T. Tiew, and M. Je, "A 400-nW 19.5-fJ/Conversion-Step 8-ENOB 80-kS/s SAR ADC in 0.18-μm CMOS," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 58, pp. 407-411, 2011.
[19] Y.-J. Min, H.-K. Kim, Y.-R. Kang, G.-S. Kim, J. Park, and S.-W. Kim, "Design of wavelet-based ECG detector for implantable cardiac pacemakers," IEEE transactions on biomedical circuits and systems, vol. 7, pp. 426-436, 2013.
[20] L. K. Mandrai and K. Sarangam, "200 kS/s, 10-Bit Low Power SAR ADC for Biomedical Applications."
[21] L. Yan, P. Harpe, V. R. Pamula, M. Osawa, Y. Harada, K. Tamiya, et al., "A 680 nA ECG acquisition IC for leadless pacemaker applications," IEEE transactions on biomedical circuits and systems, vol. 8, pp. 779-786, 2014.
[22] Z. Zhu and Y. Liang, "A 0.6-V 38-nW 9.4-ENOB 20-kS/s SAR ADC in 0.18- μm CMOS for Medical Implant Devices," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 62, pp. 2167-2176, 2015.
[23] H. Bhamra, Y.-J. Kim, J. Joseph, J. Lynch, O. Z. Gall, H. Mei, et al., "A 24 μW, Batteryless, Crystal-free, Multinode Synchronized SoC "Bionode" for Wireless Prosthesis Control," IEEE Journal of Solid-State Circuits, vol. 50, pp. 2714-2727, 2015.
[24] Y.-J. Chen, K.-H. Chang, and C.-C. Hsieh, "A 2.02–5.16 fJ/conversion step 10 bit hybrid coarse-fine SAR ADC with time-domain quantizer in 90 nm CMOS," IEEE Journal of Solid-State Circuits, vol. 51, pp. 357-364, 2016.
[25] Y.-P. Lin, H.-C. Chiu, P.-Y. Huang, Z.-Y. Wang, H.-H. Cheng, P.-C. Huang, et al., "An implantable microsystem for long-term study on the mechanism of deep brain stimulation," in Biomedical Circuits and Systems Conference (BioCAS), 2013 IEEE, 2013, pp. 274-277.

AUTHOR PROFILE

Suhaib Ahmed was born in Jammu, India, in 1991. He received the B.E. degree in electronics and communication engineering from University of Jammu, India, in 2012 and M.Tech. degree in electronics and communication engineering from Shri Mata Vaishno Devi University, India, in 2014. He is currently pursuing his Ph.D. degree in electronics and communication engineering from Shri Mata Vaishno Devi University, India. His research interests include data converters, quantum cellular automata, nanotechnology, application of wireless sensor networks in health and environment monitoring, biomedical signal processing and energy harvesting for biomedical implants. He is currently working on design and modeling of ultra low power mixed signal circuits for submicron devices. Mr. Ahmed is a member of IEEE, International Association of Engineers and Associate Member of Universal Association of Computer and Electronics Engineers.

Saima Bashir received her M.Tech degree in electronics and communication engineering from Shri mata Vaishno Devi University, Katra, India in 2016. She is currently pursuing her Ph.D. degree in electronics and communication engineering from National Institute of Technology Srinagar. Her research interests include data converters design, VLSI, analog and mixed signal VLSI design

Bisma Bilal is currently pursuing M.Tech in Electronics and Communication Engineering at Shri Mata Vaishno Devi University, Katra, India. She received her B.Tech degree in Electronics and Communication Engineering from Islamic University of Science and Technology, Jammu And Kashmir, India. Her research interests include Nanotechnology, Quantum Cellular Automata, analog and digital VLSI design and biomedical VLSI

Vipan Kakkar was born in Amritsar, India, in 1973. He received the B.E. degree in electronics and communication engineering from Nagpur University, India, in 1994 and M.S. degree from Bradford University, UK, in 1997. He received his Ph.D. degree in electronics and communication engineering from Delft University of Technology, Netherlands in 2002. He worked in Research & Development at Phillips, Netherlands as engineer and system architect from 2001 to 2009. Since 2009, he has been an Associate Professor with the Department of Electronics and Communication Engineering, Shri Mata Vaishno Devi University, Katra, India. His research interests include nanotechnology, ultra low power analog and mixed signal design, MEMS design, synthesis and optimization of digital circuits, biomedical system and implants design, audio and video processing. Dr. Kakkar is a Senior Member, IEEE and Life Member, IETE and has served as an Executive Member of IEEE, India and has published many research papers in peer reviewed journals and International Conferences. He has also authored a book on System on Chip Design and has served as an editorial board member of microelectronics and solid state electronics journal