Analysis of Two Stage CMOS Opamp using 90nm Technology

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***Abstract*—This paper describes about the analysis of two stage CMOS Opamp which is operating on 1.8 V of power supply on 90nm technology.Since Single Stage of opamp is not efficient enough to produce high gain , so a new stage is added to it . The effect of negative feedback is analyzed that with the help of negative feedback bandwidth of opamp is improved linearity of opamp improved and at the same time gain desentitivity is obtained. There are various other parameters like Power dissipation, frequency response , transient response , A.C response is analysed in this paper .**

Keyword - CMOS,PMOS,Db,Opamp,90nm

I. INTRODUCTION

Since Operational Amplifiers are playing a dominant role in Electronics , Instrumentation and Automotive industry. By keeping in mind these aspects , the need has arisen to improve the various parameters so that more and more efficient devices and equipments can be made. The only effort is to make the practical opamp behave as ideal opamp . Also the various parameters which are obtained from various analysis of opamp must not vary with any process variation or temperature variation . This paper is categorized in three sections . In first section , the basic block diagram of opamp is discussed. The need of second stage is analysed along with the various effects of negative feedback. In second section, there is detailed discussion on Single Ended differntial amplifier used in CMOS Opamp. The design methodology used in simulating a two stage opamp is also discussed . In final section various analysis like frequency , transient , A.C , D.C is observed and results are obatined.

A. . Basics of Operational Amplifier

The basics of Opamp are more clear from the block digarm shown below in figure 1.

In reference to figure 1 , following points can be observed;

1. The first stage of opamp consist of Differntial Amplifiers.

2. The second stage consist of gain stage such as common source stage.

3. The final stage consist of output buffer. It should be noted that if the opamp is motivated towards driving a capacitive load the output buffer stage is neglected

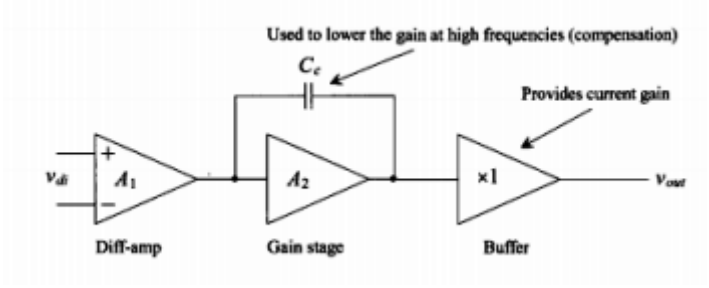

Figure 1: Block Diagram of two stage opamp

1) Negative Feedback in Opamp

Practically the Opamp is always used with negative feedback. Negative feedback is used to reduce the error at output and provide stablity to the system. For negative feedback , a feedback element is used as shown in figure 2.

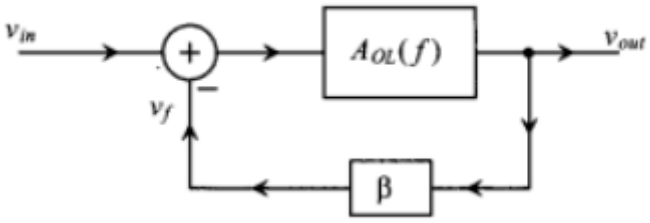

Figure 2: Negative Feedback System

Following are the effects of negative feedback on an opamp:

1. Gain desenstivity

Taking 'A' as gain , closed loop gain is given by=A(cl) while that of open loop gain is given by = A(ol) Consider 'B' signifying beta as a feedback parameter(for convnience) A(cl)=A(ol)/(1+A(ol)B) .After differentiating the above expression it is concluded that the percentage change in A(cl) is always less than the percentage change in A(ol) (1+A(ol)B) is the desenstivity factor.

2. Bandwidth Improvement With the help of feedback the dominant pole will be shifted as a result the bandwidth will increase.

3. Reduction in Non-Linearization Without feedback ,the distortions were arising due to harmonics as a result of which lots of energy were consumed in harmonics but with the help of feedback lineraity is increased.

B. Need of a Higher Gain Stage in Opamp

This higher gain stage is nothing but the second stage .This second stage is included in opamp architecture so that the higher gain can be obatined along with a larger swing .The gain improved in second stage is in the range of 5 to 15 dB . The second stage is nothing but the Common sourse amplifier. Since it is common source, source of MOStransistor is grounde which is more clear from the figure 3 shown below.

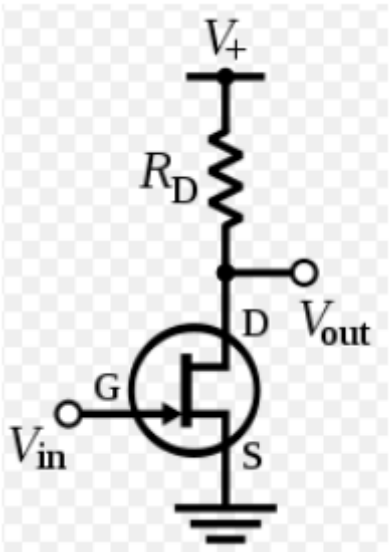

Figure 3: Common Source Amplifier

C. Single Ended Differntial Amplifier in Opmap

The following fig 4 is describing the single ended differntial amplifier used in two stage opamp. Following points are clear from above figure 4:

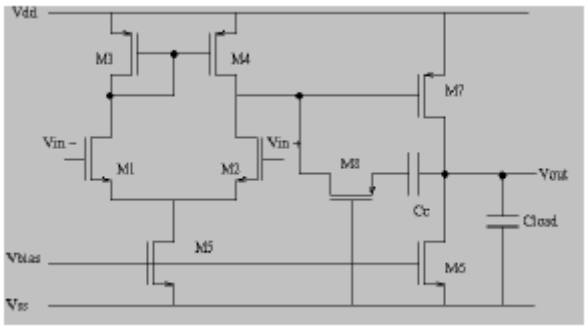

Figure 4: Single Ended Differntial Amplifier in Two Stage Opamp

1. The differential amplifier used above is having two equal but opposite inputs and common output hence known as single ended amplifier.

2.This differential pair is identical and mirror image of each other , hence the current which is flowing through each of them will be same. If it is assume that I(SS) is the current provided by the current source then the current flowing through M1 and M2 will be I(SS)/2.

3. From figure 3, it is also clear that MOS transistor M1 and M2 are V to I(Voltage to current) converter. Since these two transistor are taking volatage at their input terminals and converting the energy into current.

4. Also MOS transistor M3 AND M4 are I to V(Current to voltage converter) 5.Then again the transistor M7 will convert voltage obtained from M4 into current, 6.Finally , the MOS M6 is provided to convert back that current provide by M7 into volatge. Hence at the end we obatin output voltage as v(out). It should also keep in mind that if the Amplifier is driving the capacitive load then we completely neglect the output buffer stage

D. Design Methodology for Two stage Opamp

1) Selection of W/L Ratio:

Out of all the factors W/L ratio is one of the most important parameter in designing any analog vlsi device. So in 90nm technology , W/L for NMOS for PMOS is 1.2.

E. Various Analysis

1) Offset Voltage: The offset voltage is the voltage which is present on input or output terminal due to mismatch during fabrications. It can be obtained by evaluating the voltage at output with zero input. The simulated result is shown below in fig 5.

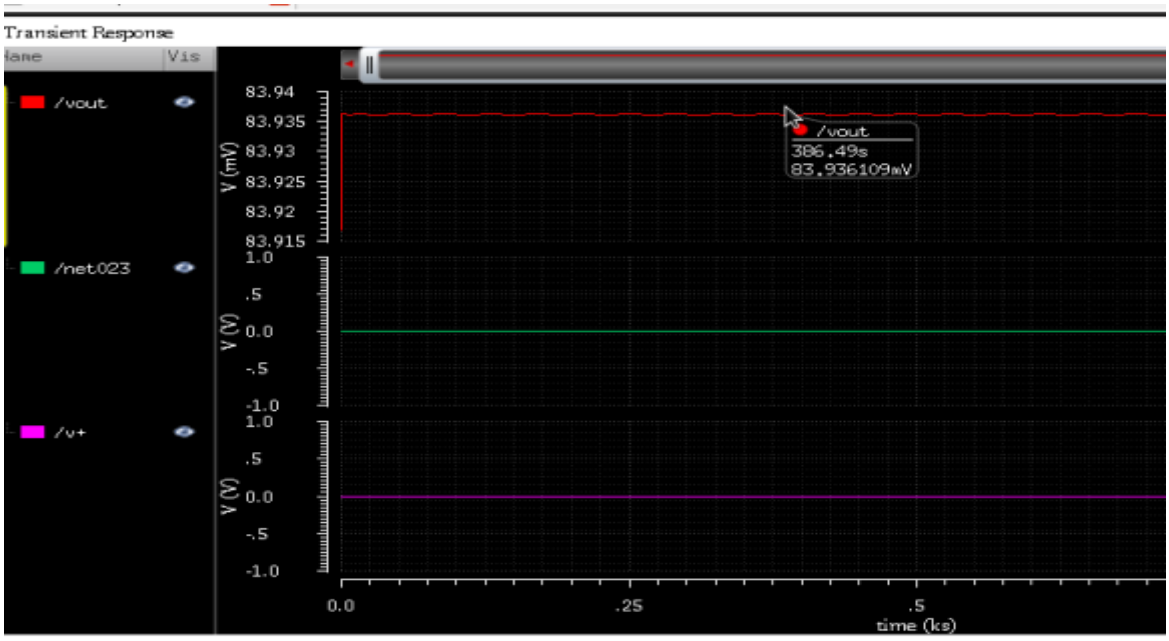

Figure 5: Offset

2) Bandwidth: As we know that the gain of the opamp starts decreasing as the frequency increases and this happens due to various parasitic capacitances present in the circuit. Bandwidth of any circuit simply defines the speed of the circuit that how fast it will be able to amplify any signal. The speed of the opamp is measured by unity gain bandwidth.

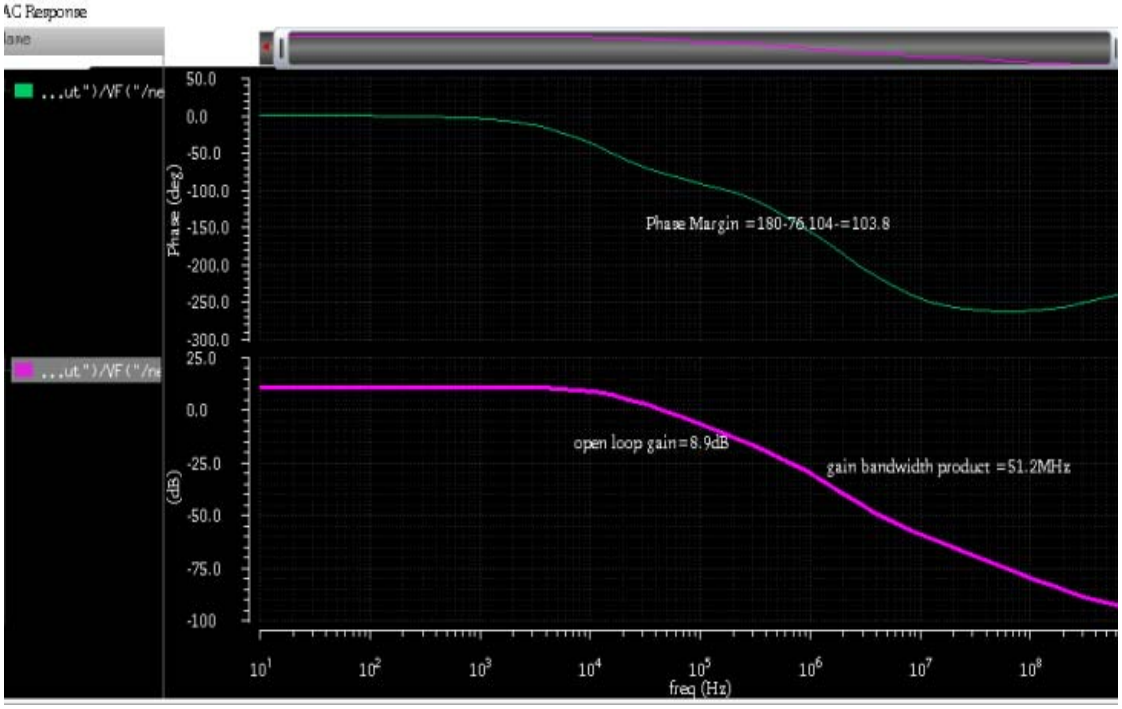

Figure 6: Gain Bandwidth Product

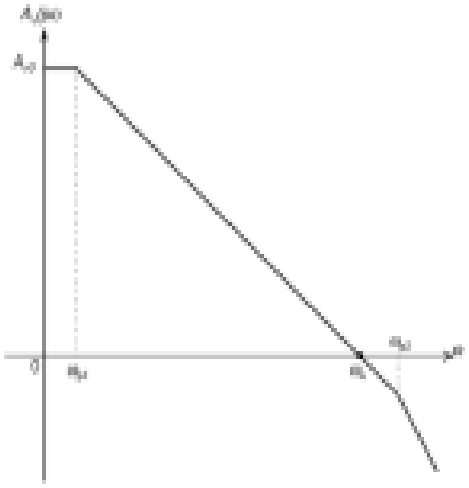

Figure 7 : Opamp Voltage Gain vs frequency plot

3) Differntial Gain: The differential gain is defined as the gain of opamp which is obtained by giving sinusoidal input a both the input terminals of differential amplifier.
4) Phase Margin: Phase Margin is a term which is used to express the relative stablity of closed loop system.The Phase Margin is the amount by which the phase shift is less than 180 (degree)at the frequency where the magnitude of the loop gain is unity. Phase Margin describes the closed loop gain peaking. The simulated results are shown below in fig 8

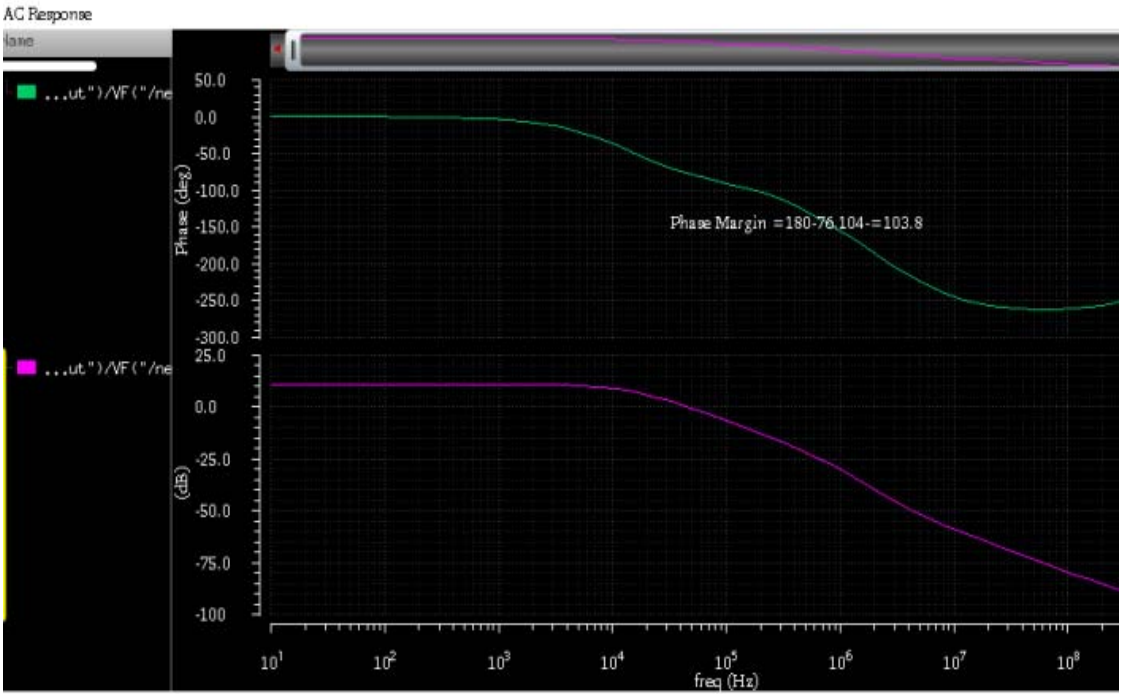

Figure 8: Phase Margin

5) Power Dissipation: In analog VLSI design, the power consumption of the device is of major concern. It should be as low as possible. The simulated Power dissipation is shown below in fig 9

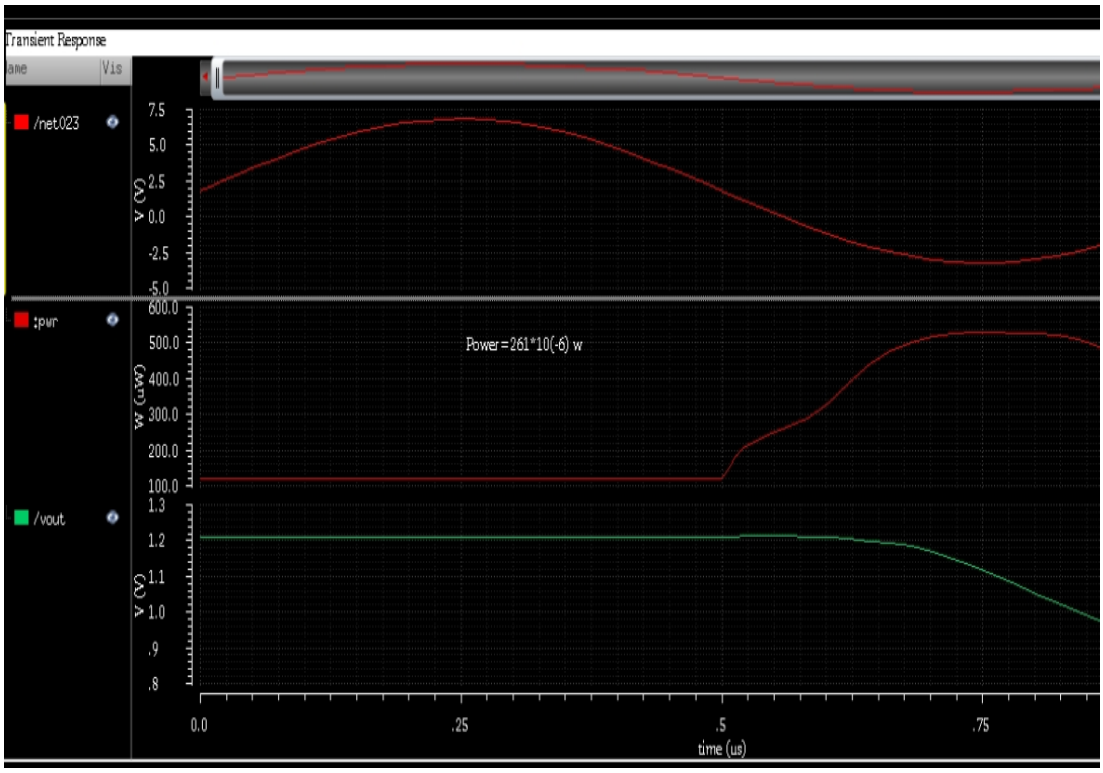

Figure 9: Power Dissipation

F. DC Analysis In DC analysis ,

The operating points are observed also along with them all the transistors must be in saturation is ensured. All the MOS transistors are in region 2 and are in saturation region are shown below in fig 10our paper must use a page size corresponding to A4 which is 210mm (8.27") wide and 297mm (11.69") long. The margins must be set as follows:

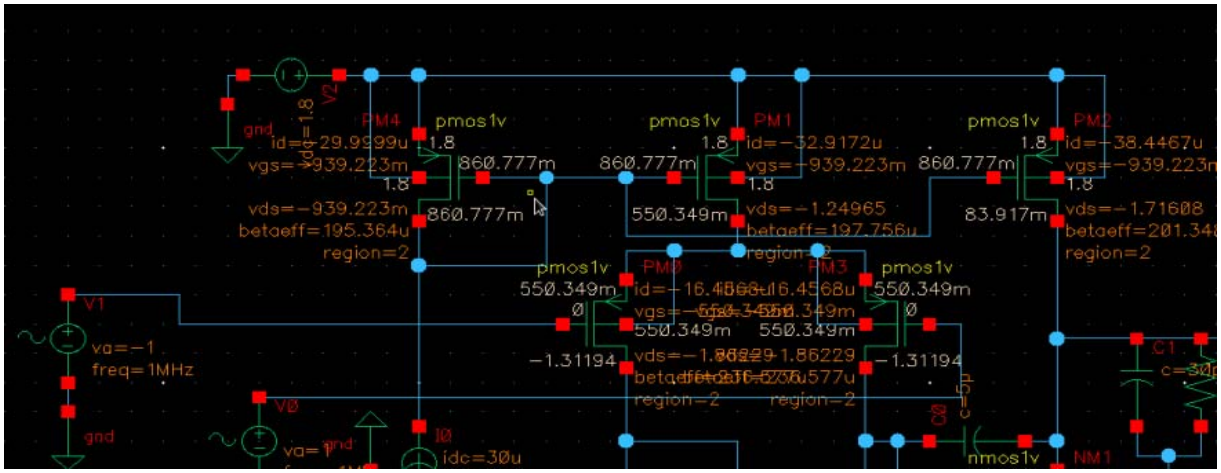

Figure 10:D.C Analysi(all transistors are in saturation)

TABLE I. SIMULATED RESULTS OF TWO STAGE CMOS OPAMP IN 90NM

Parameters	Simulated results
Power supply	1.8V
offset	83.45mV
Power dissipation	261Uw
Phase margin	103.4(degree)
GBW Product	51.2MHz
Capacitance	30pF
Open loop gain	8.9dB
Close loop gain	66dB

II. CONCLUSION

From above discussion , it is clear that the two stage cmos opamp is a very effective methodology designed in analog vlsi Although the gain is not much improved than the single stage but good output swing is achieved. Also from above discussion, it can be concluded that other parameters like bandwidth, gain, transconductance, offset can further be improved using cascode configuration. More effective results can be expected from 45nm or 35nm technology .

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