Design of Architecture for Ladder Diagram based Programmable Controller

Shobha S[#1],K.R.Rekha[*2], K.R. Natraj[*3]
[#]Cambridge Institute of Technology, Bengaluru, India,
[1]shankar.shoba@gmail.com
[*]SJB Institute of Technology, Bangalore, India,
[2]rekha.sjbit@gmail.com
[3]nataraj.sjbit@gmail.com

***Abstract*-- Ladder diagrams are specialized schematics for Programmable Controllers, predominantly used in industries. This paper presents the Architecture of the Ladder Diagram based programmable controller. Algorithms were developed for timer, counter, shift, arithmetic, conversion, coil control and comparison operations and respective modules were designed. Elaborate test benches have been written to validate these design modules using ModelSim. Place & Route of the design has been run using Xilinx ISE Design Suite.The design was targeted ona single Spartan 6 FPGA and occupies 9647 slices of LUT with an operating frequency of 105.6MHz.**

Keyword-Programmable Controller, Ladder Logic, RTL,Xilinx,FPGA

I. INTRODUCTION

Programmable Controllers are equipments used to bring automations in industries.The facility to accept programming in ladder diagram format envisioned the success of programmable controllers in the industry.Ladder logic has evolved into a programming language that represents a program by a graphical diagram that resemble ladders, with two vertical rails and a series of horizontal rungs between them.The basic programming skills needed to develop the applications using Ladder Diagram programs can be learnt relatively quickly and the graphical presentation can be understood almost intuitively, especially suited for Plant technicians. The technique is very easy to understand by any people who are familiar with simple electronic or electrical circuits using symbols of components like relays and switches. Consequently, it is well accepted by operators, electricians and plant technicians.

II. RELATED WORK

In recent years, several dedicated architectures for large scale Programmable Controllers have been proposed, and some of them are used in commercial programmable controllers. A flexible high-performance programmable controller that executes both instrumentation control and electric control in which the language, configuration and computation method of the high-performance single-chip PC processor is discussed [1].A dedicated architecture of a Ladder Solving Processor in which mathematical representation of the ladder language is suggested and algorithms for solving this ladder language are presented using abstract notations [2]. The Ladder solving Processor is an example of array processor architecture. Research work has been reported for a redundant PLC by considering ladder diagrams to be equivalent to a gate and a flip-flop based logic [3]. The authors claim that FPGA is the best choice for redundant PLCs. Formal models using ladder diagrams have been suggested for the programmable controllers that require high level of reliability in critical environment [4]. In order to program a controller the inter-conversion of ladder diagrams to instruction list is suggested [5]. A Programmable Controller uses VLSI circuits instead of Electro mechanical devices that provides intelligent control of unlimited number of complex operations. The system suffers from none of the disadvantages of relay based logic control. Logic can be easily programmed for any application using ladder diagrams. Ladder logic is preferred because it is easy to use and interpret and is widely accepted in industry. It is one of the standardized languages ofr programmable controllers. It is a graphical programming language with representation similar to that of circuit diagrams which can be implemented using FPGA [6]. Ladder diagrams are also used for discrete event controllers [7]. A novel architecture in which each computation of the underlying ladder logic is performed at a fixed number of clock cycles per ladder rung [8]. Software testing is the act of exercising software with test cases for the purpose of finding failures. In the nuclear power plant control system, as existing analog systems have been replaced by digital systems controlled by software, testing of digital control systems has become more important. The control software is usually implemented on PLCs which are widely used to implement safety critical real-time system [9]. The previous works were the design and simulation of the attributes of Ladder diagram and design of timers, counters, shift operations, arithmetic, comparison, conversion and coil control operations [10,11,12,13].

III. PROGRAMMABLE CONTROLLER ARCHITECTURE

Architecture of the designed programmable controller is shown in Fig.2. In the architecture 'clk' signal is used for synchronizing all internal operations of Programmable controller. Active low signal 'reset_n' clears the register indicated by signal 'actual' that represents final result of the operation performed. The Programmable Controller inputs are debounced and are stored in the input image register byte-wise, accommodating 8 discrete inputs per byte. This is organized as 8 bits of data using the address bus 'IO_addr'. Since Programmable Controller processes bit-wise, the inputs (as well as outputs) need to be arranged as an array of single bit. For this sake IOF image register is used in which the information needs to be reorganized as 1 bit for each location pointed by 'O_addr'. IOF Image is a set of one bit memory locations where in the status of input signals and output signals are stored. The signal 'IO_read' enables storage activity in IOF Image and Parallel to serial conversion is proposed for this purpose. The block ps_cnt performs this conversion using the signal 'ps_sr'. The signal 'coil' is energized once the respective operation is completed and the status of it is stored in IOF image in the location pointed out by signal 'O_addr'.

Code memory holds the codes used for performing various tasks. The signal 'code_in' indicates the ladder codes to be stored in code memory. The control signal 'read_code' is used in read operations from code memory whereas the signal 'write_mem' to store codes into it. The signals 'attribute' and 'code' together indicates the type of function to be performed. The signal 'io_address' indicates the address at which the coil status to be stored in IOF image. When code pertaining to the operation to be performed is decoded, the signal 'TRIG' of program unit is activated from the output of Ladder circuit shown in Fig.1, which in turn given as input to the respective module. Program Unit block performs various operations like timing, counting, shifting, arithmetic, conversion, comparison and coil control operations using Ladder Diagram for Programmable Controller. The signals 'Op1' and 'Op2' indicates required data for operation to be performed. The signal 'EN' is a control signal to enable the respective module. Register array module is a set of memory locations of user memory used as registers for temporary storage of data. Three types of registers are considered pertaining to this module, namely, Input Register (IR), Output Register (OR) and Holding Register (HR). The signals 'RM_in' and 'RM_out' are used to write data into and read it from these register arrays. The address of these array locations are indicated by the signal 'RM_addr'. The signal 'RM_rw' when triggered reads the data required for operation from register arrays IR/OR. The signal 'actual' holds the result of various operations to be stored in Register Array Module. The signal 'H_O_write' represents write operation to store final result of the operation performed into Register Array Module.

IV. XILINX P&R RESULTS FOR THE PROGRAMMABLE CONTROLLER DESIGN

Designs are meaningful only if they are mapped on to a target chip such as an FPGA. Hence XILINX synthesis tool is used for synthesizing proposed design. The synthesis tool not only maps HDL design on an FPGA but also brings about an efficient optimization of logic, thus conserving a substantial number of gates. The Place and Route tool report is as follows:

Target Device: Spartan 6 XC6SLX25
Target Package: FGG484
Number of Slice LUTs : 9647 out of 15032 64%
Number of occupied Slices : 3114 out of 3758 82%
Number used as Memory : 1299 out of 3664 35%
Number of bonded IOBs : 248 out of 266 93%
Number of fully used LUT-FF pairs : 4418 out of 10269 43%
The total equivalent gate count for the design: 8,272
Maximum Frequency : 105.6 MHz

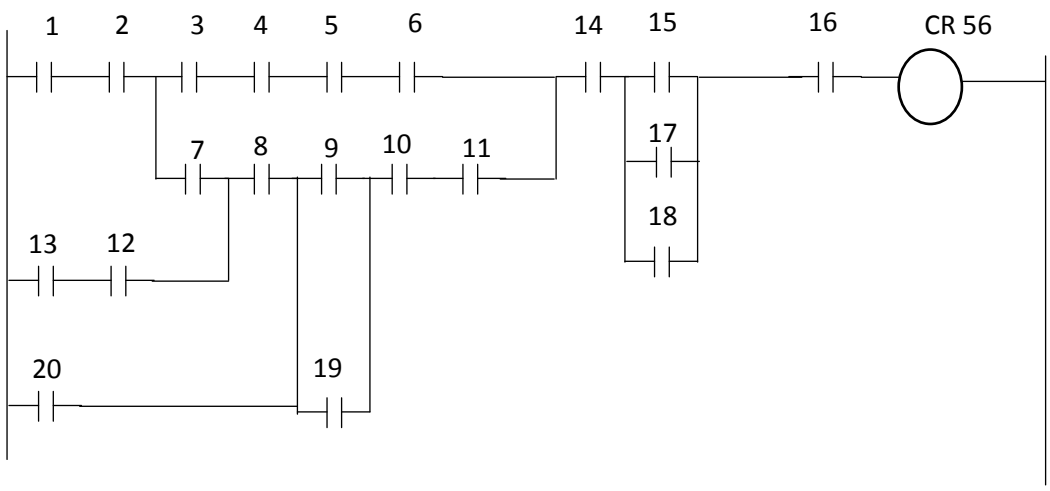

Fig. 1: Ladder Circuit example

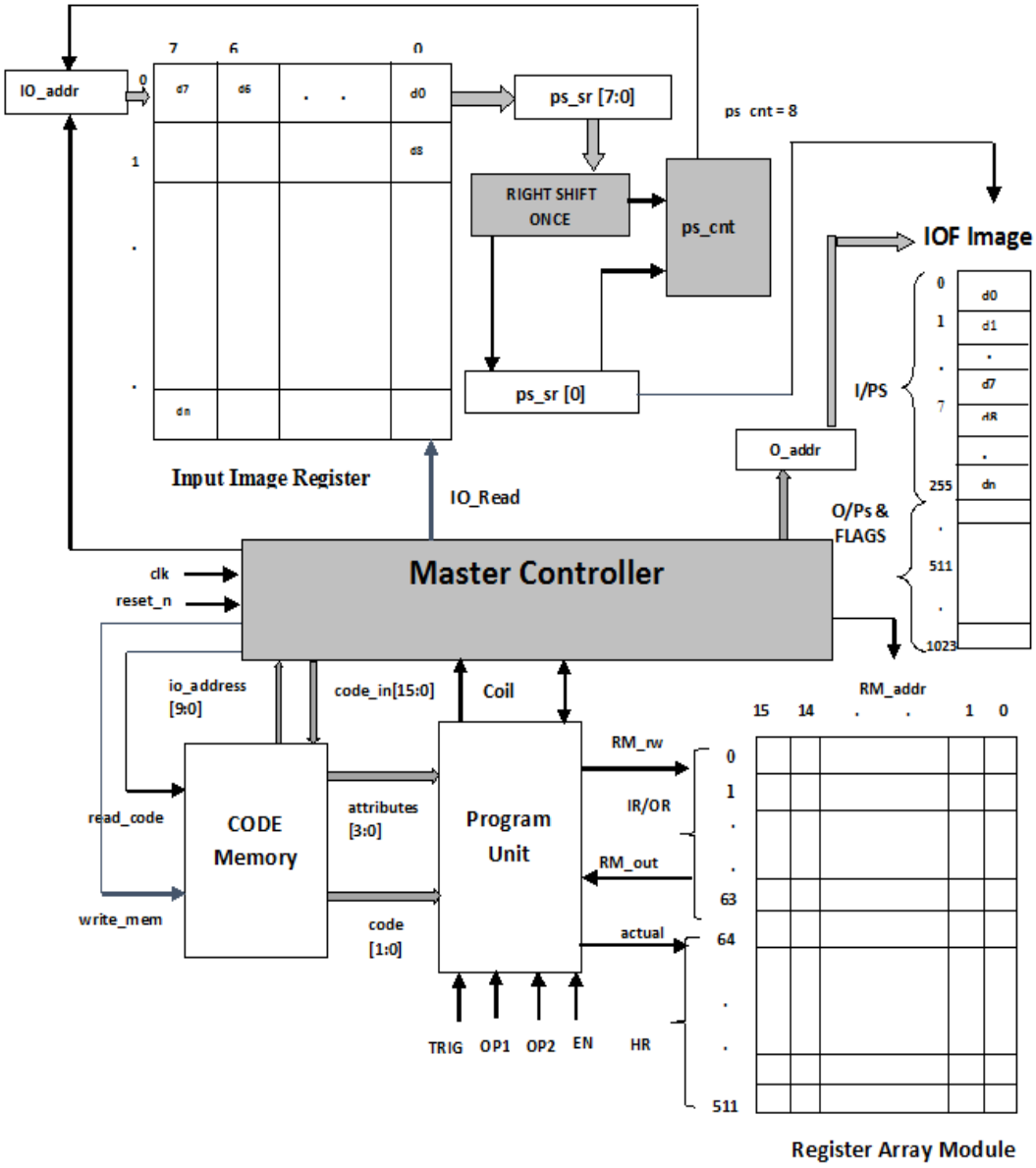

Figure 2. Architecture of the Programmable Controller

V. CONCLUSION

New architecture has been designed for Ladder diagram based Programmable Controller. The design is realized using RTL Verilog. Test bench has been developed in Verilog and the design has been successfully simulated using Model Sim. XILINX synthesis tool is used for synthesizing the design. The design was targeted on a single Spartan 6 FPGA and occupies 9647 slices of LUT with an operating frequency of 105.6 MHz.

REFERENCES

[1] Y. Shimokawa, T.Matsushita, H.Furuno and Y.Shimanuki, " A high performance VLSI chip of programmable controller and its language for instrumentation and electric control", IECON'91, 1991.
[2] Kim J, J Park, and W.H.Kwon, "Architecture of a ladder solving processor for programmable controllers", IECON'91, 1991.
[3] A.S.Pillai, S.K.Dubey, S.J.Gupta, M.M.Patil, "An Affordable Methodology for the Design and Implementation of a PLC on a single chip FPGA", International Journal of Systemics, Cybernetics and Informatics, IJSCI, April 2007.
[4] Da Silva L.D, Gorgonio H, Perkusich A and Martins A.F, "Obtaining formal models from Ladder Diagrams" 9th IEEE International Conference on Industrial Informatics, Brazil, 2011.
[5] LI Dandan, "The new Inter-conversion algorithm between Ladder Diagram and Instruction List", IEEE International conference on Intelligent Computing and Intelligent Systems, 2010.
[6] Miyazawa, I. Nagao, T.Fukagawa, M.Itoh, Y. Mizuya, T.Sekiguchi, T.Kanagawa, "Implementation of Ladder Diagram for programmable controller using FPGA" in Emerging Technologies and Factory Automation, Proceedings ETFA'99, 1999.
[7] Shih Sen Peng Meng Chu Zhou, "Ladder Diagram and Petri-net-based discrete event control design methods", IEEE Transactions Systems, Man and Cybernetics, PartC: Applications and Reviews.
[8] Zulfakar Aspar and Mohamed Khalil-Hani, "Modeling of a Ladder Logic Processor for High Performance Programmable Logic Controller", Third Asia International Conference on Modelling and Simulation, 2009.
[9] Popovic D and V.Bhatkar, "Distributed Computer control for Industrial Automation", Marcel Dekker, Inc., 1990,pp.566-576.
[10] Shobha S, S.Ramachandran, "RTL Logic Realization using Ladder Diagram for Programmable Controller", International Journal of Computer Engineering and Applications, vol. 7, Issue I, pp-148-162, part I, July 2014.
[11] Shobha S, S. Ramachandran, "Realization of Timers, Counters and Shift Registers for Programmable Controller using Ladder Diagram", International Journal of Scientific and Engineering Research, vol.7, Issue 4, pp. 137-148, April 2016.
[12] Shobha S, K.R. Rekha, K.R.Nataraj, "Arithmetic and Comparison Operations for Ladder Diagram based Programmable Controller", IEEE International Conference on Recent Advances in Electronics and Communication Technology, 16th and 17th March 2017.
[13] Shobha S, K.R.Rekha, K.R.Nataraj, "Realization of BCD and Binary Inter conversions and Coil control operations for Ladder Diagram based Programmable Controller" International Journal of Applied Engineering Research.

AUTHOR PROFILE

Shobha S is currently working as Associate Professor in Cambridge Institute of Technology, Bengaluru, Karnataka, India. Her areas of interest are Image processing and Embedded Systems. She is currently pursuing Ph.D.

Dr.K.R.Rekha is currently working as Professor in Sri Jagadhguru Balagangadharnatha Institute of Technology, Bengaluru, Karnataka, India. Her areas of interest are Image processing and Embedded Systems. She has published papers in several national and international Journals.

Dr.K.R.Nataraj is currently working as HoD and Professor in Sri Jagadhguru Balagangadharnatha Institute of Technology, Bengaluru, Karnataka, India. His areas of interest are Image processing and VLSI systems. He has published papers in several national and international Journals.