Design and simulation of Low Power Successive Approximation Register for A/D Converters using 0.18um CMOS Technology

Kalmeshwar N. Hosur[#1], Girish V. Attimarad[*2], Harish M. Kittur[##3], S. S. Kerur[#4]

[#] Department of Electronics & Communication Engg.,
S.D.M. College of Engineering & Technology, Dharwad, Karnataka, India,
[1] kalmeshwar.hosur@gmail.com
[4]kerurss@gmail.com

[*] Department of Electronics & Communication Engg.,
Dayanand Sagar College of Engineering, Kumarswamy Layout, Bangalore, Karnataka, India,
[2]shreyagiri@rediffmail.com

[##]School of Electrical Sciences, VIT University, Vellore, Tamilnadu, India .
[3]harish13579@rediffmail.com

Abstract— **This Paper presents the design and simulation of low power successive approximation register for the Analog to Digital Converters (ADC) using 0.18um CMOS Technology. This acts as digital part of successive approximation ADC. The principle of the Successive Approximation Register (SAR) circuit is to determine the value of each bit of the ADC in a sequential manner, depending on the value of the comparator output. If an N bit analog to digital converter is implemented, there are 2^N possible conversion output values, which means that the SAR needs at least 2^N states and so, as minimum, N FFs. For N bit SAR ADC, the sequence/code register SAR structure requires 2N Flip-Flops and hence power consumption and area occupied is more and Non redundant SAR structure requires N Flip-Flops and a little combinational Logic and hence power consumption is less and area occupied is also less compared to that of Conventional. For 10 bit SAR architecture, the dynamic power consumed by sequence/code register SAR structure is 63.4359uW and non reduandant SAR architecture is 49.2569 uW. The total power reduction using non redundant architecture is 22.35%.**

Keyword - Analog- to- Digital converter, Digital- to- Analog converter, Successive Approximation, Low Power.

I. INTRODUCTION

The rapid development of portable devices such as cell phones, laptops and implantable chips in human bodies and the progress in technology have made the power consumption of microelectronic devices a major concern. The more amount of power is consumed by digital circuits compared to analog circuits. In order to reduce the power consumption of digital circuits, some techniques have been proposed at both the circuit and system level, such as leakage reduction, voltage scaling, clock gating and architectural design techniques, logic reordering and interconnect optimization. In some ultra low voltage applications such as biomedical applications, sub threshold circuits, in which the transistors are biased below threshold voltage, are used. In this we have discussed different design approaches of SAR.

Successive approximation analog to digital converter (SAR ADC) is a capable approach in moderate speed and resolution applications. SAR ADC implements the binary search algorithm using SAR control logic. In general, basically there are two approaches of designing SAR logic. The first one which is proposed by Anderson consists of a sequencer register and code register. In this type of SAR logic 2N flip flops are used. The second is proposed by Rossi, contains N flip flops and some combinational logic [1].

SAR ADC has the benefit of power efficiency compared with other ADC architectures. Moreover, SAR ADC benefits from technology downscaling because of two main reasons: (1) SAR ADC is an op amp-free architecture; and (2) SAR ADC mainly consists of digital circuits. In other words, SAR ADC does not require high gain and high bandwidth op amps to guarantee the linearity. In advance process nodes, a high-performance op amp consumes huge power, and suffers from short channel effect and low supply voltage [2].

Synchronous and asynchronous solutions are investigated for low power SAR control logic. For high-speed SAR ADCs in order to avoid a high-frequency system clock asynchronous processing has been normally used [4]. Many of the limitations of classical SAR implementation are solved by binary search ADC based on Switched Capacitor (SC) realization. In fact, in CMOS technology SC circuits have frequently been selected

because their gain depends only on the ratio between the capacitances, rather than on the value of a single capacitor [5]. LFSR Based SAR Logic is presented in [6]. An LFSR is a shift register that, when clocked, advances the signal through the register from one bit to the next most-significant bit.

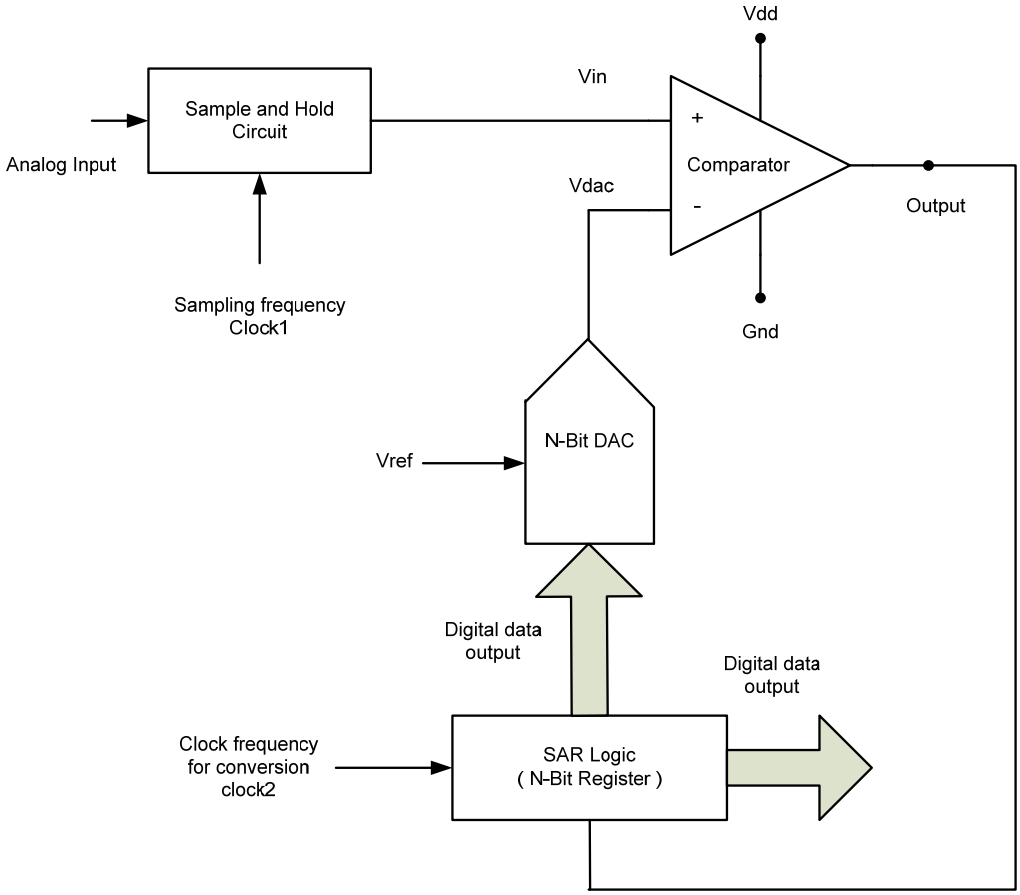

Fig. 1. SAR ADC structure

The basic SAR ADC structure is shown in Fig.1 and mainly consists of sample and Hold circuit, comparator, SAR logic and DAC.

This paper describes Design and simulation of 10-bit low power SAR structure. Section II discusses the low power techniques in digital design. Section III discusses the low power SAR design. Section IV explains the implementation using Cadence. Section V contains simulation results and Section VI contains conclusions.

II. LOW POWER TECHNIQUES IN DIGITAL DESIGN

A. Supply voltage reduction

One of the most important strategies for lowering power consumption is supply voltage scaling in digital circuit design, since dynamic power consumption is proportional to the square of operating voltage. On one hand, reducing the supply voltage will lower the dynamic power consumption, but on the other it lowers the speed, and thus there should be a trade-off in reducing the supply voltage to maintain the system at the desired speed. Low power design is the major concern while the speed has a secondary importance in some applications, such as biomedical devices and sensor networks. For ultra-low power applications Sub-threshold design as a very promising method has been broadly used until now. Since the maximum achievable speed in the circuits that are designed in the sub-threshold area is limited, these circuits are used in ultra-low power applications that need low to medium speed. The supply voltage in this area is below the threshold voltage of transistors (VDD<Vth). Since the threshold voltage changes in different design technology, the operating region of a transistor in sub-threshold designs is not fixed. Operating current in the sub-threshold region is the leakage current, which is significantly smaller than the operating current in the super-threshold area, and as such the speed in the sub-threshold designs is lower. Sub-threshold area in digital designs is defined as a region where the gate-source voltage of all transistors is below the threshold voltage while the drain current remains positive [7] [8]. This area is shown in Fig. 2.

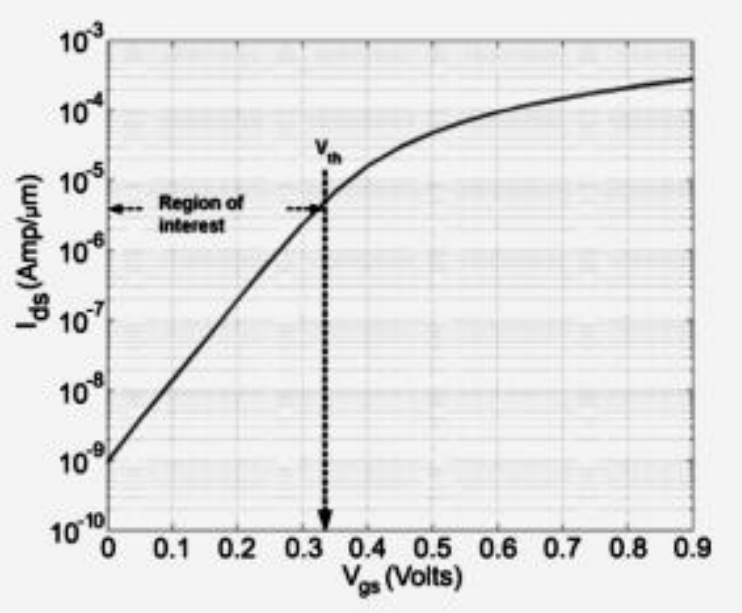

Fig. 2. Region of operation of digital sub-threshold logic.

B. Leakage Power Reduction

There should be a trade off between the switching speed and leakage power consumption with technology scaling. The main strategy used to lower the power consumption is to reduce the supply voltage, which leads in an undesirable speed reduction. To balance for the speed reduction, one way is reducing the threshold voltage which increases the leakage current and therefore the leakage power is increased. This increase in the leakage power consumption is compensated by using different techniques such as dual-threshold voltage schemes, sleep transistors, body biasing, and clock gating. Equation 1, shows that the leakage current in digital designs increases exponentially as the threshold voltage decreases, where Vgs is the gate-source voltage, VDS is the drain-source voltage, Vth is the threshold voltage, n is the sub-threshold slope coefficient which depends on the fabrication process and has a value between 1.3 and 1.5 in new CMOS processes.

$$I_{sub} = I_0 \, e^{\left(\frac{(Vgs-Vth)}{\eta Vt}\right)} \quad (1)$$

The current I_0 is shown in Eq.2, where μ_n is the carrier mobility, Cox is the gate oxide capacitance, V_T is the thermal voltage ($V_T \approx 26$ mv at 300K), and W/L is the aspect ratio of the transistor.

$$I_0 = \mu_n C_{ox} \frac{W}{L} (n-1) {V_T}^2 \quad (2)$$

In dual threshold voltage design techniques, higher threshold voltage devices are used in non-critical paths while critical paths of the circuit that have a main effect on the circuit speed are implemented with the lower threshold voltage devices. The setback with this technique is that it causes delays between different parts of the design. In sleep transistor techniques, additional transistors are used to connect the supply voltage and ground to the circuit, thus providing virtual supply and ground for the circuit. These transistors disconnect the circuit from the supply lines when the circuit is not in an active mode which precludes the direct leakage current between the power supply lines and ground lines. In clock gating techniques, the clock signal is deactivated when the system is in standby mode. The power consumption of the clock circuitry is usually 30-35% of the power consumption of the entire system. It should be noted that the digital circuits used to gate the clock should require a small amount of power to make this technique efficient. Generally, AND gates or OR gates are used to gate the clock in practice; nevertheless, other gates such as XOR gates may be used with equal success [7] [8].

III. LOW POWER SAR DESIGN

There are two different structures have been proposed for SAR. First is the Sequencer/ Code register structure and second is the non-redundant SAR. Both the structures are composed of a particular number of registers to determine and save the value of the bits in a digital word produced by SAR ADC. In the proposed work, these two structures with the objective of reducing their power consumption are considered. These two structures work based on the binary search algorithm. At the starting initial time t_0, the first register which is accountable for determining the value of the Most Significant Bit is set to '1', and puts its value on a bus. After converting this digital word to equivalent analog value and is compared with sampled input of SA-ADC. The output of the comparator determines whether the MSB should be left as '1' or if it should be reset to '0' during time t_1. Then, the second register is also set to '1' during time t_1 and the same process is repeated. Therefore

each flip flop is active only for two clock pulses in each conversion. These registers are in an order from the Most Significant Bit to the Least Significant Bit and after the bit value is determined, this value is saved in its related register.

A. *Basic D Flip-Flop used in SAR Logic*

D Flip- Flop using Transmission gates is shown in Fig. 3. The positive edge triggered D-Flip-Flop is formed by placing RC high pass circuit in front of the D Flip-flop. It uses less number of transistors compared to conventional D Flip-Flop.

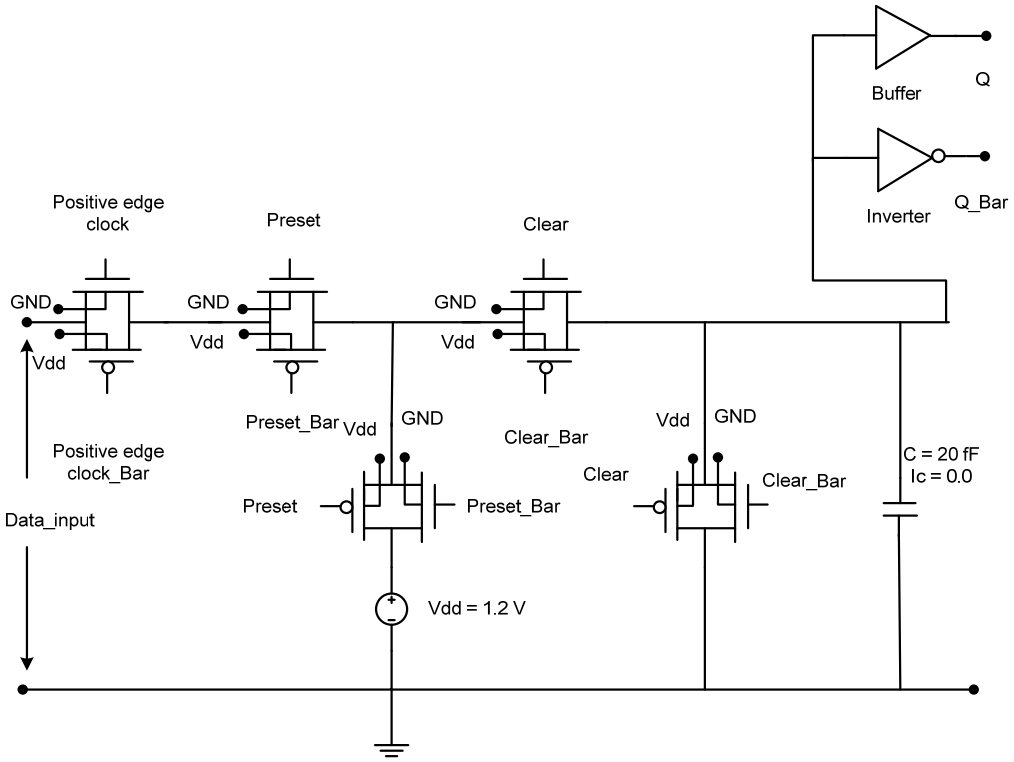

Fig. 3. D-Flip Flop using Transmission gates

B. *Sequencer/ Code register Structure*

This structure has two sets of registers. The set of sequencer registers is in charge of providing the sequence and the registers of code register section are responsible for saving the value of bits. A Sequencer/Code register structure is shown in Fig. 4. To reduce the delay, the non-inverted outputs of the shift registers in the sequencer circuit are used to set the registers of the code register circuit.

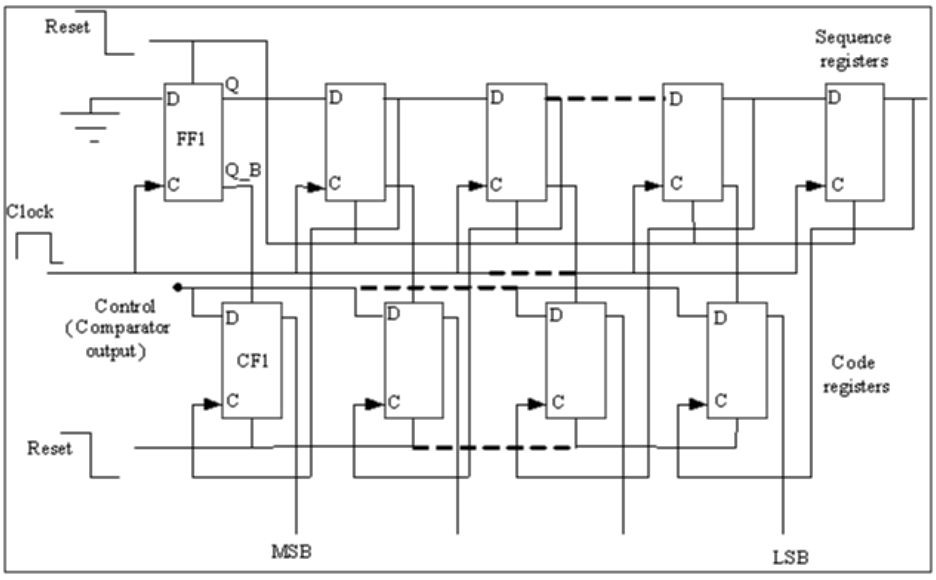

Fig. 4. SAR Logic

The schematic of the SAR logic is as shown in Fig. 4. Firstly the reset input is connected 0 voltage level, and it controls set input of FF1 and reset inputs of all other sequencer register flip-flops. The same reset line also controls the reset input of code register flip-flops. Outputs Q and Q_B of FF1 are set to 1 and 0 respectively. The output Q_B also controls set input of code register first flip flop that is CF1. Therefore the CF1 output is enforced to 1. This is the Most Significant Bit and the weight for full scale range of Voltage is VFSR/2. It is important to note that, since sequence register is reset firstly, the set line of all the code registers flip- flops except CF1 is at logic 1. Thus all the other code register outputs are at logic 0. Hence a sequence MSB is one and all others set to zero logic. The DAC will generate analog equivalent of this weight. When reset input goes high and clock is triggered, output Q of FF1 becomes 0, since D input of FF1 sequence register array is grounded and flip flop two (FF2) outs logic High. This low level to high level transition of flip flop two (FF2) triggers the code register flip- flop CF1 to store control bus value that is comparator output to its output. When clock signal runs further, the code register flip-flop retains the set value as FF2 output goes to zero. In this circuit positive edge triggered D-flip flop is used. This procedure is repeated for each of the flip-flops until after N-clock cycles a high logic comes out of sequencer flip-flop controlling the code register least significant bit flip-flop.

C. *Non-redundant SAR structure*

This architecture uses the minimum number of FFs and is based on the dependency of the state of each bit with the other bits state. The operation principle of the SAR logic is very straightforward: the algorithm of the conversion starts with the activation of the MSB, while all the other bits are 0. Then, going on with the conversion, the remaining bits are sequentially activated, while the value of the one activated just before is depending on the result of the comparator

The fundamental structure of the SAR is a multiple input N bit shift register. At the beginning step, in order to start the conversion, all the flip-flops are forced in the initialization state. Then, for the next states, by adding a multiplexer and a decoder to every FF, each k^{th} register has the chance to choose among three data input lines coming from:

- The flip flop output (shift).
- The comparator output (cmp).
- The flip flop output itself (k).

The selection will depend only on the current state and on the next states of the following register. The schematic with the complete realization of SAR Logic is depicted in Fig. 5 [5].

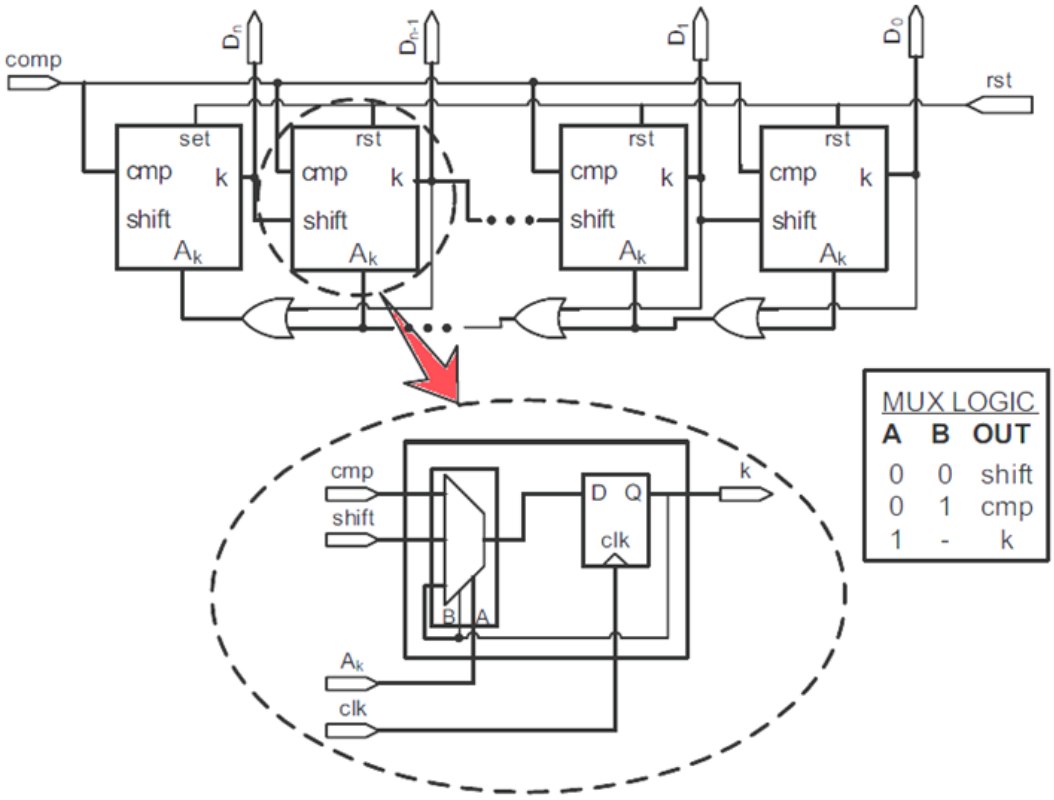

Fig. 5. Schematic of the SAR Logic

IV. IMPLEMENTATION OF SAR

The schematic of 10 bit sequencer code register SAR is shown in Fig. 6 and uses 20 D flip-flops. The preset pulse is made low for 50 nS and high for 500 nS to set the first code register flip-flop and reset the remaining flip-flops. The total period of preset is 550 nS. The clock of 50 nS is used. The data input of first flip flop of sequencer register is applied with zero input. The data inputs of all flip-flops are applied with comparator output that is zero. The low level of 0.0 V and the high level of 1.2 V.

The schematic of 10 bit non-redundant SAR is shown in Fig.7 and uses 10 D flip flops. Flip-flops are reduced to half compared to sequencer / code register SAR structure. The preset pulse is low for 50 nS and high for 500 nS to set the first code register flip-flop and reset remaining flip-flops. The total period of preset is 550 nS. The clock of 50 nS is applied. The data input of first flip flop of sequencer registers is applied with zero input. The data inputs of all flip-flops are applied with comparator out that is zero. The low level equal to 0.0 V and the high level of 1.2 V.

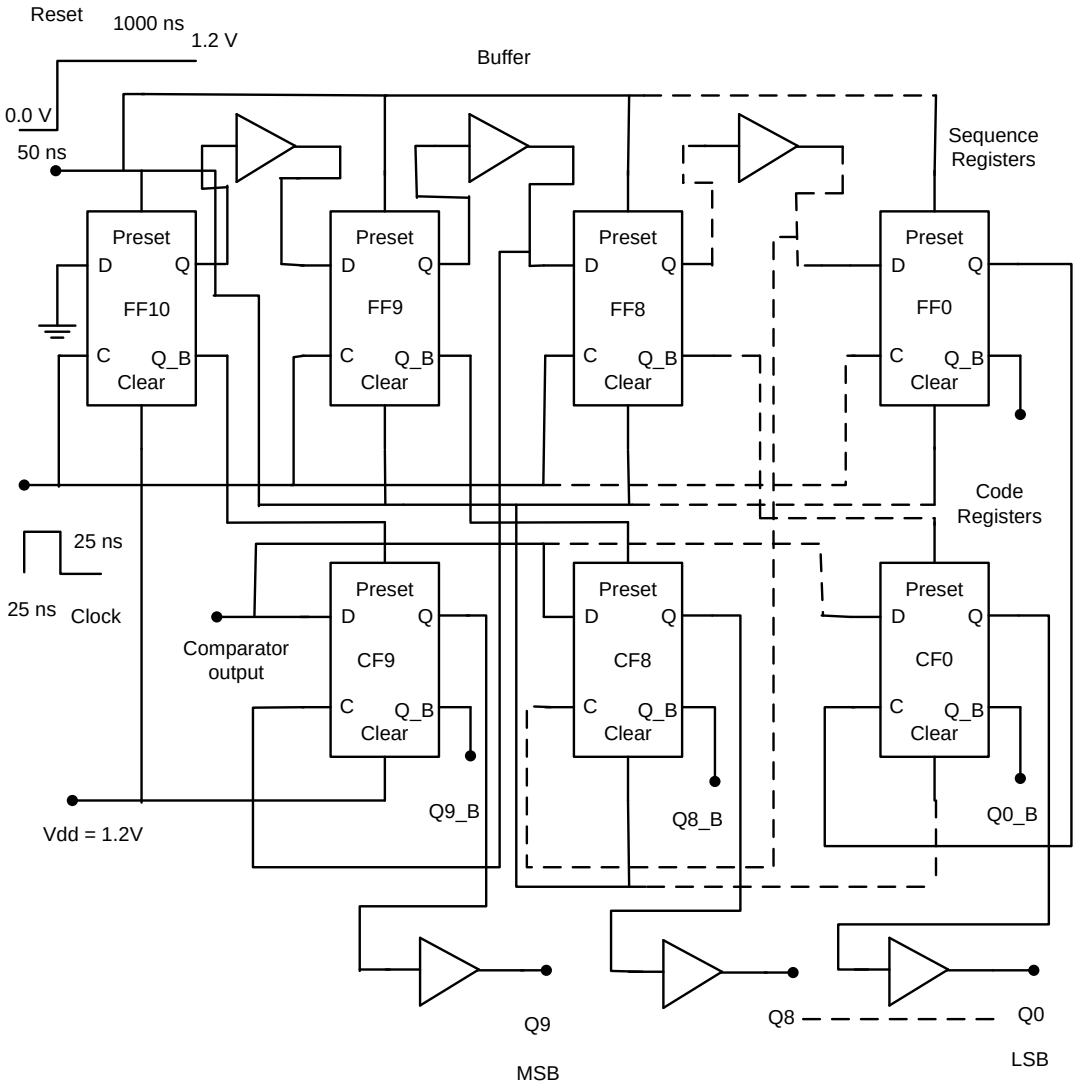

Fig. 6. Schematic of Sequence/Code register structure

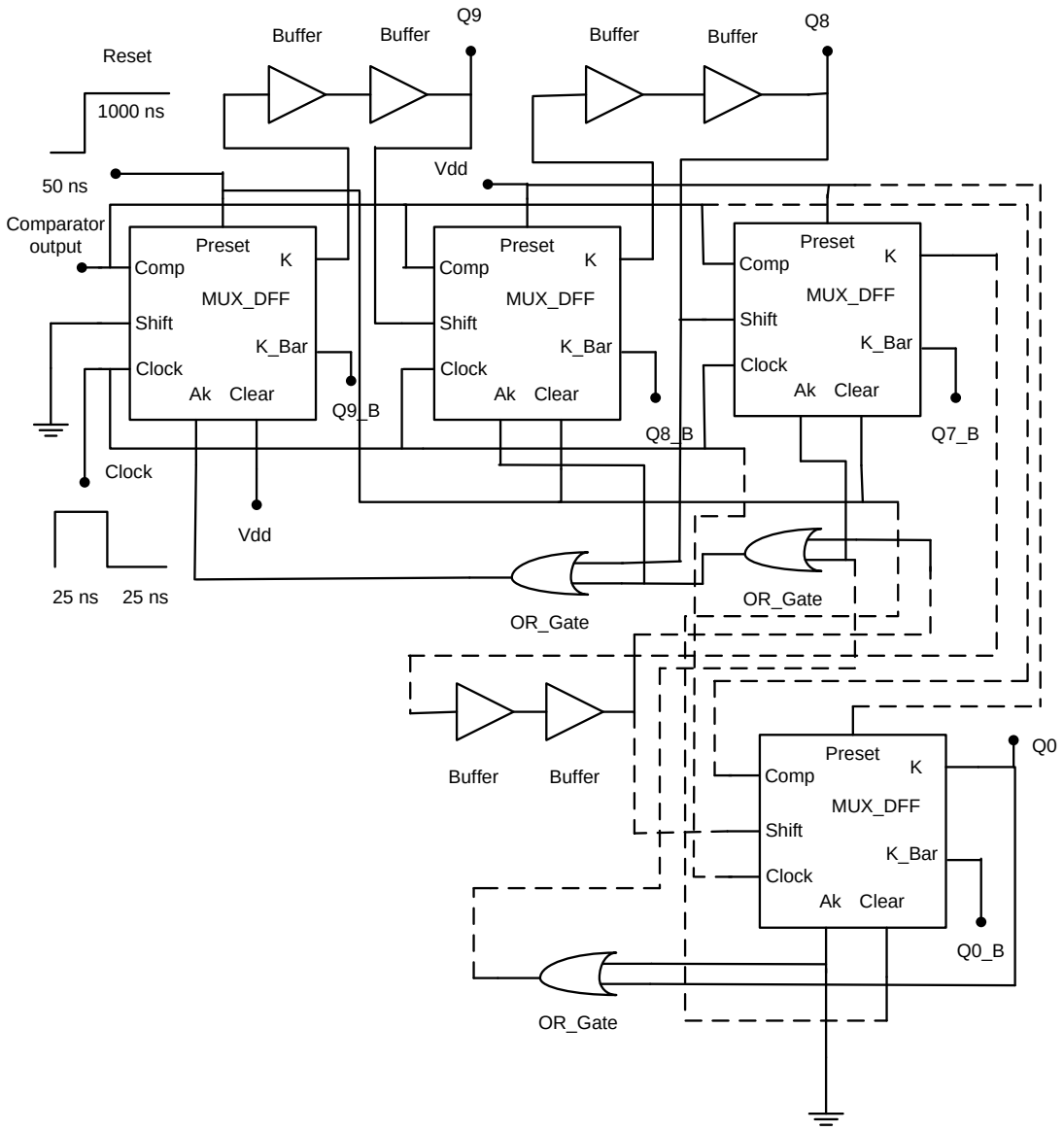

Fig. 7. Schematic of Non-Reduant SAR Structure

V. EXPERIMENTAL RESULTS

The simulation results of sequencer /code register SAR are shown in Fig. 8 and for non redundant SAR structure are shown in Fig. 9. The power consumed by sequencer/code register SAR structure is 63.4359 uW and non-redundant SAR structure is 49.2569 uW and area occupied by this structure is less as it uses less number of flip flops.

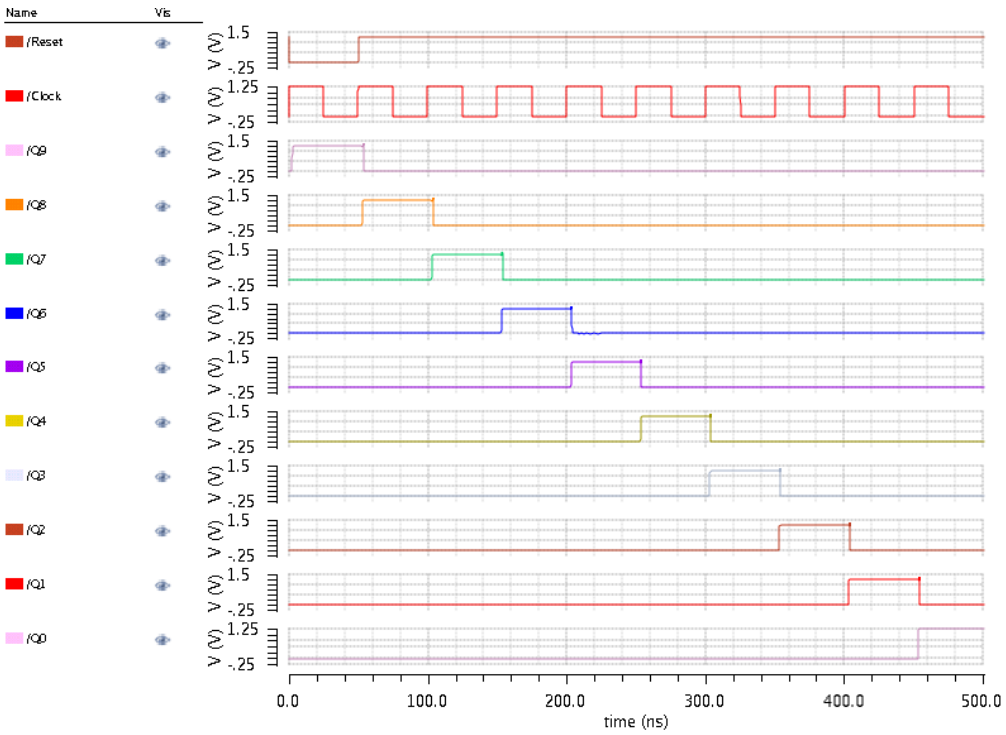

Fig. 8. Simulation Results of Sequencer/ Code SAR Structure

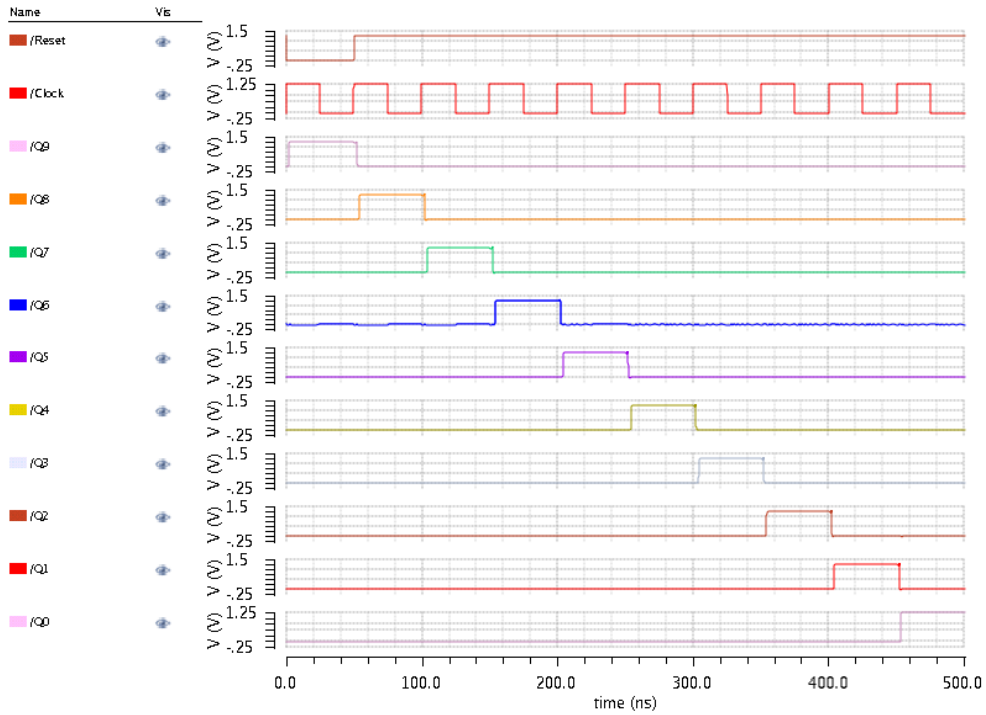

Fig. 9. Simulation Results of Non-Redundant SAR

VI. CONCLUSION

The designed low power successive approximation registers are simulated using GPDK 180 nm CMOS technology. The results of 10 bit sequence / code register SAR structure and non-redundant SAR structures are equal. Flip-flops used in non-redundant SAR structure are exactly half of the flip-flops used in sequence / code register structure with some additional combinational logic. Hence power consumed and area occupied by non-redundant SAR structure is reduced comparably. The dynamic power consumed by Non-redundant SAR structure is 49.2569 uW and for sequence / code register is 63.4359uW. The total power reduction using non redundant architecture is 22.35%.

ACKNOWLEDGEMENT

We thank the management, Principal, Staff of S.D.M College of Engineering and Technology, Dharwad, Karnataka, India, for encouraging us for this research work.

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AUTHOR PROFILE

Author 1: Mr. Kalmeshwar Hosur , working as Assistant Professor in the department of Electronics and Communication Engineering, SDMCET, Dharwad, Karnataka, India. Received B.E (Electronics and Communication Engineering) from Karnataka University, Dharwad and M.Tech (VLSI Design and Embedded Systems) from VTU, Belgaum. Currently pursuing Ph.D in the field of VLSI. Areas of interests are Digital and Analog VLSI Design, Embedded Systems, data converter architectures.

Author 2:Mr. Girish Attimarad, working as Professor and HOD, department of Electronics and Communication Engineering, Dayanand Sagar College of Engineering and Technology, Bangluru, Karnataka, India. Recived B.E (Electronics and Communication Engineering) from Gulbarga University, Gulbarga, India, M.E (Digital Electronics) from Karnataka University, Dharwad, India and Ph.d (Mirowave Communication) from Delhi Unversity, Delhi, India.

Author 3: Mr. Harish Kittur, working as Professor and HOD School of VLSI Design, VIT, Vellore, Tamilnadu, India. Received M.Tech (Solid State Technologies) from IIT Madras, India and Ph.D from RWTH Aachen, Germany. Areas of Interests are VLSI Design, Solid State Technology, and Nanotechnology.

Author 4: Mr.Siddalingappa Kerur, working as Faculty in the Department of Electronics and Communication Engineering, SDMCET, Dharwad, Karnataka, India. Received B.E (Electronics and Communication Engineering) and M.Tech (Digital Electronics) from Karnataka University, Dharwad. Recently completed Ph.D in the field of VLSI. He is Chairman of IETE Sub-center, Dharwad and also National Executive Council Member of ISTE, New Delhi (Karnataka Section). He is having more than 17 years of teaching experience in Engineering Colleges and the 2 Years of Industrial experience. His field of interest VLSI, Architecture design and Embedded systems.