OPTIMUM RESOLUTION OF PHASE FREQUENCY DETECTOR BY CMOS TECHNOLOGY FOR PLL

B.Y. Vinay Kumar *[1], Syed Shameem[2], G.v.Ganesh[3]

[*1]PG Student Department of ECE in K.L.University Green fields-522502,AP,India
vinayboddanapalli@gmail.com
[2]Associate Professor Department of ECE in K.L.University Green fields-522502, AP,India
shameemsyed@kluniversity.in
[3]Assistant Professor Department of ECE in K.L.University Green fields-522502, AP,India
Ganeshgorla_ece@kluniversity.in

ABSTRACT-One of the nonlinear components in PLL is Phase Frequency Detector (PFD),the purpose is to compare two input frequencies in terms of their phase and frequency. In this process jitter will be introduced to the PLL system by PFD. proposed PFD is the preferred approach for detecting weak signals as from a deep space profile. The increase of MOS devices on a single chip will consume more power. Various applications of the PLL such as wireless communication systems, digital circuits, and receivers, targets optimum PFD Design. Optimized PFD reduces jitter effect on PLL and enhances the performance of PLL by increasing the locking range, reducing the phase error variance, reducing the acquisition time and reducing the power consumption. The power consumption in the design of PFD is dependent on CMOS logic of the gates In this paper we propose CMOS PFD, where the performance of the result will be analyzed by using Tanner EDA Tool by considering 45nm technology.

Keywords:-PFD,PLL CMOS Logics and Rise time, Fall time, and frequency

I. INTRODUCTION

CMOS technology is the semiconductor technology used in the transistors that are manufactured in the present days .Nowadays it is a mark able invention for the electronic designers to integrate all the components in a single chip in a system. The new invention towards the technology implementation is speed of the increase of memory, cost decreases and reduction of size of the devices. The transistor occupies less space. The integration of MOS transistors in the design of large multiprocessors, the leakage current in MOS transistors becoming a severe problem. The variations of leakage current increases with the power consumption in MOS transistors. The MOS devices work with only switching voltages in terms of power consumption.

The significance of analog signals represents different conversion parameters takes place in different devices in CMOS technology. The chip designers uses cmos technology based on speed and performance criteria. Phased locked loop are widely used in different applications in analog and digital systems for desired control voltage operating devices.PLL was first described in early 1930s.Frequency modulation is one of the application in the PLL design, used in many devices. The feedback control circuit changes the output according to the desired application by locking the phase of input signal. For instances, the analog signal is implemented by a digital signal with different types of devices i.e. Analog to digital conversion in the design of PFD. Example, comparator takes the analog input signal and it will be change as digital signal by flip flop and counters.

The analog signals used in many different practical applications needs conversion of discrete digital signal in advance such as charge pump. In the design of PFD both analog and digital signal are used, different logics are applied in the design. The knowledge of signals makes the PFD more synthesized, challenging environment.

II. PHASE LOCKED LOOP

Negative feedback system in the design of PLL locks the clock signal, generated by the oscillator of the phase and frequency locked to a reference signal. A reference signal is usually retrieved from a oscillator.

When the PLL gets locked the phase error between output and input signal is zero or should remain at a consistant phase error.PLL is configured with integrated circuit. The PLL design problems can be approached using the Laplace transform technique. It is a feedback system that includes a vco, phase detector, with in its loop. The locking property of the PLL is numerous applications such as frequency, or phase modulation and demodulation. The standard analog PLL implementation is problematic in many application. Analog signal conversion is a challenging process in the design of PFD in the sense of clock. PLL synchronizes VCO frequency to input reference frequency through feedback.
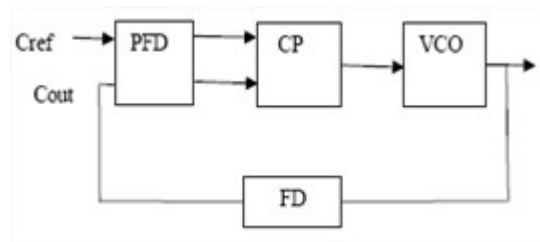
Fig: 1.Block Diagram of PLL

The output signal from vco to the PFD for comparison is called feedback loop, a frequency that is a multiple of the input frequency.PLL can be used to generate a stable frequency at multiple of an input frequency or distribute precisely timed clock pluses in digital clock circuits. The PLL consists of the following fundamental functional blocks namely

A. Phase frequency detector

The main part of PLL circuit is the phase frequency detector.PFD is typically an error amplifier The main working principle of pfd is to compare two input signals Cref and Cout.The both outputs, up signal and down signal are given to the charge pump circuit to give single output.[2]It compares the input frequency and generates an output signal which is a function of the difference between the phases of two input signals. The output signal of the device is dc voltage. It is asynchronous sequential circuit. A phase frequency detector prevents a false lock condition in PLL applications. It compares the phase at each input and generates an error signal. Phase frequency detector is not capable to detect large frequency differences hence not used generally, the error pulse is named as up and down pulse for the purpose of simplicity. If the phase difference between input and output is positive then it generates an up signal.The difference in phase or frequency can be detected by only PFD in the PLL system, as only this block talks with both the signals.This block generate a signal to slow down the vco frequency.The down pulse is nothing but the signal which will order the vco to step down its frequency or in other words to slow down. Similarly an signal is generated to tell the vco to catch with the reference in case its frequency has slowed down as compared to reference clock Proposed PFD operation using nor gate
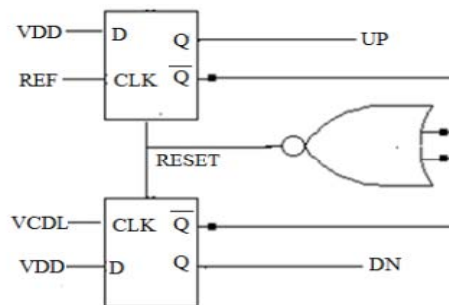

Fig 2.Block diagram of nor gate PFD

At any point of time ,the PFD can be in one of the four states

UP=0 and down=0

UP=1 and down=0

UP=0 and down=1

UP=1 and down=1

The up and down signal leads that of voltage control delay line(VCDL) then up goes to logic low. i.e up keeps high until the rising edge of VCDL makes down signal on low level. The up and down signals are in the operation of nor gate.so reset goes to logic high and resets the PFD in to the initial state

B. Charge pump

Its function is to provide a large open loop gain by pumping charge in to the loop filter the amount of charge pump is proportional to the amount of phase difference detected by the PFD.since the capacitor is an open circuit for direct current, charge accumulates very quickly and results in a large dc gain which causes the final steady state phase error between the input and the output to the very small the theoretical dc voltage for a charge pump based PLL is infinite, however in practice this is impossible It consists of two input signals coming from the PFD.It consists of current sources and switches. The charge pump and low pass filter govern the stability

and smoothness of the PLL system. The charge pump produces a single output depending on charging and discharging state of the charge capacitor.

C. Voltage control oscillator(vco)

The frequency of oscillation can be control by an externally applied voltage. The Voltage control oscillator provides the relationship between the applied voltage and applied oscillation frequency. The design of VCO is done by externally applied voltage.This voltage refers frequency variation and phase. The output frequency is called center frequency, happens at externally applied voltage or control voltage is zero. The input voltage to the VCO changes its output frequency, that reduces the difference between phase and frequency of VCO. The error(or) control voltage applied as an input to the vco.once locked,PLL tracks the frequency changes of the input signal.PLL goes through three states free running, capture and phase locks.The effect of noise in control voltage minimizes the gain of VCO. The phase variation in the input of VCO is effected by noise.

D. Frequency Divider

Frequency divider is also called a clock divider. It is in the feedback loop and hence it decides the stability also.In advanced transceiver the dividers operating at microwave frequencies also.It takes the input from the output of VCO.The noise introduce from the VCO creates same harmonics in the frequency divider.The PLL requires programmable frequency dividers, operates at higher frequencies, in the selection of channels in advanced applications.In frequency divider the desired division ratio is selected by means of multiplexer, controlled by control lines, takes less noise.

III. Design of PFD by using Different logics

A. Dynamic logic using PFD

Dynamic gates require monotonically rising inputs during evaluation.Dynamic logic is having two modes one is pre-charge and evaluate It is having no static power dissipation minimum clock frequency must be maintained. Dynamic gates suffer from charge sharing. Dynamic circuit's temporary storage of signal values on the capacitance[3] of high impedance nodes popular in the 1970's. These circuits are usually faster than static counter parts. Counter has a higher toggle rate than static logic[4].But the capacitive loads being toggle are smaller[5].so the overall power is uniform when referring to a particular logic family it is so called distinguished from static circuit. For most implementation of the design, a clock signal is not even needed. It requires minimum clock rate, fast enough, power saving technique can be designed in a dynamic logic based system. It requires less no of transistors to implement for a given logic. Once the output of dynamic gate is discharged, it cannot be charged again until the next pre-charge operation.
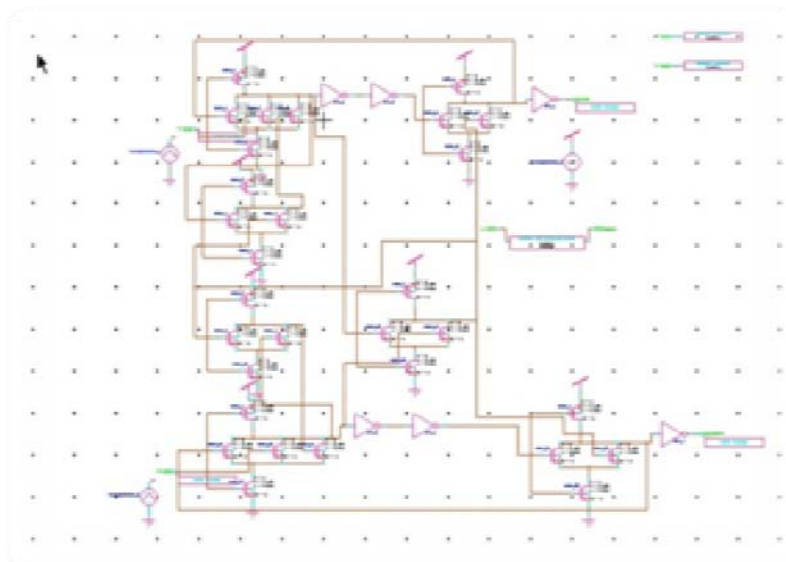

Fig 3.schematic of Dynamic logic pfd

B. Domino logic using pfd

In Domino logic the relationship changes between input parameter and pickup signal compared width equal static cell.A domino buffer shown figure[5] with MOS transistor of PMOS and NMOS respectively.Assume the gate capacitances of MOS transistor is same per unit dimension for a domino logic it is possible to built a buffer with the same signal strength, but which has unit dimension. As one of the input parameter for the same signal strength it is possible to design with high capacity buffer. The buffer is a connection of different types of MOS transistors connected in series. A clock input is given one of the MOS transistor, one side of the MOS transistor is connected to the ground terminal.An inverter is connected in parallel with the MOS transistors connected in

series. Resistance of MOSFET is inversely proportional to drain current.Drain current is proportional to channel width. Hence resistance is inversely proportional to channel width. The series resistance of MOS transistors is equal to sum of the resistance of individual transistors.It is constructed by the series combination of the one PMOS transistor and two NMOS transistors.Generally the width of PMOS transistor is less than the NMOS transistor for inverter. The width of PMOS is greater than NMOS transistor.The output is taken from the inverter side.The degradation in signal strength for the PMOS transistor in a Domino buffer is weak as compared to NMOS transistor that are connected in series.The dimensions of PMOS transistor will depend on time available for the output, this time is called delay. This delay is called pre-charged delay.
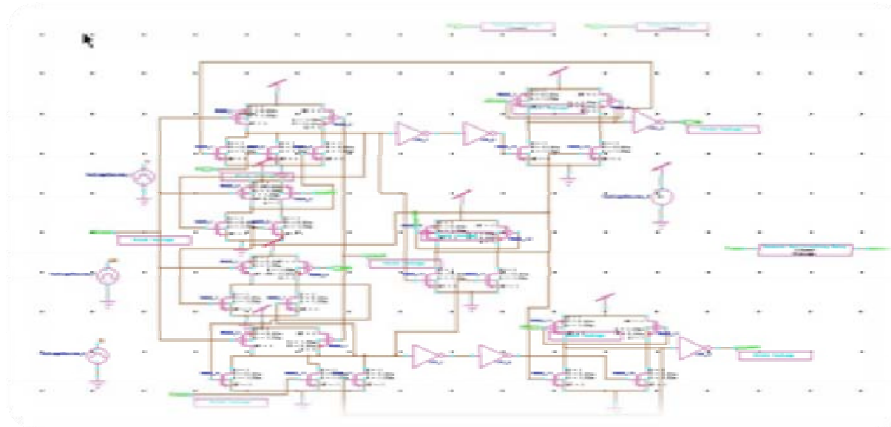

Fig 4.Schematic of Domino logic pfd

The width of PMOS to NMOS transistor tend to be lower in the logic condition.Weak signals dominates in domino cells in the sense in order to get better output conditions.The logic is having a high speed operation. Any input condition to switch logical states that results alternate switched on and off conditions.For the transistors the input conditions for the cells will given an output in terms of rise and fall condition.

The ratio of width of PMOS to NMOS will increases or decreases the speed of rise or fall of the transistor.The speed of operation will effect the switching of transistor becoming slower. It is difficult to rise transision in domino cells.The alternate transision causes the static cells tends to nearer to the supply voltage level (VDD).The input signal causes to discharge in the domino cell,there is no struggle exist between PMOS and NMOS transistor .This causes the switching action, will start when the input voltage reaches threshold voltage level.The switching action of the voltage of a Domino cell will effect speed up operation.The input voltage above threshold level leads domino cell faster operation.
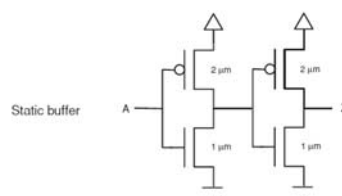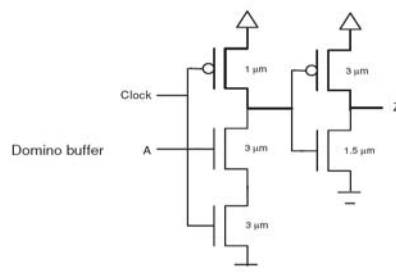

Fig 5.Static buffer

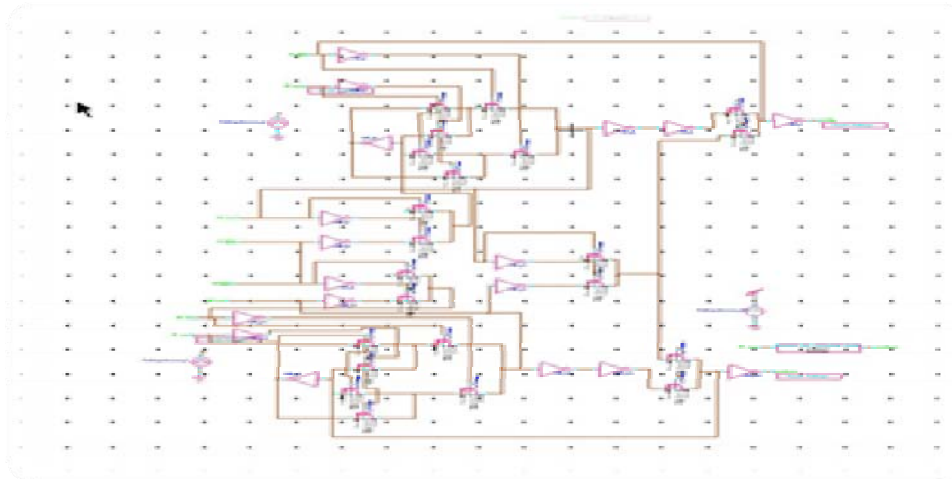Fig 6.Domino buffer

C.   Pass transistor logic

Fig 7.schematic of pass transistor logic pfd

It often uses fewer transistor requires less power, runs faster. The transistors used as switches to pass transistor logic levels between nodes of circuits, instead of switches connected directly to supply voltage. This reduces the no of active devices.

The logic is implemented to digital systems successfully which are faster and performed efficiently than static CMOS implementation. for the same design.It has small input capacitances. Delay analysis is not as well defined in terms of sizing choices, very efficient in use of transistors. Potentially very efficient layout results, usually more internal node capacitances than with conventional CMOS gates. Propagation delays can become large in long series string of pass-transistor. Static power dissipation is unaffected, dynamic power dissipation may be decreased.
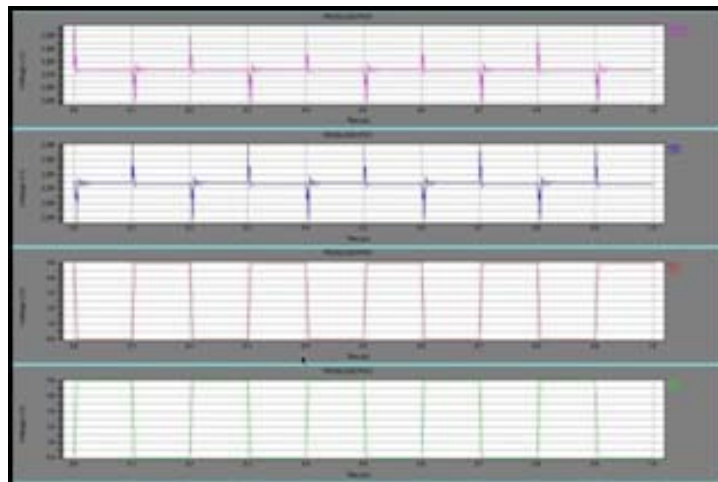
IV.   Simulation results
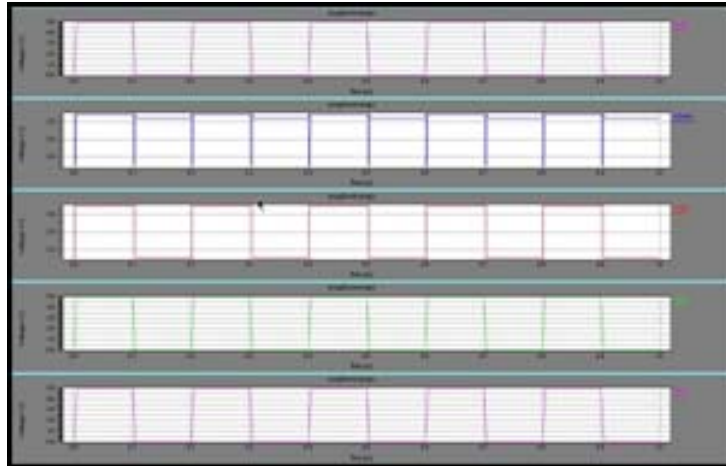

Fig 8.Dynamic logic using pfd
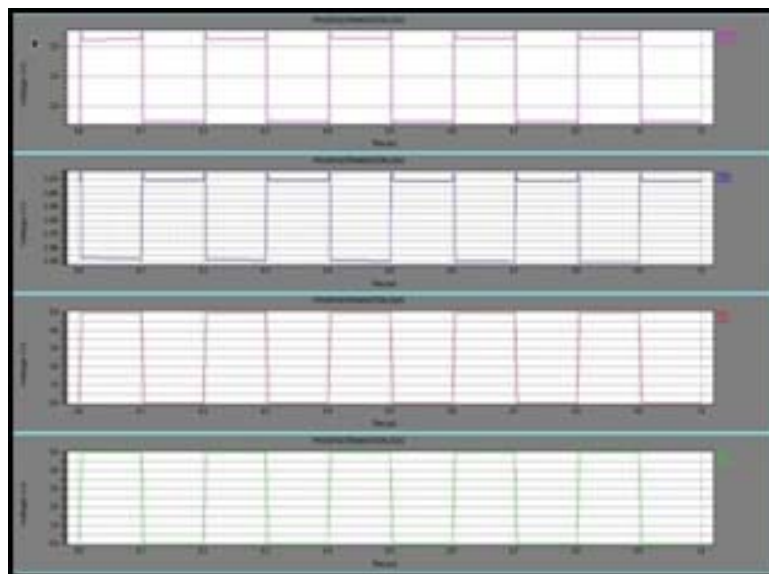
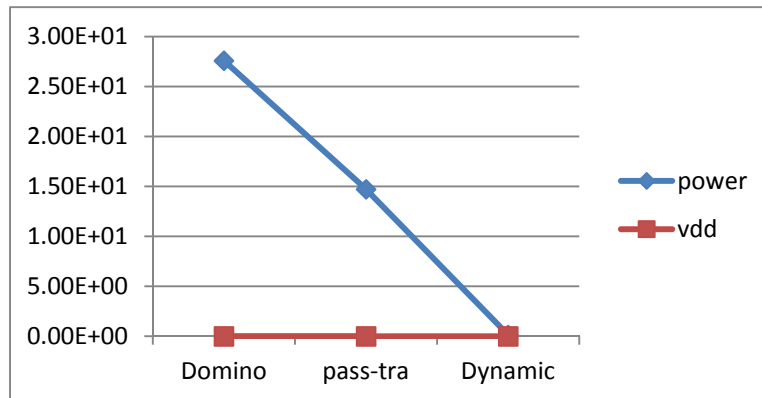Fig 9.Domino logic using pfd

Fig 10.Pass transistor logic using pfd

Fig 11.power vs vdd
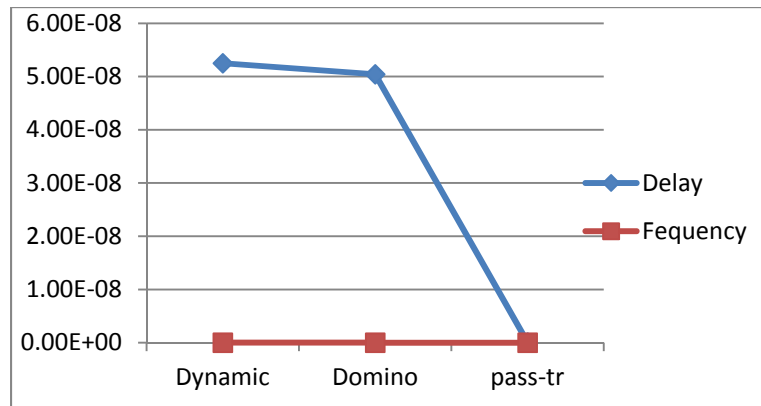
Fig 12.Delay vs frequency

TABLE-I

Parameters	Dynamic logic pfd	Domino logic pfd	Pass transistor logic pfd
Max operation frequency	5MHZ	5MHZ	5MHZ
Max power	1.476354e-001 at time 2.60807e-009	5.517701e+001 at time 9.05118e-007	3.040616e+001 at time 5.05e-007
Min power	1.389881e-001 at time 1.21472e-007	1.885099e+000 at time 3.01012e-007	2.129307e-001 at time 5e-009
Power consumption	1.393406e-001	2.759424e+001	1.472406e+001
Transistor counts	42	42	56
Delay	5.2500e-008	5.0430e-008	4.6456e-011

TABLE-II. Performance Comparison

By Comparison of above result we discuss different types of power consumptions per transistor by different logics as follows.

Logic conditions	Maximum power(w)	Minimum power(w)	Power consumption(w)
Dynamic logic	0.0351	0.0330	0.0331
Domino logic	0.1313	0.0448	0.0657
Pass-transistor logic	0.0542	0.0380	0.0262

Dynamic logic pfd consumes less maximum power during rise time. It takes less minimum power consumption among different logic conditions. Operating frequency is same for all logic conditions 5MHZ.

CONCLUSION

This paper represents different PFD implemented technology by nor gates in 45nm technology. PFD designed with different types of logics has been proposed in this paper. The dynamic logic pfd has optimum power consumption with 30 transistors with a maximum delay of *5.2500e-008 and* operating frequency is maximum at frequency of 5MHZ.

REFERENCES

[1]   Ashwini Rajole Author "online case study on phase frequency detector" ISSN(online):2319- 7064 volume 4 Issue1,January 2015.
[2]   Rhruti, R Angadi and Dr.k.Rekha Author's "Design of pass transistor based phase frequency detector for PLL applications"ISSN:2278-0181, vol.4, 05, May-2015.
[3]   Lars wanhammer(1999).DSP integrated circuits Academic press.P.37.ISBN 978-0-12-734530-7
[4]   Andrew marshall and sreedhar Natarajan (2002).SO I design; analog, memory and digital techniques. Springer P.125, ISBN 978-0-7923-7640-8.
[5]   A. Albert Raj and T.Latha "VLSI Design" PHI Learning pvt ltd, p.167.ISBN 978-81-203-3431-1
[6]   Raj Nandini, Himadri singh, Raghav and B.P Singh "Design of Low power phase frequency Detectors for delay locked loop"International Journal of Emerging science and Engineering, ISSN:2319-6378, volume-1,Issue-5,March 2013.
[7]   Abdul Majeed K K and Binsu j kailath "A novel phase frequency detector for a High frequency PLL Design" International Conference on Design and manufacturing,IconDM 2013.

[8] Supraja, Batchu, jayachandra Prasad, Talari Ravi and Nirlakalla"Analysis of Low power and High speed phase frequency detectors for phase Locked Loop Design"3rd International conference on Recent Trends in computing 2015(ICRTC-2015).
[9] Janani.s and Dr.M.jagadeesawari"An Efficient Domino logic style for cmos circuits" ACEEE.
[10] Sung mo kangi and yusuf Leblebici(2003) "cmos digital integrated circuits. Analysis and design". MCGraw-Hill, ISBN 978-0-07-246053-7.

Boddanapalli Yamini Vinay Kumar was born on 13th August 1991, in A.P., India. He received his, B.Tech degree in Electronics & communication Engineering from Jawaharlal Nehru Technological University, Kakinada, A.P., in 2014. Presently he is pursing M.Tech VLSI Technology in KL University. His research interest include analog, FPGA implementation.

Syed Shameem he receive his B.Tech in ECE, M.Tech in Microwave Engineering and P.hd is done in MEMS. He is working as Assoc Professor in K L University. His interest focuses on Biological sensors and MEMS.

Venkata Ganesh.G He received B.Tech from JNTU, Hyderabad M.Tech from Andhra university in 2007 and 2009 respectively. He is working as Assistant Professor in K L University. His interest focuses on nanoelctronics.