

Feasibility of Back Probagation Network in The Design of Viterbi Decoder

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Abstract— Convolutional coding is the most widely used coding technology for reliable data communication. At the receiver's end, Viterbi decoders are used for extracting the message bits. A conventional Viterbi decoder not only occupies higher memory space, but also is computationally more complex. Though considerable research is performed in this area to overcome these challenges, an efficient architecture is yet to be developed. In this paper, feasibility of a soft computing technique that substitutes the Viterbi decoder has been explored. The proposed Viterbi decoder works satisfactorily in terms of accuracy in robust environment.

Key Words- Viterbi decoder, Back Propagation Network, Accuracy, convolutional codes

I. INTRODUCTION

In wireless communication, convolutional encoding enhances the reliability of data transmission. A Viterbi decoder used for decoding the codes is successful in correcting 1, 2, 3 bit errors. However as the number of bit errors increases the computational complexity of the decoder also increases. A Viterbi decoder consists of Branch Metric Unit(BMU), add Compare Select Unit(ACSU), and Survivor Memory Unit(SMU). In recent years extensive research is carried out to reduce the complexity of constituent unit. However due to the inherent properties of BMU, ACSU, SMU, complexity is yet to be reduced. The paradigm has now shifted to the use of soft computing technique for replacing a part of the Viterbi decoder. However the complexity can be further reduced if the entire Viterbi decoder is replaced with the soft computing algorithm. In this paper the feasibility of Back Propagation Network (BPN) for replacing the entire Viterbi decoder is explored. BPN is a multilayer feed forward network which uses supervised learning and is used for prediction and classification. It learns from the set of exemplars, used for learning and updates its weight accordingly. With the updated weight, it predicts the output for an entirely new set of input. Hence a BPN can be successfully used for predicting the message bits from the convolutional encoded bits. This paper is organized as follows: Section II describes the related work. In Section III, an overview of BPN is provided. Section IV compares the accuracy of the proposed BPN based Viterbi decoder. Section V concludes the work.

II. RELATED WORKS

Klaus Haeske 2007 used recurrent Neural Network for the decoding of convolutional error correction codes. The impact of shape of the activation function and level of self feedback of the neurons are also studied. In order to perform the operations, code with $R=1/2$ and $K=3$ is used, the encoder polynomials are D^2+1 and D^2+D+1 . In order to reduce the limitations caused by local minimal, Gaussian noise is added during the iteration process. The proposed RNN based convolution decoder had less number of iterations and increased the conventional Viterbi decoder.

JinJin He et al 2012 proposed a high speed low power design for Viterbi decoder that was used in Trellis Coded Modulation (TCM) decoders. Here a novel implementation of T-Algorithm is proposed to reduce the decoding speed in determining the optimal PM in order to increase the speed of a rate-3/4 Viterbi decoder, a 2 step precomputation method was proposed. In the proposed approach the conventional 64 to 6 priority encoder was replaced with 3 4 to 2 priority decoder it is found that the precomputational architecture had reduced the power consumption without sacrificing the decoding speed. It has reduced the power consumption by 70% and the maximum decoding speed by 11%.

Padmapriya, Praveenkumar 2013 encoded serial binary data with convolutional coding (rate of $1/2$ or $2/3$ or $3/4$). Coded serial signal is then grouped into symbols of $1/2/4/6$ based on data rate and then serial stream signal was converted into complex constellation points, parallel such carriers are then modulated and demodulated using IFFT and FFT pairs. It was found that Bit Error Rate of BPSK was lesser than QPSK and QAM. Performance of BPSK is much higher even after embedding.

Sayak Bhowal 2013 proposed a low-power CSA module of the Viterbi decoder. In this design, it was assigned that the designer already knew the expected codeword and hence minimized the logic of branch metric generation. Power dissipation is reduced nearly 10% for each approaches whereas the total area of the circuit is increased.

Bineeta Soreng et al 2013 implemented convolution encoder and Viterbi decoder of code in 1/2, constraint length 7 on a stratix IV family in Altera DE board. The steps involved in the proposed approach were as follows, calculate the possible branch metric, load the branch metric, perform ACS, and store the path information. If the states end, again repeat from new branch metrics. If yes check if it is the end of trellis stages if the trellis stages end then output the decoding bits, these repeat from calculating the four possible branch metrics. It was found that there is an area improvement in hardware implementation.

Qolamreza Nadalinia Charei et al 2013 proposed the use of ANN to improve the efficiency of soft decision neural network is trained with 1000 input sequence with 1db SNR. In order to test the network 1000 random bits are used for 40 times. Three different cases with conventional Viterbi decoder, neural network in the decision block and in the third case, a part of the training data is also used for testing from the proposed neural network in decision block of Viterbi decoder has reduced the BER in AWGN channel.

Chu Yu et al 2013 proposed a novel dualcode rate memory less Viterbi decoder for software defined radio using a 4 level decision making. The proposed architecture consists of Reconfigurable Branch Metric Unit (RBMU), a Path Metric Memory (PMM), an Add-Compare-Select Unit (ACSU), a Path Selection Unit (PSU), and a Path Tracer Unit (PTU). In contrast to the conventional hardware, the Survivor Memory Unit (SMU) is eliminated. the proposed architecture is capable of proving both rate-1/2 or rate-1/3 decoding and identifying the probable survivor path individually and provides the output bit stream directly also it consumes less power, less area then the conventional hardware design.

Suganya et al 2013 proposed an efficient logic design for a cryptosystem that involves convolutional encoder and adaptive Viterbi decoder. The Viterbi decoder consists of a BMU, Path metric unit (PMU) and Trace Back Unit (TBU). Hamming distance or the Euclidean distance is used for determining the branch metrics. The ACS unit in PMU adds the corresponding states path metric to determine to new path metrics a decision bit is generated based on the path with the better metrics. The decision bits are then used to calculate the decoder output in this approach trellis diagram is realized with permutation network based path history unit to back trace the survivor path connection between two adjacent stages determined based on the decision bit of the ACS unit.

Pooran Singh et al 2013 integrated virtex7 and Spartan6 FPGA on a single IC to create a High-speed lowpower Viterbi encoder and decoder with little hardware area. Here it is assumed that parallel successive code symbols are sent to a Viterbi decoder from which the boundaries and frames can be identified. Here absolute difference used for determining the Branch Metrics (BM) and State Metrics (SM) are obtained by adding the BM with the previous SM, a dual port memory is used not only to generate but also to rectify the errors.

Khmaies Ouahada et al 2014 discussed distance preserving mapping convolutional codes and implemented conventional convolutional codes in Galois fields of order higher than two performances of these codes combined with a multiple frequency shift keying modulation scheme to correct narrowband interface in power line communications channel. Demodulators were modified to refine the selection and the detection. Gain was found to be improved for specific values of the modified detectors. It was also observed that the proposed code works better than conventional codes.

III. PROPOSED WORK

In order to design a Viterbi decoder with BPN it is first necessary to determine the architecture of BPN. In this work, a five layered BPN is designed with an input layer, three hidden layers, and one output layer. The number of neurons in the hidden layer is 20,10,5 respectively. Here the number of message bits is equal to 3, number of code bit is equal to 10. A Viterbi decoder receives 10 bit code and predicts the message bits. The activation functions are tansigmoidal for hidden layers and pure linear for output layer. Both the learning and momentum parameters are fixed as .1. Totally 80 exemplars were generated where 10 exemplars are noise less and the remaining exemplars with 1bit errors. The BPN is trained and tested with two different sets of exemplars (40 each). Convolutional code are generated with three stages and two outputs V1 and V2 where $V1 = m \oplus m1 \oplus m2$ a set of 10. Exemplars are shown in table1. Performance of the proposed technique is measured in terms of accuracy of the decoded message bits.

TABLE 1
Convolutional code and the corresponding message bits (One bit error)

S.No.	Convolutional code										Output codes		
1	0	0	0	0	0	0	0	0	1	0	0	0	0
2	1	1	1	0	1	1	0	0	1	0	0	0	1
3	0	0	1	1	1	0	1	1	1	0	0	1	0
4	1	1	0	1	0	1	1	1	1	0	0	1	1
5	0	0	0	0	1	1	1	0	0	1	1	0	0
6	1	1	1	0	0	0	1	0	0	1	1	0	1
7	0	0	1	1	0	1	0	1	0	1	1	1	0
8	1	1	0	1	1	0	0	1	0	1	1	1	1

In the Table 1, the last three rows designate the input message bits that are to be detected by Viterbi decoder. The inputs are the convolutionally coded message bits. These bits are obtained from the convolutional coder with xor gates.

IV. RESULTS AND DISCUSSION

After training the Back propagation Network, it is tested with a new set of data. The relationship between the actual and desired output is shown in Table 2. A total of 40 exemplars are used for testing in which each code has been given 5 inputs. The accuracy for the detection of the codes is also shown in Figure 1. The average accuracy for decoding of one bit error Viterbi decoder using BPN is 55%.below.

Table II
Accuracy of the proposed Viterbi decode

S.No.	Expected Code	Accuracy%
1	000	60
2	001	80
3	010	40
4	011	20
5	100	60
6	101	40
7	110	80
8	111	80

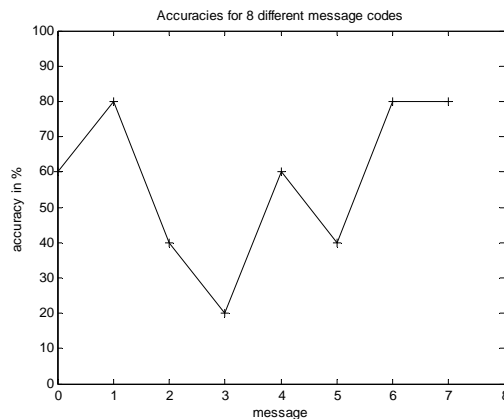


Fig. I. Accuracy of the proposed technique

V. CONCLUSION

In this paper, BPN has been successfully used for realizing a Viterbi decoder. It predicts the 3-Bit message from the 10 bit convolutional codes. The proposed network works well in robust environment, where the noise changes a bit in the convolutional code. Accuracy of the proposed decoder is 55%. However 2 bit and 3 bit errors are yet to be tested in the proposed BPN based Viterbi decoder. Also in order to reduce the area, the number of hidden layers and the number of neurons in each layer are to be reduced. Also the proposed BPN based Viterbi decoder is to be implemented in VLSI.

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