High Speed and Efficient 4-Tap FIR Filter Design Using Modified ETA and Multipliers

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Abstract—The FIR filter is a fundamental processing element in many Digital Signal Processing (DSP) systems. FIR filters are used in DSP applications ranging from image and video processing to wireless communication. Arithmetic circuits like adders and multipliers are basic building blocks of FIR filter. Digital systems are prone to errors and these are inevitable. The scheme of Error Tolerance (ET) states that some digital systems accept certain amount of errors and they are more efficient. The scheme of ET can be incorporated in DSP systems which accept that ET circuits can be used for applications in image, speech and video processing. As more devices becomes embedded or battery dependent, power consumption plays a vital role. Multipliers are the core of FIR filters; they consume a lot of energy and are generally complex circuits. This paper presents the implementation of 4-tap FIR filter using combination of conventional adder and Modified Error Tolerant Adder (META) with two different multiplier structures namely parallel array and Modified Wallace Tree Multiplier (MWTM). The highest sampling frequency achieved for the FIR filter is 505.05MHz by using combination of MWTM and META with lowest power consumption of 0.312mW. The design is implemented using Cadence® Virtuoso gpdk045nm CMOS technology. The implemented FIR filter is useful in various domains of DSP system such as audio, video, speech and image processing.

Keyword-45nm Technology Library, Conventional Adders, High speed DSP, META, MWTM, 4-Tap FIR filter.

I. INTRODUCTION

The techniques of DSP systems are extensively used in numerous applications such as multimedia and communication. Recent trends in communication and mobile computing demand high speed and ultra low power DSP systems. Digital filters are useful structures for DSP applications and in signal analysis and estimation [1]. The band selection, signal preconditioning and low/high pass filtering are typical filter applications. Finite Impulse Response (FIR) and Infinite Impulse Response (IIR) are two types of digital filters.FIR filter have advantages over IIR filter due to linear phase response and stability [2]. Also the FIR filters are non-recursive. Digital filters are widely used for computation and communication. For this computation, different types of adders and multipliers are used. Also the digital systems are less sensitive to variation in temperature, ageing, component values and other external parameters. Some digital circuits and systems tolerate certain amount of error excluding feedback control systems. Hence the scheme of ET has been proposed based on concepts and characteristics of VLSI design [3-7]. A circuit is called Error Tolerant when it produces accurate and acceptable results even when it contains defects that may cause internal or external errors [8]. The scheme of ET can be incorporated in such systems to reduce the power consumption and to operate at higher frequencies. The FIR filter may operate at high sampling rate for one application and for other application at moderate sampling rate with low power. In the field of wireless communication Software Defined Radio (SDR) is used to replace analog computation by DSP systems [9]. The channelizer is computationally main block of SDR receiver which must be realizing of low power and operate at high sampling rate. Hence the multiplier and adders used for the design of FIR filter must be fast enough and efficient.

The structure of 4-tap FIR filter includes adders, multipliers and D flip flops. This paper presents the design of 4-tap FIR filter using parallel array and modified Wallace tree multiplier. Two different types of adders are used for summation namely Ripple Carry Adder (RCA) and modified ETA. The results of these combinations are compared in terms of power, delay and number of transistors. The modified ETA is logical and structural modification in ETA.

Here, Section II describes the basic terms of ETA, addition arithmetic and dividing strategy. Section III describes the hardware implementation and the design of ETA. Structural implementation of modified

ETA is proposed in section IV. The conventional array and modified Wallace tree multiplier are described in section V and VI respectively. The architecture of 4-tap FIR filter and its implementation is described in section VII. The FIR filter is implemented in cadence® EDA tool using 45nm CMOS technology. The simulation results and comparison are mentioned in section VIII. Finally, section IX provides conclusion.

II. ETA BASICS, ADDITION ARITHMETIC AND DIVIDING STRATEGY

For the huge data processing and the instant response, high speed adders are required. The conventional adders have the simplest architecture but the speed of operation is limited due to carry propagation from Least Significant Bit (LSB) to Most Significant Bit (MSB). Hence there is always a trade-off between power consumption and speed of operation. To overcome this trade-off special adder such as ETA is required. ETA tolerates certain amount of errors by compromising some amount of accuracy to reduce power consumption and to enhance speed of operation. Some basic terminologies related to ETA are given as follows [8].

1) *Overall Error (OE):* | *Rc - Re* |, where *Rc* denotes the correct results obtained from addition arithmetic. *Re* denotes the result obtained by adder (all results are represented in decimal).
2) *Accuracy (ACC):* It indicates the accurate results of adder output for given input pattern. It is calculated as: *(1-OE/Rc) * 100%.*
3) *Minimum Acceptable Accuracy (MAA):* It is the accuracy higher than a threshold value of the acceptable output to fulfill the requirement of the whole system though the errors are allowed. Threshold value is nothing but the *MAA.* Acceptable results should be more than *MAA.*
4) *Acceptance Probability (AP):* Acceptance probability ranges from 0 to 1 should be higher than minimum acceptable accuracy *AP=P (ACC > MAA).*

The delay is mainly associated with the carry propagation from LSB to MSB of the conventional adders. The carry propagation in the critical path may cause glitches, due to which significant amount of power dissipates. Hence the carry propagation can be eliminated not only to limit the power consumption but also to increase the speed of operation. For this purpose the novel addition arithmetic for 16-bit input operands is illustrated in Fig. 1.

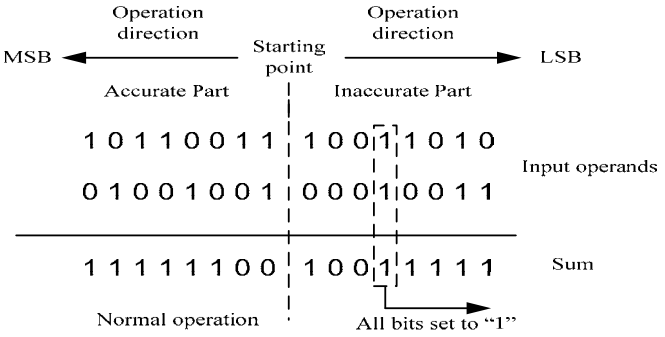

Fig. 1. Addition arithmetic of ETA

Here the bits of input operand are split into two parts as accurate part and inaccurate part. The accurate part consists of higher order MSB bits and the inaccurate part consists of lower order LSB bits of operands. The addition arithmetic starts from middle towards the opposite direction where partition is done. As the higher order bits play significant role in digital system the normal addition arithmetic is applied from the LSB to MSB for the accurate part. The two operands X= "1011001110011010" (45978) and Y="0100100100010011" (18707) are divided equally into 8-bits as inaccurate and accurate part. The rules of the addition arithmetic for the accurate and inaccurate part are as follows

1. For the accurate part the normal addition arithmetic is applied from LSB to MSB to maintain correctness.
2. For the inaccurate part useful addition arithmetic is applied from MSB to LSB i.e. carry propagation is eliminated. a) When both the bits are '0' or different, the normal addition is applied for one bit. b) When both the bits are '1' then addition stops and output from that bit onward towards right i.e. toward LSB set to '1'.

The addition operation can be easily understood from the Fig. 1. The correct output of final result is "1111110010101101" (64685) and the output produced from above described addition arithmetic is "1111110010011111" (64671).Hence the overall error produced can be computed as follows:

Overall Error (OE) = 64685 – 64671 = 14.

The accuracy of the adder is:

Accuracy (ACC) = (1-(14/64685)) x 100%=99.98%.

Hence the overall delay and power consumption can be greatly reduced by elimination of carry propagation. The accuracy of adder depends on the input pattern. Larger the number of bits, greater will be the accuracy. The relation between the number of bits of adder and acceptance probability can be easily derived and stated by equation as follows:

$$P\left(ACC = 100\%\right) = \frac{4^{(N_t - N_l)} * 3^{N_t} + 2^{(N_t - N_l)}}{4^{N_t} + 2^{N_t}} \quad (1)$$

Where, N_t : Total number input of bits i.e. the size of the adder

N_l : The number of bits in the inaccurate part.

It can be concluded that lowering the minimum acceptable accuracy, acceptance probability increases for the adders. Here the number bits in inaccurate part should be greater than the bits in accurate part since LSB bits have lower weight. When the input pattern is large, this method of calculation used in ETA is efficient for reducing power consumption.

While dividing the number of bits in accurate and inaccurate part the strategy should be such that the delay of accurate and inaccurate part should nearly be equal for achieving optimal delay. Let the delay of accurate part be T_A and the delay of inaccurate part be T_B .The overall delay can be computed as follows:

$$\text{Overall Delay} = \text{Max}\ (T_A, T_B)$$

When the requirements of minimum acceptable accuracy and acceptance probability are not met ,then shift one bit from inaccurate part to accurate part to achieve designers requirement.

III. HARDWARE IMPLEMENTATION AND DESIGN OF ETA

The hardware implementation of 16-bit ETA and its block diagram is shown in Fig. 2. The ETA consists of two parts namely accurate and inaccurate .The conventional adders like RCA, Carry Select Adder [10], Carry Look Ahead Adder [11], Carry Skip Adder [12] etc. can be used for the design of accurate part. The inaccurate part consists of control block and carry free addition block.

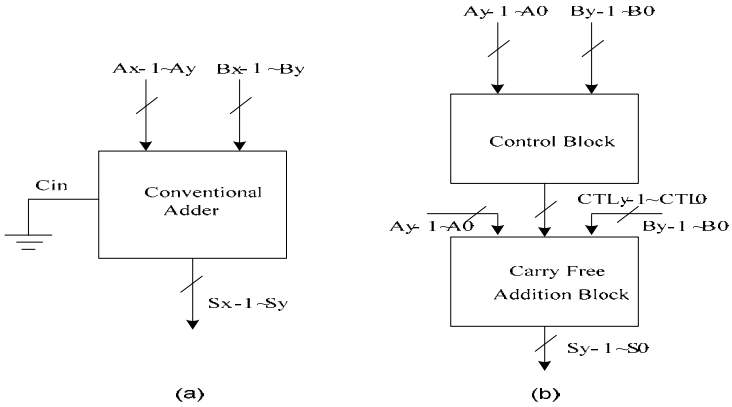

Fig. 2. Hardware implementation of ETA (a) accurate part (b) Inaccurate part

Here the 16-bits are divided into 8-bits as accurate part and inaccurate part respectively. For the design of accurate part simple RCA can be used to reduce the power consumption. Block diagram of 8-bit RCA is shown in Fig. 3.

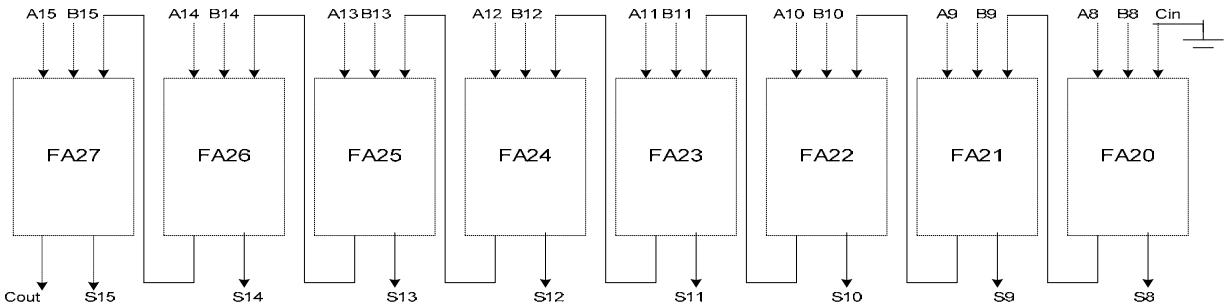

Fig. 3. Accurate part of ETA (8-Bit RCA)

The inaccurate part plays vital role in determining power consumption, accuracy and the speed performance of the 16-bit ETA. It mainly consists of two blocks, the control block and the carry free addition block. The control

block comprises of 8 Control Signal Generating Cells (CSGC) used for generating control signals. The 8 cascaded CSGC are divided into 2 blocks as shown in Fig. 4. Each CSGC generates control signal which is given as input to modified XOR gate. There are two types of control signal generating cells (CSGC) namely CSGC-I and CSGC-II whose schematic is shown in Fig. 5. The CSGC generates control signal when both input bit positions are '1' and passes this signal from same position to rightmost position of that bit and sets all output sum bits to '1'. The control signal generated by left most CSGC in each block is given to left most CSGC of next block so as to minimize the critical path.

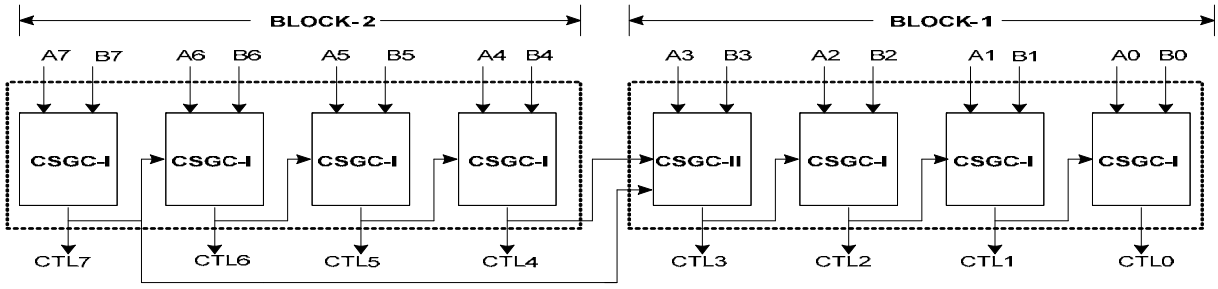

Fig. 4. Block diagram of control block

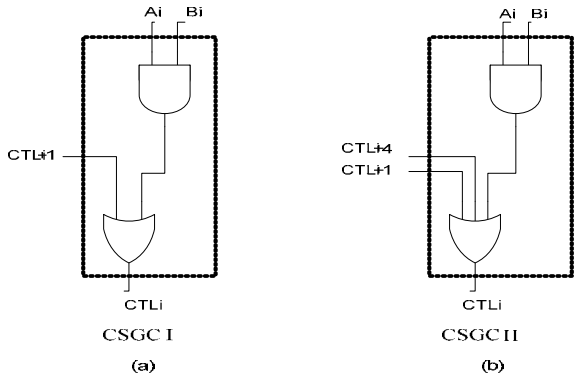

Fig. 5. Control Signal Generating Cells (a) CSGC I (b) CSGC II [1]

The carry free addition block consists of 8 modified XOR logic blocks which is shown in Fig. 6. The input to carry free addition block is control signal generated from CSGC cell for the respective input bit positions. The same input bits are fed as input to CSGC cells and modified XOR gate. The schematic of modified XOR gate is shown in Fig. 7 which is different from normal XOR logic. Here the two PMOS transistors P1, P2 and an NMOS transistor N1 are used for deciding the mode of operation of the circuit. The control signal CTL coming from respective bit position of CSGC cell as shown in Fig. 4 is given as input respective modified XOR gate. The control signal CTL given as input to transistor P1 and its inverted output from inverter is given to transistor N1 and transistor P2 as shown in Fig. 7. The circuit has two modes of operation when control signal is either low or high. When CTL=0 the transistors P1 and N1 both are ON and P2 if OFF. In this mode circuit operates in normal mode of operation as XOR logic does giving the SUM output. When CTL=1 the two transistors P1 and N1 are turned OFF and P2 transistor is turned ON pulling the SUM output to VDD hence the output SUM is set to "1".

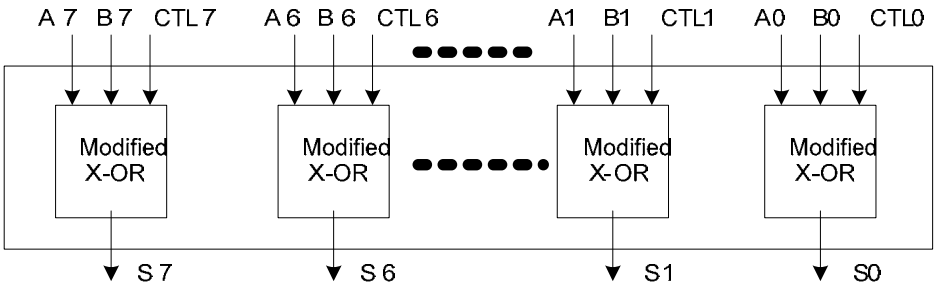

Fig. 6. Architecture of carry free addition block

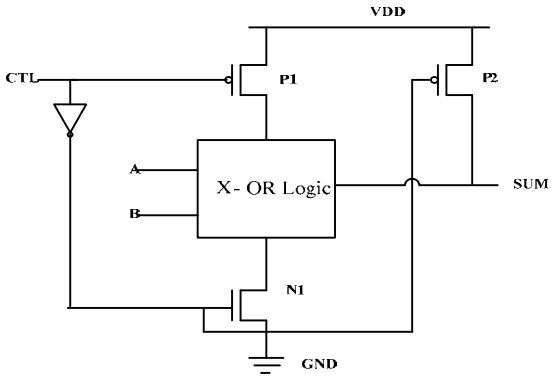

Fig. 7. Schematic of modified XOR gate [1]

IV. MODIFIED ETA

The inaccurate part is very important for deciding the power dissipation and speed performance of ETA. The modified structure of ETA is shown in Fig. 8. The modified XOR gate used for carry free addition block is eliminated and replaced by simple OR logic thereby, reducing the hardware complexity. The modified ETA consists of 8 cells for producing sum output. It mainly consist of AND-OR logic used for generating present control signal CTL_i for the input bit positions A_i and B_i . This AND-OR logic follows OR logic producing the sum output. There are 2 blocks each consisting of 4 cells for generating sum output. Let us see the operation of modified ETA, assume the bit positions of *A7 A6 A5 A4* be "0101" and that of *B7 B6 B5 B4* be "1011".The bit *A7* and *B7* produce the control signal *CTL7=0* and SUM *S7=1* likewise, it does the operation and produces the SUM outputs *S6=1*,*S5=1*. Here the control signals *CTL6* and *CTL5* both are zero. When the input bits *A4=1* and *B4=1*, it activates control signal i.e. *CTL4=1* producing SUM bit *S4=1* and also sets all SUM bits to "1" from that position to its right side. The control signal *CTL7* from *cell7* of block-2 is also fed to *cell3* of block-1 to reduce the worst path for the propagation of control signal. Thus, modified ETA reduces the hardware complexity, power consumption and propagation delay compared to ETA.

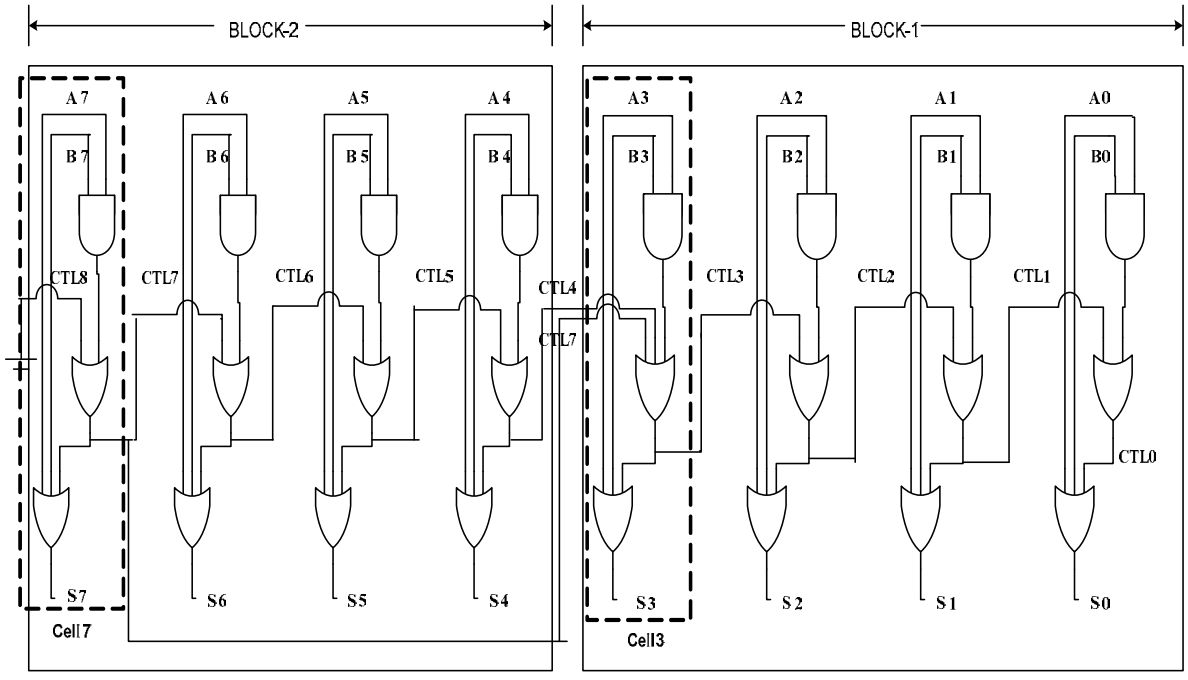

Fig. 8. Modified ETA

V. CONVENTIONAL ARRAY MULTIPLIER

The multiplier plays vital role while designing FIR filter due to its complexity. Let the multiplication of two unsigned numbers, where x= X_{n-1}, X_{n-2} … X_0 is the multiplicand and y= Y_{n-1}, Y_{n-2} …Y_0 is the multiplier [13]. The product of these two is stated using equation (2)

$$P = \sum_{i=1}^{n-1} X_i \sum_{j=1}^{n-1} Y_j 2^{(i+j)} \quad (2)$$

$$x = \sum_{i=1}^{n-1} X_i 2^i \quad (3)$$

$$y = \sum_{j=1}^{n-1} Y_j 2^j \quad (4)$$

The Fig. 9 shows 8x8 multiplications, from equation 4 which generates eight rows of partial products. The hardware required for the implementation of partial terms is AND gate. These partial terms can be added using CSA and Carry Propagate Adder. In this addition method first row of partial terms can be added using half or full adder. When the two input data are present, the third input C_{in} is considered as zero in full adder. The architecture of single full adder is shown in Fig. 10.The carries are forwarded diagonally to the next row of adder. The sums and carries in the final stage are merged using fast carry propagate adder like RCA or CSA. The architecture of conventional array multiplier is shown in Fig. 11.

Fig. 9. Bit level multiplication 8x8

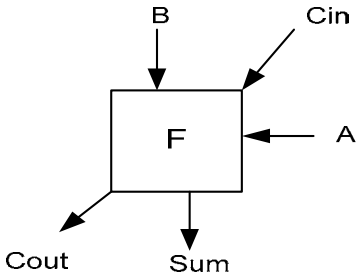

Fig. 10. Architecture of full adder

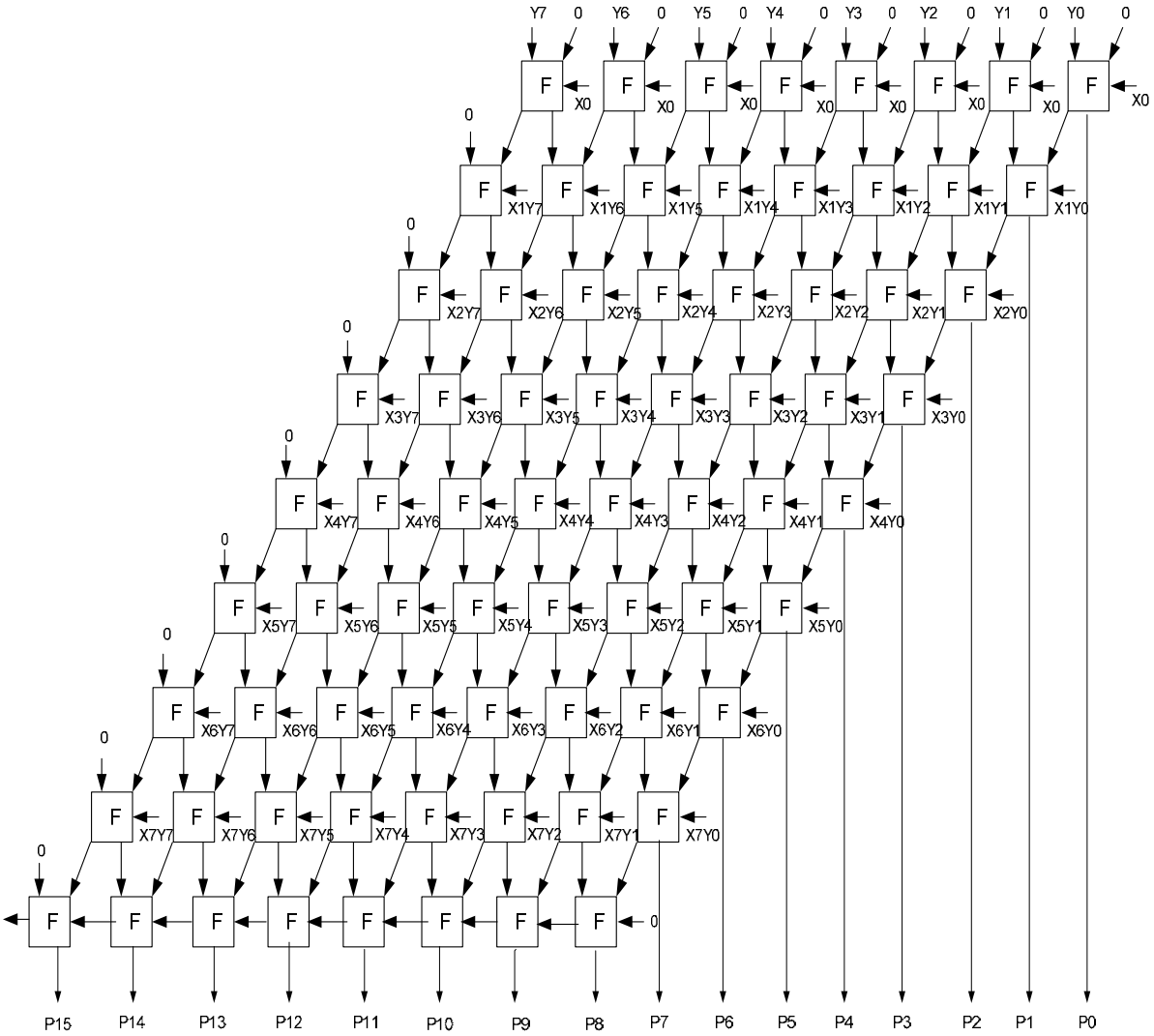

Fig. 11. Conventional 8x8 array multiplier architecture

VI. MODIFIED WALLACE TREE MULTIPLIER

The efficient 8x8 modified Wallace tree multiplier is implemented using Wallace tree logic and using the compressor for fast addition and to reduce hardware complexity, propagation delay than conventional Wallace tree multiplier. The Fig. 12 shows the 8x8 multiplication of operands with their partial product terms.

AND gates are used for the generation of 64 different partial product terms. These partial product terms are added using the full adder. The eight rows of partial product terms are divided into two groups which contain four adjacent rows. These are grouped as group 1 and group 2 in stage A as shown in Fig. 12. The partial product terms are added depending on number of partial terms available for addition in group 1 and group 2. The half adder, full adder and 4:2 compressors are used depending on number of bits available for addition. The generated partial sums and carries are divided and added in same manner in second level stage B. The final product will arrive in third level stage C only after the generated terms in the second level stage are added. The Fig. 13 shows 4:2 compressor implementation using two full adders [14]. The modified Wallace tree multiplier has less hardware complexity, power consumption and propagation delay for the worst case input pattern.

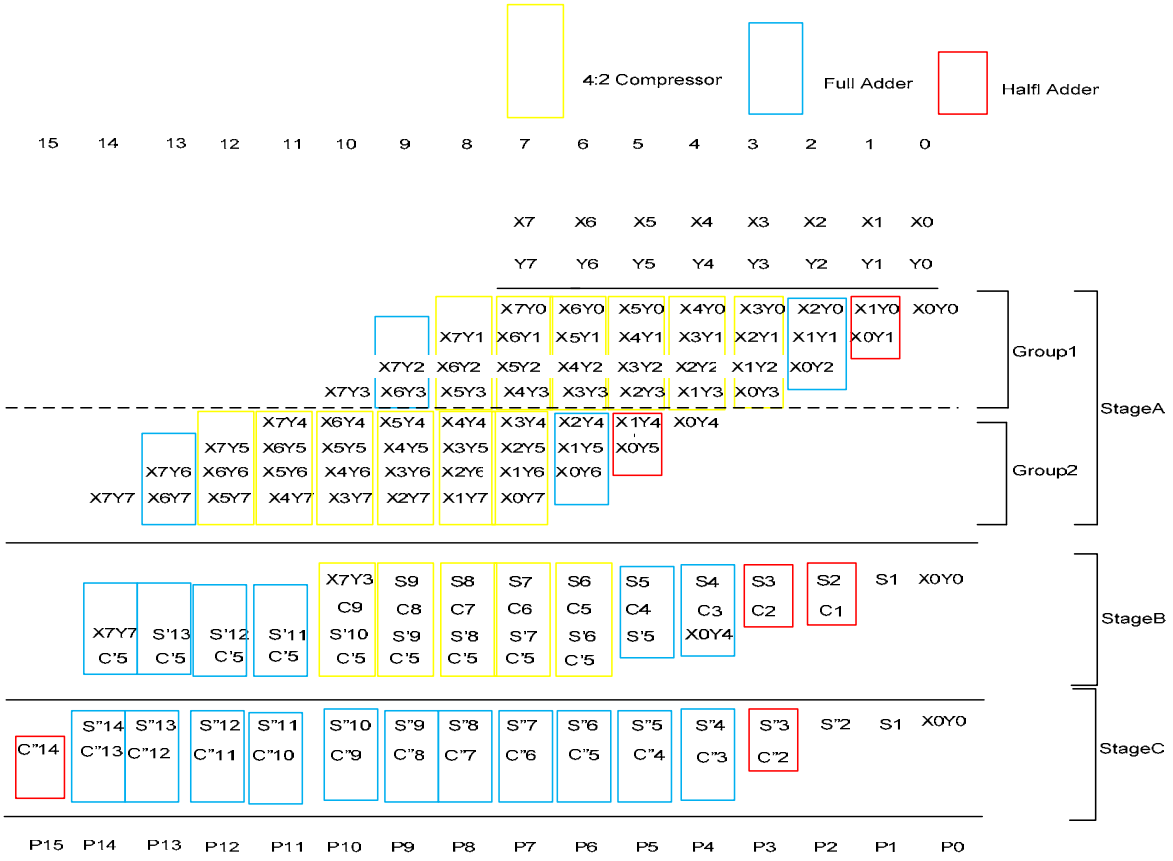

Fig. 12. 8x8 Modified Wallace tree multiplier

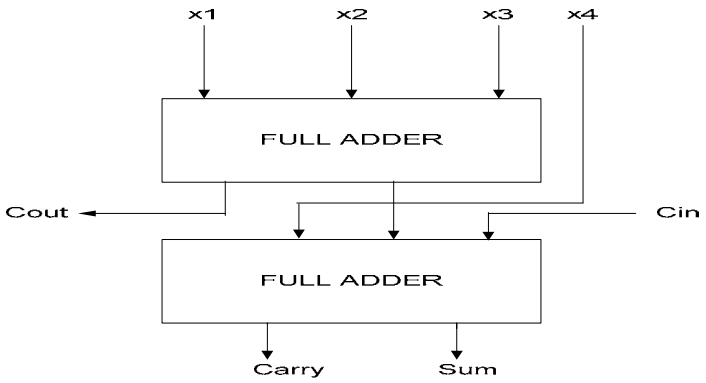

Fig. 13. 4:2 Compressor using full adder [13]

VII. FIR FILTER

The numbers of coefficients generated for the designing of FIR filter determine the order of the filter. If the order of the filter is N, then N+1 coefficient terms are required [15]. Depending on rate at which the number of input samples can be processed, the speed of FIR filter can be defined. To increase the speed of FIR filter the critical path has to be reduced from input to output .The sampling period T_{sample} of FIR filter can be stated by using equation (5).

$$T_{sample} \geq T_m + (N-1)T_a \tag{5}$$

Hence the sampling frequency f_{sample} is stated using equation (6)

$$f_{sample} \leq \frac{1}{T_m + (N-1)T_a} \tag{6}$$

For the low pass 4-tap FIR filter using data broadcast form the sampling period is T_m + 3Ta and for the transposed structure T_m + T_a. The architecture of data broadcast and transposed structure for 4-tap FIR filter is shown in Fig. 14 and Fig. 15 respectively.

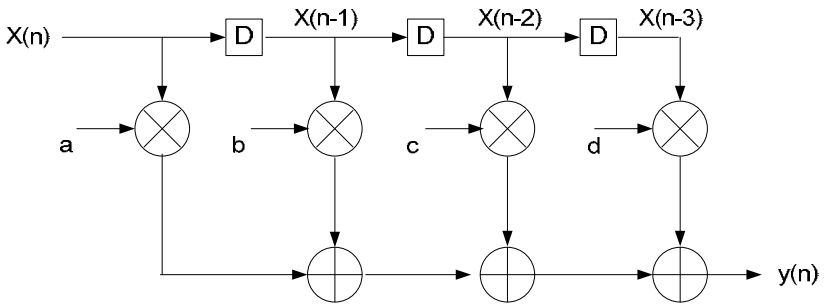

Fig. 14. 4-tap data broadcast FIR filter

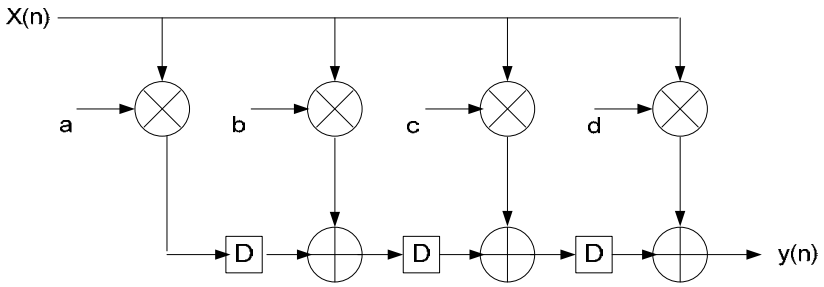

Fig. 15. 4-tap transposed FIR filter

The FIR filter is implemented using multipliers, D flip flops and adders. The schematic of FIR filter using Cadence EDA tool is shown in Fig. 16.

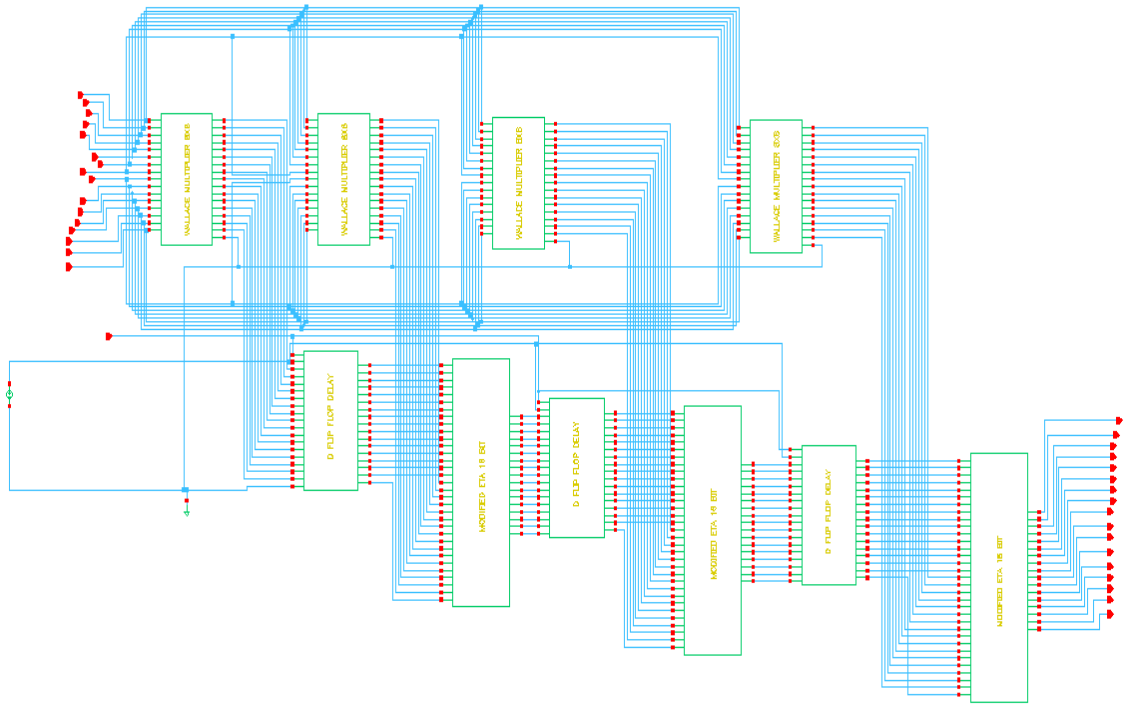

Fig. 16. Schematic of 4-tap FIR filter

VIII.RESULTS AND DISCUSSION

The 4-tap FIR filter is implemented using D flip flops, adders and multipliers. The different combinations of adders and multipliers are used for the design of filter. The input data and multiplier coefficients are used as 8-bit unsigned representation. The acceptance probability of the modified ETA is more than 96% for the sum generated at the output of FIR filter using different data input patterns and multiplier coefficients calculated using equation (1). The combination of META and MWTM gives very less power consumption, delay and transistor count compared to other combinations. Table I shows the comparison of these combinations with respect to power consumption, propagation delay and transistor count.

TABLE I. Comparison of 4-tap FIR filter combinations with power, delay and transistor count.

Combination type	Power consumption (mW)	Propagation delay (ns)	Transistor count
4-tap FIR filter using array multiplier and full adder	0.561	3.58	11136
4-tap FIR filter using array multiplier and modified ETA	0.483	3.11	10453
4-tap FIR filter using modified Wallace tree multiplier and full adder	0.405	2.52	8923
4-tap FIR filter using modified Wallace tree multiplier and modified ETA	0.312	1.98	8240

The Frequency Analysis and Design (FDA) tool from MATLAB is used for generating filter coefficients and analyzing the filter characteristics. The 4-tap low pass FIR filter is designed for the pass band frequency of 0 to 20MHz and stop band frequency range of 21MHz to 25.25MHz. In the pass band region the ripples have the magnitude of 4dB while in stop band it is -40.3dB.

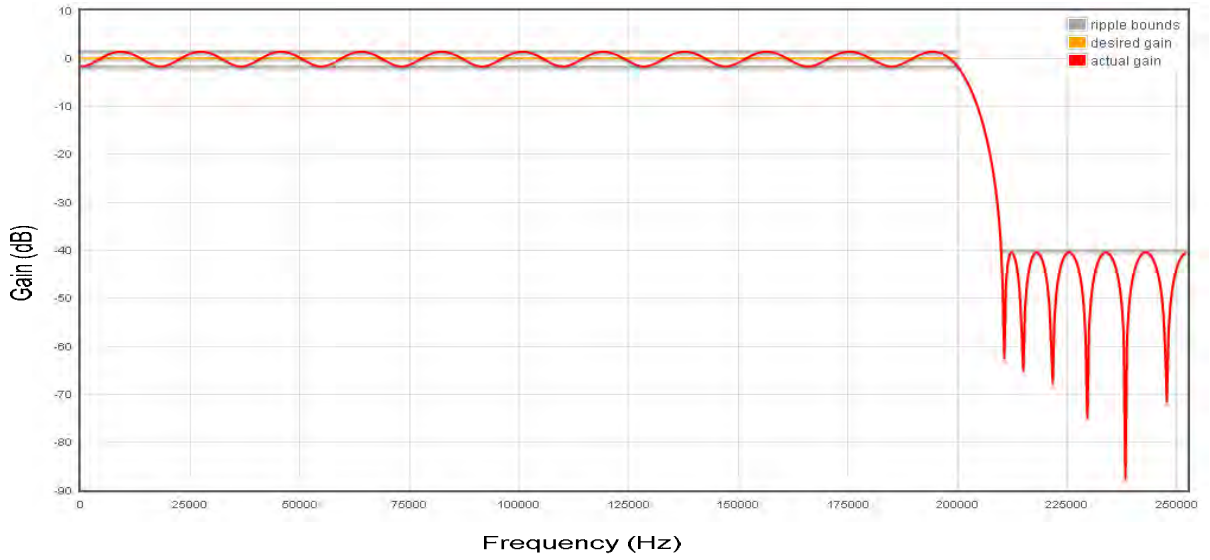

Fig. 17. Magnitude responses of FIR filter

The highest sampling frequency of the filter is 505.05MHz for the combination of META and MWTM. The magnitude response of the ripples in pass band and stop band are shown in Fig. 17.The Fig. 18 shows the comparison of power consumption of all combinations. The combination of META and MWTM has 44.38% power less than the combination of RCA and array multiplier.

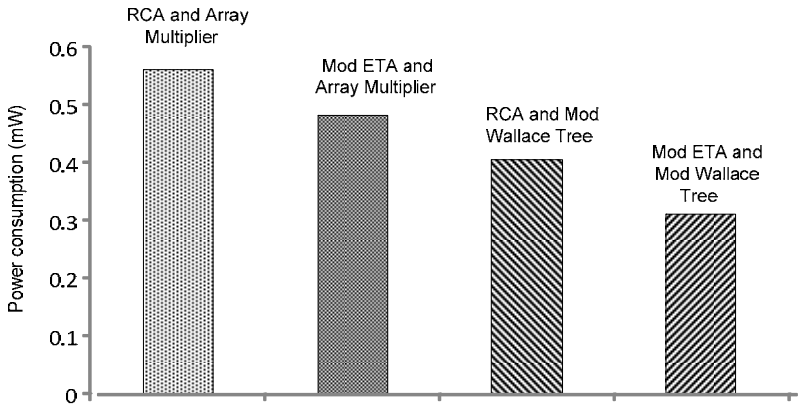

Fig. 18. Power consumption graph

The minimum propagation delay which helps in increasing sampling frequency is 1.98ns in the case of FIR filter using META and MWTM. Hence the maximum sampling frequency achieved for the design is 505.05MHz. The Fig. 19 shows the comparison of propagation delay of all the combinations.

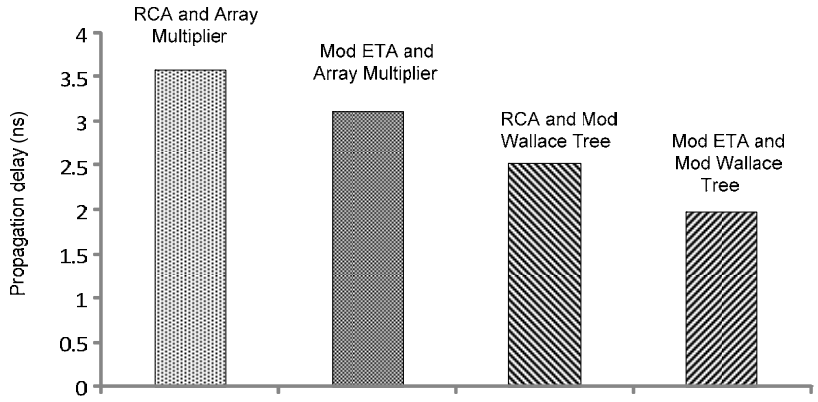

Fig. 19. Propagation delay graph

The transistor count has been reduced numerously due to reducing hardware complexity for MWTM and META. The comparison of transistor count for all combinations is shown in Fig. 20.

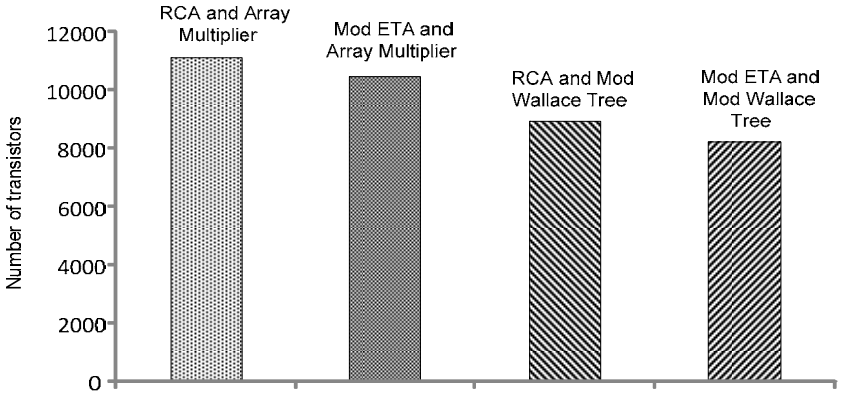

Fig. 20. Number of transistors graph

IX.CONCLUSION

The 4-tap high speed FIR filter based on concept of Error Tolerance application is designed. The design runs at maximum sampling frequency of 505.05MHz and the lowest power consumption of 0.312mW. The two different combinations of adders and multipliers are used for the implementation of 4-tap low pass FIR filter. The combination of MWTM and META gives the better speed performance and reduced power consumption out of four combinations. The designed FIR filter is used in numerous DSP applications where accuracy is not the main issue. It can be used in speech and image processing fields as well, to increase battery life performance in the portable devices such as Laptop, smart-phones etc. The bottom-up design flow gives good idea of IC design implementation using Cadence® Design System tool. The design of N-tap FIR filter implementation is not possible using bottom-up design flow. For the implementation of N-tap FIR filter the top-down design methodology is used with optimized algorithm.

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