

# A Comparative analysis of three level VSC based multi-pulse STATCOM

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**Abstract - This paper presents a comparative analysis among different models of three level NPC (Neutral point clamped) VSC (Voltage source converter) based STATCOMs. Here separate models of 12-pulse, 24-pulse, 36-pulse, 48-pulse VSC based STATCOMs are configured in MATLAB environment. These individual models are synthesized using appropriate number of three level converters which are switched at fundamental frequency and their gate pulse pattern are properly phase shifted to get desired number of pulses. The simulation results of each individual model are analyzed in three different modes: inductive, capacitive and floating mode. Harmonic content of the proposed higher pulse models are limited as per IEEE 519 standards.**

**Keywords-** Three level NPC converter, multi pulse VSC based STATCOM, 36-pulse STATCOM, Fundamental frequency modulation.

## I. INTRODUCTION

Due to lack of electrical storage facility in AC power system; generation and load must match always. Self-regulating nature of the system may meet the unbalance up to a small extent but most of the times it fails to do so, which leads to significant change in system voltage and frequency and ultimately a system collapses. This issue can be resolved by the FACTS devices whose basic aim is to control system impedance or phase angle or injection of appropriate voltage in line. STATCOM is a shunt controller which injects a controllable current in phase quadrature (leading or lagging) with line voltage thereby delivering or consuming the reactive power. It is based on voltage sourced converter whose output voltage can be changed according to the system requirement [1]. For control of reactive as well as active power energy storage devices (large DC capacitor, battery, flywheel etc.) are required to be integrated with the VSC.

The design of VSC can be accomplished in several ways. It can be modeled using the conventional three-phase bridge converter (two-level) or multi-level converter. Multi-level converter offers a wide variety of advantages over conventional converter such as lower harmonic content, reduced stress on switches and decreased switching loss [2]. Multi-level converters produce stair case type voltage wave form which is close to sinusoidal by using a number of capacitors in DC side. An 'L' level converter needs 'L-1' number of capacitors.

But these types of converters always suffer from one common limitation which is the unbalance between different capacitor voltages. This shortcoming can be overcome by variety of multi-level VSC topologies namely: - flying capacitor type, neutral point diode clamped type, cascaded multi-level converters [3]. In this paper the models synthesized are based on diode clamped three-level converter. Again a diode clamped converter can be designed with different switching strategies such as: -Pulse Width Modulation (PWM), Selective Harmonic Elimination (SHEM) and Fundamental Frequency Modulation (FFM). Several papers were documented on these switching strategies [4-6].

Multi-pulse STATCOM can be built by using several number of three-level VSC. If we observe the wave forms of phase to phase voltage and phase to neutral voltage of a conventional three phase converter, we can see both waveforms are phase shifted by 30°, amplitude of phase to phase voltage is  $\sqrt{3}$  times that of phase to neutral voltage and both waveforms contain several lower order harmonics which are in phase opposition in both the waveforms. If phase to phase voltage of one converter is added to phase to neutral voltage of another converter with the output of the converters connected to Y and  $\Delta$  secondary of two transformers (for correcting the 30° phase shift) with appropriate turns ratio (for correcting magnitude unbalance), it will result a waveform having twice the number of pulse of single converter with significant reduction of lower order dominant harmonics [1]. The phase shift pattern of the coupling transformers and gate pulse pattern of the individual converters are crucial for getting proper multi pulse waveform with less percentage THD [7-8]. There are

several papers focusing on the control architecture of STATCOM for getting better dynamic performances which contains mainly AC voltage regulator, DC voltage regulator, PLL [9-10].

In this paper a detailed explanation of three-level diode clamped VSC based STATCOM is presented. Different types of multi pulse STATCOM models:- 12-pulse STATCOM, 24-pulse STATCOM, 36-pulse STATCOM, 48-pulse STATCOM are configured in MATLAB using SIMPOWER SYSTEM tool boxes. There are already several papers on 12-pulse, 24-pulse, 48-pulse STATCOM [11-14]. One paper is also documented on 36-pulse STATCOM but using different topology [15]. In this paper 36-pulse STATCOM is configured using three-level diode clamped converter using FFM. Hence a fair comparison can be made among these four models because all are synthesized using same topology and same parameter values; except the number of converters, number of coupling transformers, phase shift pattern, gate pulse pattern which are needed to be appropriate to get desired number of pulses. This paper ultimately proposes a comparative harmonic analysis based on the simulation results of synthesized models in MATLAB using SIM POWER SYSTEM block sets.

## II. BASICS for DESIGNING MULTI-PULSE STATCOM from CONVENTIONAL VSC

STATCOM injects a variable controlled current (leading or lagging) into the system which is in phase quadrature with line voltage. Hence it supplies or consumes reactive power. If the converter is equipped with storage capacity then active as well as reactive power can be controlled.

Main building block of a STATCOM is a converter which can be VSC (voltage source converter) or current source converter. Due to economic and performance factors VSC is preferred. VSC produces AC output voltage by the sequential switching of DC voltage which is represented by a capacitor. Through proper converter topology the generated AC output voltage can be controlled in terms of its magnitude, frequency and phase angle. VSC is made of number of valves which contains a turn off device and a diode in antiparallel. The turn off device conducts when power flow from DC side to AC side representing inverter action. Diode conducts in the reverse case representing rectifier action. Due to this power reversal action we will get a square wave output voltage. To get sinusoidal voltage with reduced harmonics there are several topologies like PWM configuration, SHEM configuration, cascaded inverters, multilevel converters, etc.

For a better understanding of those advanced topologies let us consider a conventional three phase full wave VSC (two-level). It gives a six pulse output, its phase to neutral voltage and phase to phase voltages are given by equation (1) and (2) respectively [1].

$$V_{pn} = \frac{2}{\pi} V_{dc} \left[ \cos \omega t + \frac{1}{5} \cos 5\omega t - \frac{1}{7} \cos 7\omega t - \frac{1}{11} \cos 11\omega t + \frac{1}{13} \cos 13\omega t + \dots \right] \quad \text{----- (1)}$$

$$V_{pp} = \frac{2\sqrt{3}}{\pi} V_{dc} \left[ \cos \omega t - \frac{1}{5} \cos 5\omega t + \frac{1}{7} \cos 7\omega t - \frac{1}{11} \cos 11\omega t + \frac{1}{13} \cos 13\omega t + \dots \right] \quad \text{----- (2)}$$

If we will observe both the voltage wave forms we could deduce that fundamental component of  $V_{pp}$  is phase shifted by  $30^\circ$  and its magnitude is  $\sqrt{3}$  times of  $V_{pn}$  which is evident from the equations. Observation of the above two equations suggest that if we can add these two equations then 5<sup>th</sup> and 7<sup>th</sup> harmonics will be cancelled. Adding these equations practically needs use of two converters,  $V_{pp}$  of one will be added to  $V_{pn}$  of other converter. But before addition the phase shift and unequal magnitude must be corrected. For correcting the  $30^\circ$  phase shift Y/Y and  $\Delta/Y$  transformers can be used.  $V_{pp}$  of second converter connected to delta secondary of  $\Delta/Y$  transformer,  $V_{pn}$  of first converter connected to star secondary of Y/Y transformer and gate pulse pattern of two converters must be phase shifted by  $30^\circ$ . For correcting the unequal magnitude  $\Delta/Y$  transformer is given with  $\sqrt{3}$  times turns than that of the other transformer. Now the combined output voltage of both the converters (six pulses each) will be a 12-pulse voltage containing the harmonics of the order  $12n \pm 1$ , having significant harmonics as 11<sup>th</sup> and 13<sup>th</sup>. Thus a 12-pulse STATCOM can be configured as shown by fig. 1. In a similar way 24-pulse, 36-pulse, 48-pulse STATCOMs can be synthesized.

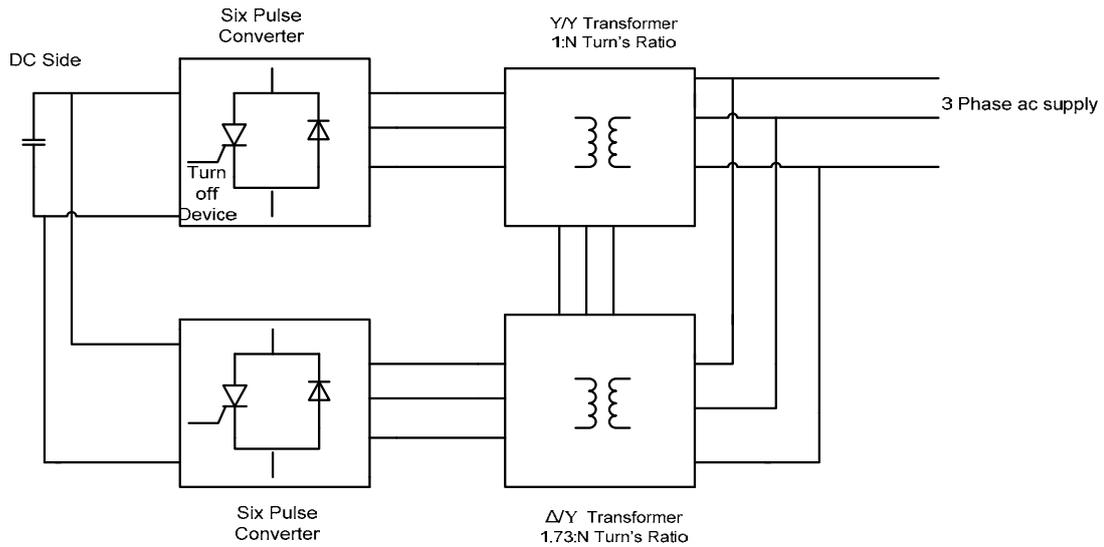


Fig.1a. Transformer connections for producing 12-Pulse output from two six pulse converters

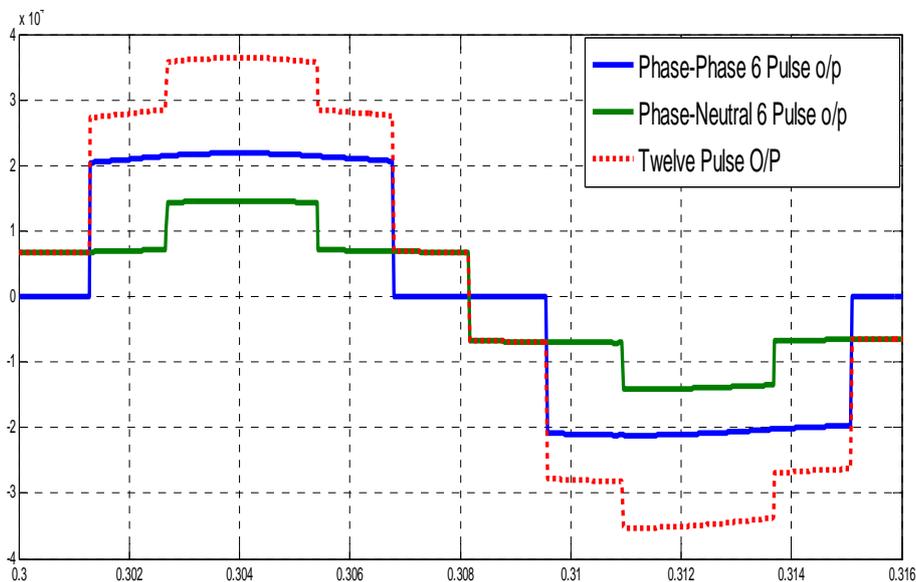


Fig.1b. Twelve Pulse waveform from two 6-pulse o/p

### III. THREE-LEVEL NPC BASED VSC

It is desirable to control the ac output voltage of STATCOM for controlling the line voltage, reactive power flow, current injection etc. One common way to vary the output voltage is to vary the magnitude of DC capacitor voltage. But it is advantageous to vary output voltage without changing DC input voltage which can be accomplished by multilevel converters. The problem with these multilevel converters is voltage unbalance of different DC capacitor levels. This issue can be resolved by three ways: - diode clamp, flying capacitor, cascaded inverter [3]. The models simulated here are the diode clamp three-level VSC which is shown in fig. 2a.

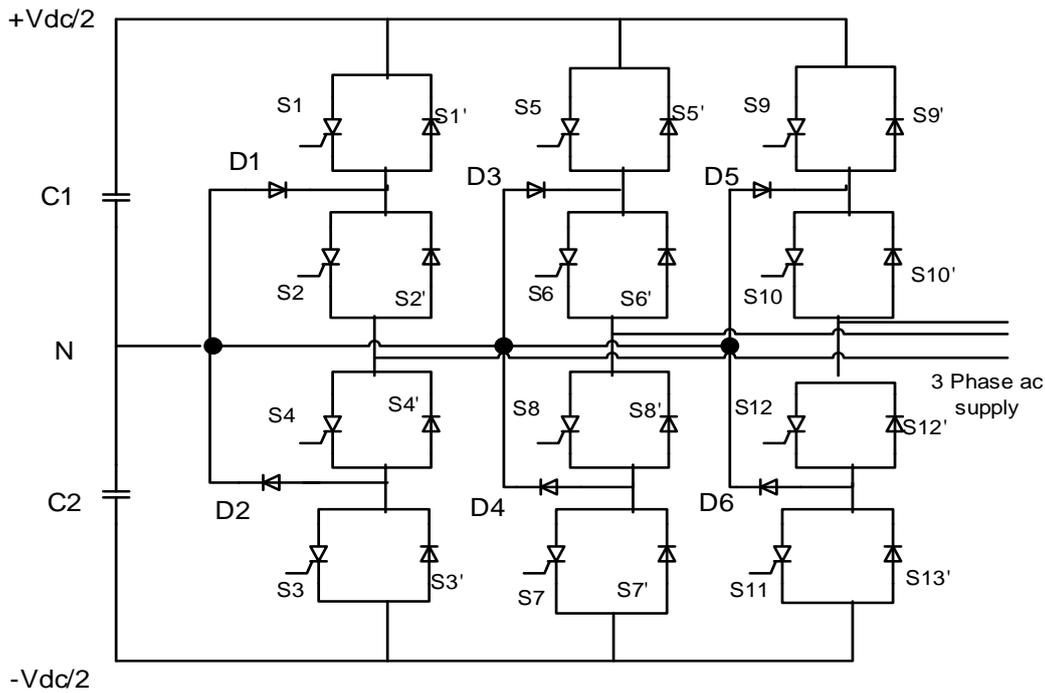


Fig.2a. Circuit Diagram of Diode clamped Three-level VSC

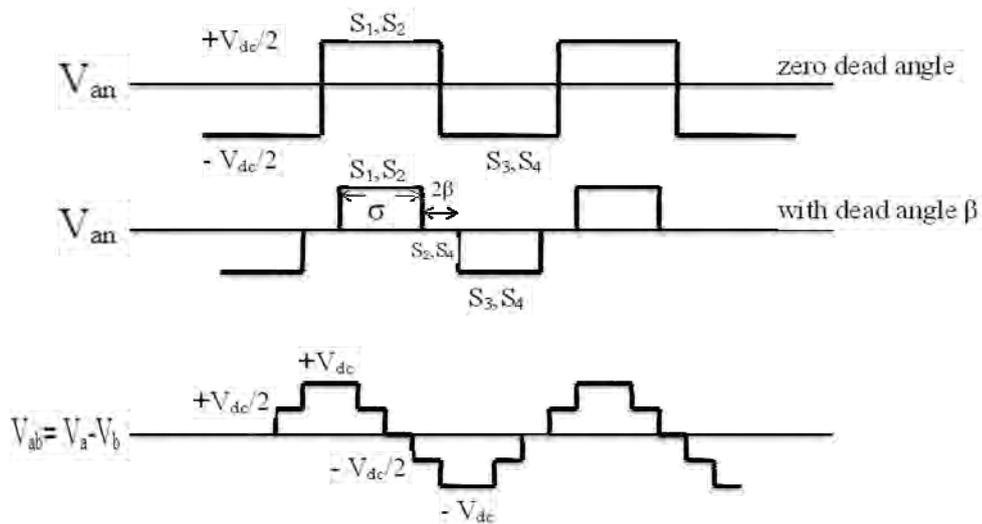


Fig.2b. Output waveform of three-level VSC

For a ‘L’ level diode clamped converter, ‘L-1’ number of capacitors,  $2 \times (L-1)$  number of valves per phase are required. Midpoint of valves connected by diodes is known as clamping diodes. It can be observed here that voltage across each capacitor is  $V_{dc}/(L-1)$  (for three-level converter  $V_{dc}/2$ ) and each device voltage stress will be restricted to  $V_{dc}/(L-1)$  by clamping diodes. In this three-level converter the three levels of a phase to neutral voltage ( $V_{an}, V_{bn}, V_{cn}$ ) are zero,  $V_{dc}/2, -V_{dc}/2$ .

- a) To get  $V_{an} = V_{dc}/2$ , upper switches S1,S2 are ON
- b) To get  $V_{an} = -V_{dc}/2$ , lower switches S3,S4 are ON
- c) To get  $V_{an} = 0$ , middle two switches S2,S3 are ON along with the clamping diodes D1,D2.

The angle during which voltage is clamped to zero is known as dead angle ( $\beta$ ) which is variable. By varying this dead angle, conduction angle ( $\sigma = 180 - 2\beta$ ) can be varied which can in turn vary  $V_{an}$  as shown in fig. 2b. Thus a three-level converter could vary AC output voltage without changing DC capacitor voltage. In a similar analysis we can get ‘b’ and ‘c’ phase voltages with  $120^\circ$  and  $240^\circ$  phase shifted waveforms. Subtracting  $V_{bn}$  from  $V_{an}$  we can get the line voltage consisting of  $(2L-1)$  level waveform (5-levels for present case) which is a  $2 \times (2L)$  pulse (12-pulse for present case) waveform. For a three-phase system relation between number of levels

L and number of pulses P can be represented by  $P=6 \times (L-1)$ . As explained for conventional 3-phase bridge converter this three-level converter can be connected properly to give 24-pulse, 36-pulse, and 48-pulse outputs.

**IV. CONFIGURATION of 12-PULSE, 24-PULSE, 36-PULSE, 48-PULSE MODELS**

So, one three-level converter yields 12-pulse output. For 24-pulse, 36-pulse, 48-pulse the number of three-level converters required are 2, 3, and 4 respectively. For a three-level VSC of P-number of pulses, phase shift between each converter group is  $\frac{360^0}{P/2}$  [16]. For a 24-pulse converter the phase shift between the 2 converters will be 30°. For 36-pulse converter and 48-pulse converter, it will be 20° and 15° respectively.

Next the phase shifting transformers must be properly chosen for each model to create the required amount of phase shift. For 24-pulse STATCOM, two transformers one Y/Y with a phase shift of +15° and other with a phase shift of -15° used. The gate pulse pattern for converter-1 is advanced by 15° and that of converter-2 is delayed by 15° which gives a phase angle of  $0^0+15^0 = 15^0$  for first converter which is connected to Y-secondary and a phase angle of  $-30^0-15^0 = -45^0$  for the second converter which is connected to Δ-secondary.

In a similar way 36-pulse converter is designed with 3 converters and three corresponding phase shifting transformer. It is made of one 24-pulse converter and one 12-pulse converter. The 24-pulse converter has two converters phase angles of +7.5° each and phase angle of 12-pulse converter is -15°. The gate pulse patterns are phase shifted in a similar way.

For synthesizing 48-pulse model four phase shifting transformers are given a phase shift in the following manner: First Y/Y transformer with a phase shift of +7.5°, second Y/Δ transformer with a phase shift of +7.5°, third Y/Y transformer with a phase shift of -7.5° and fourth Y/Δ transformer with a phase shift of -7.5°. Phase angles of the four converters can be obtained as 7.5°, -22.5°, -7.5° and 37.5° by following the same procedure that was adapted for 24-pulse [12]. Configurations of these four models are summarized in table no. I.

TABLE I  
Configuration of 12- pulse, 24- pulse, 36- pulse and 48- pulse STATCOM

	12- PULSE	24- PULSE	36- PULSE	48- PULSE
<b>No. Of Converters</b>	1	2	3	4
<b>Gate Pulse Pattern Of Converters</b>	[0°]	[15° -45°]	[ +7.5° -22.5° -15°]	[+7.5° -22.5° -7.5° - 37.5°]
<b>Phase Angle Of Phase Shifting Transformer</b>	[0°]	[15° -15°]	[+7.5° +7.5° -15°]	[+7.5° +7.5° -7.5° - 7.5°]
<b>Optimum Dead Angle</b>	15°	7.5°	5°	3.75°

**V. SELECTION of OPTIMUM DEAD ANGLE**

A phase difference of 30° between Y and Δ secondary cancel 5<sup>th</sup>, 7<sup>th</sup> etc. harmonics which is evident from equations (1) and (2). In general harmonics of order 5+12k (5<sup>th</sup>,17<sup>th</sup>,29<sup>th</sup> etc...) and 7+12k (7<sup>th</sup>,19<sup>th</sup>,31<sup>st</sup> etc.) are cancelled. A phase shift of  $\frac{360^0}{P/2}$  provided between the converter groups helps cancelling 11<sup>th</sup> and 13<sup>th</sup> harmonics or in general 11+24k (11<sup>th</sup>,35<sup>th</sup>,59<sup>th</sup>...) and 13+24k (13<sup>th</sup>,37<sup>th</sup>,61<sup>st</sup>...) are eliminated. So the most significant harmonic in a P-pulse converter which are not eliminated are  $\frac{P}{2}+1, \frac{P}{2}-1, P+1$  and  $P-1$ . So for a 24-pulse the harmonics not removed are 11<sup>th</sup>, 13<sup>th</sup>, 23<sup>rd</sup>, 25<sup>th</sup>. To eliminate  $\frac{P}{2}+1, \frac{P}{2}-1$  order harmonics in a P-pulse VSC proper selection of dead angle is necessary.

For eliminating a particular K<sup>th</sup> order harmonic  $\beta=180/2k$  [9]. From the previous discussion we have concluded that by proper selection of dead angle  $\frac{P}{2}+1, \frac{P}{2}-1$  order harmonics will be eliminated. Hence we can simply deduce that for a P-pulse converter dead angle should be  $\beta=\frac{180/2}{P/2}=180/P$ . The conduction angle  $\sigma=180-2\beta$ . For 12-pulse, 24-pulse, 36-pulse, 48-pulse STATCOM dead angle chosen to be 15°, 7.5°, 5°, 3.75° respectively as represented in table-I. Choosing dead angle something else apart from these calculated values will increase THD [9].

Different values of dead angle are applied in the simulation model and percentage THD is recorded. These values are plotted and fig. 3 is obtained which shows THD increases if the dead angle is either increased or decreased from 7.5° in case of a 24-pulse STATCOM.

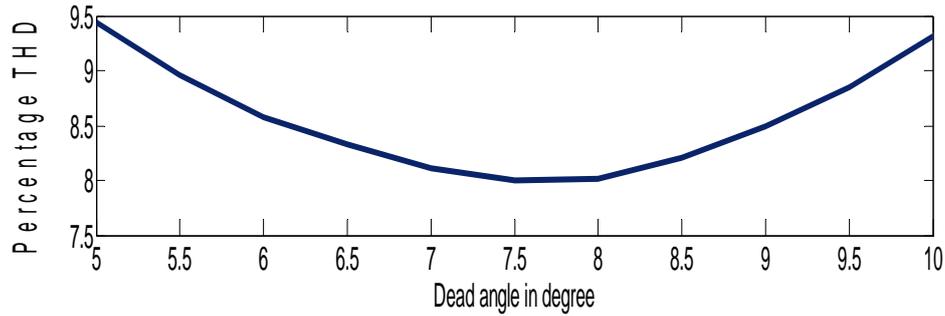


Fig. 3. Percentage THD with respect to dead angle

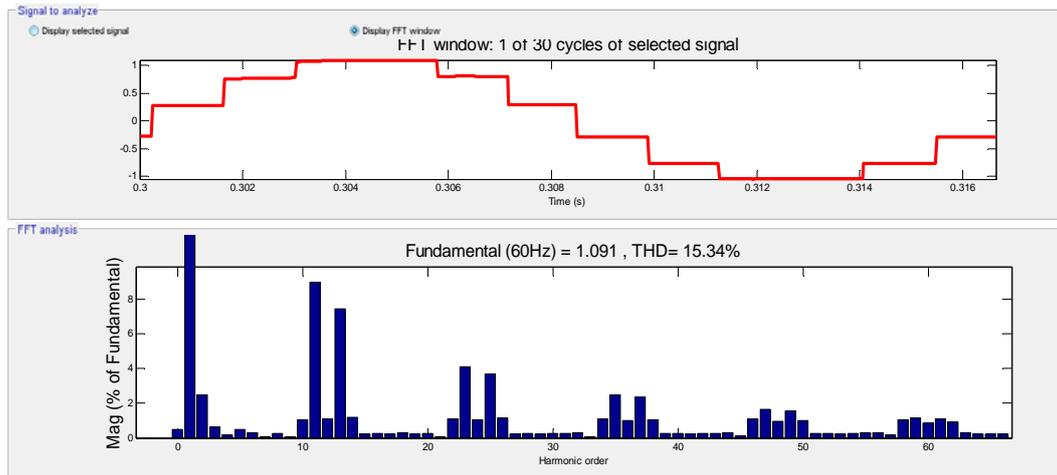


Fig.4. 12-Pulse output voltage and Percentage THD of 24-Pulse STATCOM for zero dead angle

TABLE II  
Comparison of Harmonic Content of Models for Zero Dead Angle and Optimum Dead Angle

	12- PULSE		24- PULSE		36- PULSE		48- PULSE	
	$\beta=0^\circ$	$\beta=15^\circ$	$\beta=0^\circ$	$\beta=7.5^\circ$	$\beta=0^\circ$	$\beta=5^\circ$	$\beta=0^\circ$	$\beta=3.75^\circ$
<b>INDUCTIVE MODE</b>	30.92%	17.68%	15.34%	8.88%	12.03%	6.33%	8.20%	5.10%
<b>CAPACITIVE MODE</b>	31.16%	17.38%	15.38%	8%	11.9%	6.06%	8.02%	4.42%
<b>FLOATING MODE</b>	31.11%	17.31%	15.2%	7.8%	11.76%	6.01%	7.77%	4.01%

One important point to be noticed here is that if  $\beta$  is made zero, then a VSC of ‘P’ number of pulses behaves as a VSC of ‘P/2’ pulses which also implies that the three-level converters behaves as a two-level converter. From fig. 4 we can observe a 24-pulse STATCOM gives 12-pulse output for zero dead angle. Observing its percentage THD, we can see its harmonic content is little lower than that of 12-pulse STATCOM which is shown by fig. 5d. The percentage THD values of other models under zero dead angle are tabularized in table-II.

### VI. SIMULATION RESULTS

Considering the output voltage of a 48-pulse STATCOM from fig. 5a we can observe each cycle consists of 48 steps each step of duration  $360^\circ/48 = 7.5^\circ$  which is  $3.97 \times 10^{-4}$  sec in time for a 60 Hz system. We can also observe at peak points of the wave approximately 3 pulses are combined. In a similar way it can be observed from fig.5 that output waveforms of 12-pulse, 24-pulse, 36-pulse STATCOM contain 12, 24, 36 steps respectively. For better performance of STATCOM these waveforms should be sinusoidal which is possible if it contains more number of steps.

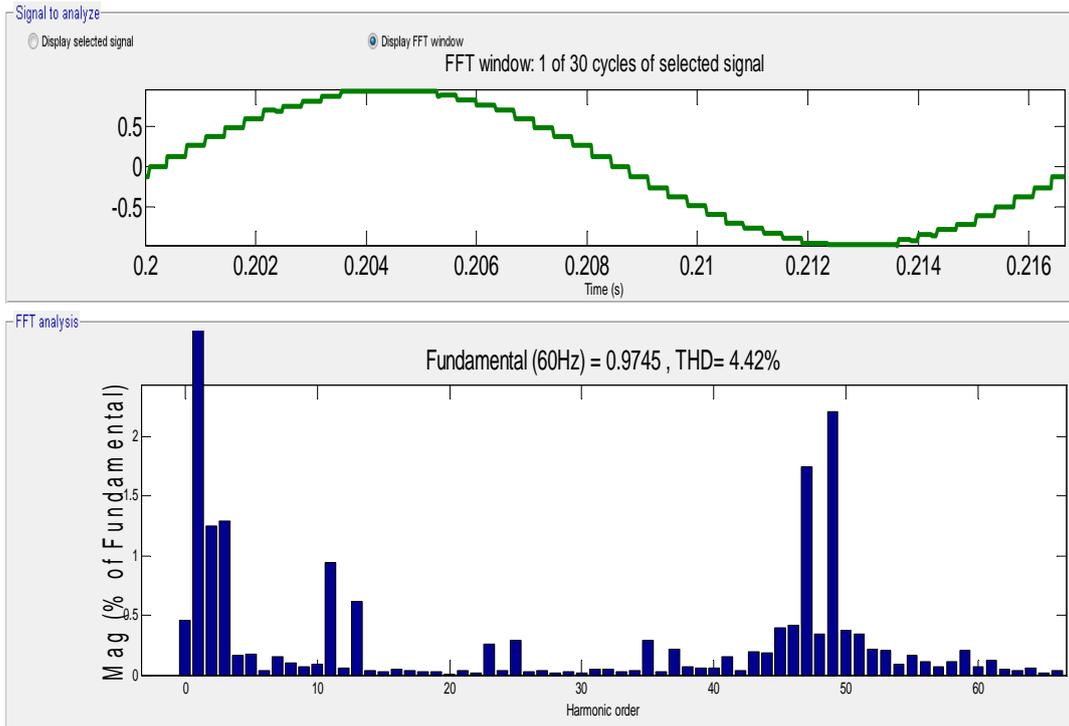


Fig.5a. 48-pulse output voltage and THD during capacitive mode

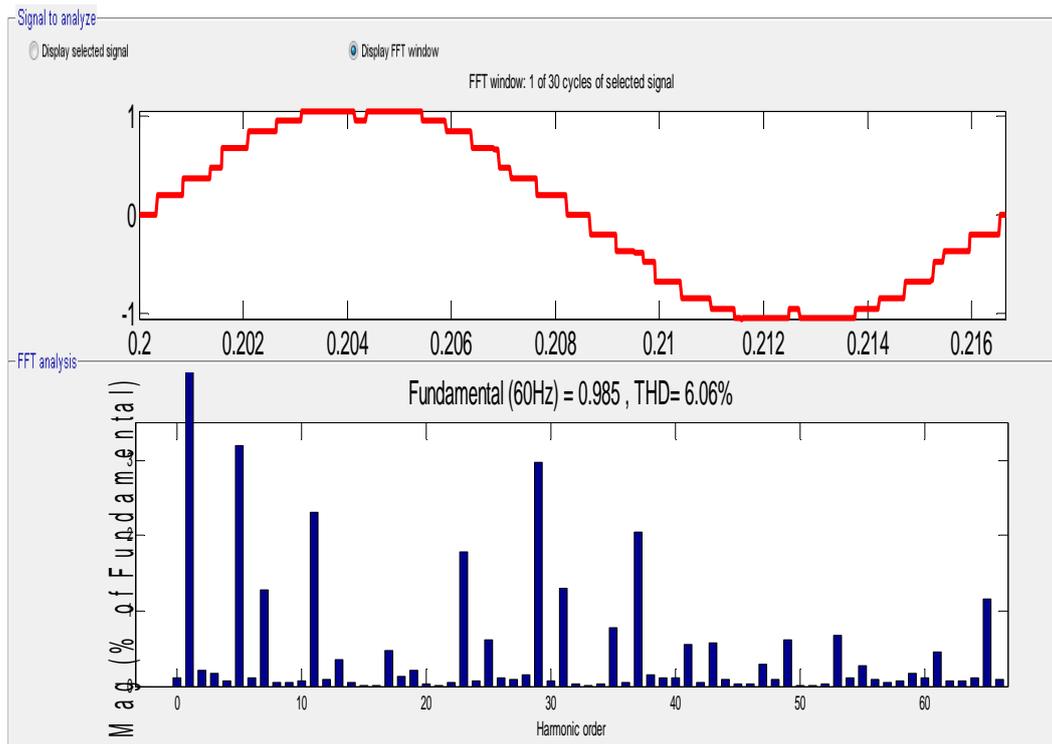


Fig.5b. 36-pulse output voltage and THD during capacitive mode

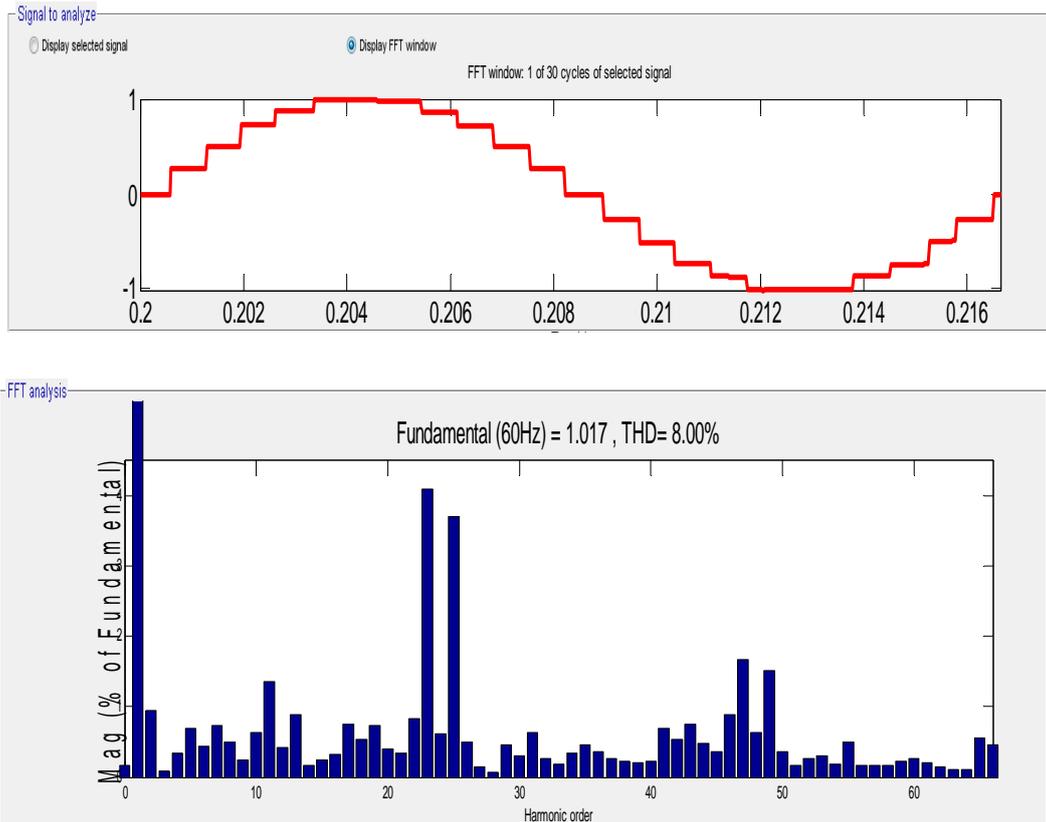


Fig.5c. 24-pulse STATCOM output voltage and THD during capacitive mode

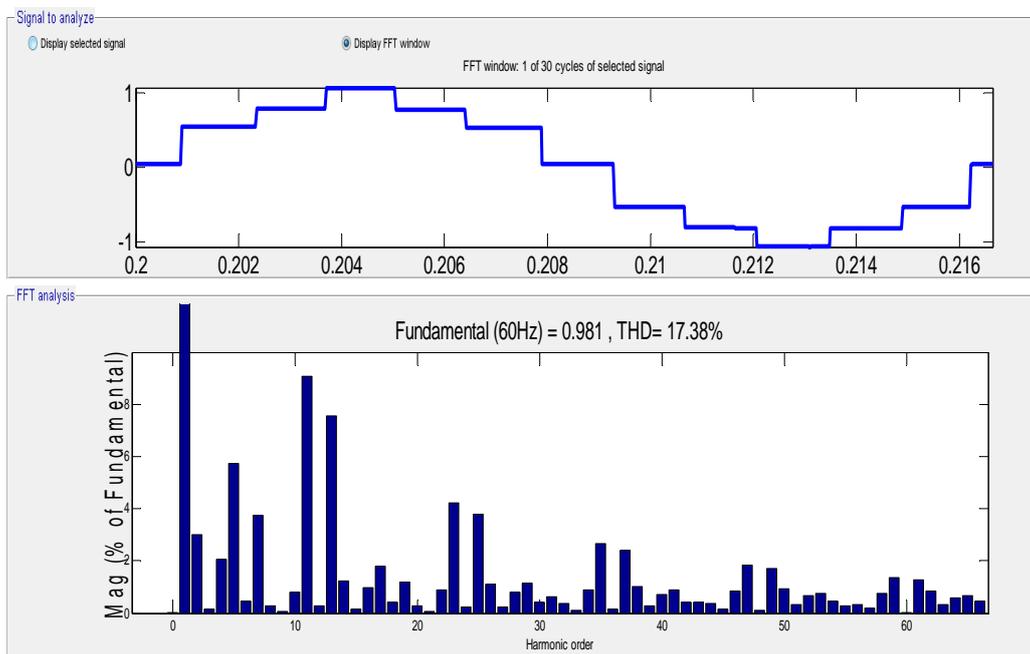


Fig.5d. 12-pulse STATCOM output voltage and THD during capacitive mode

STATCOM has three modes of operation: - inductive, capacitive and floating mode. When STATCOM output voltage is less than system voltage, it operates in capacitive mode by generating reactive power. When STATCOM output voltage is more than system voltage it operates in inductive mode by consuming reactive power. When STATCOM output voltage and system voltage are equal it operates in floating mode without any reactive power exchange.

For demonstration of the models in three modes, the magnitude of programmable voltage source used is set to 0.96 p.u. at 0.2 sec. This reference voltage is again increased to 1.04 p.u. at 0.3 sec. This value is set back to 1p.u at 0.4 sec.

A. *Capacitive Mode:*

Considering the 24-pulse STATCOM, at 0.2 sec when the reference voltage reduced by 4% and made 0.96 p.u., STATCOM automatically comes into actions by supplying a reactive power  $Q=65$  MVAR with increased capacitor voltage and manages to raise the voltage level up to 0.981 p.u.as shown in fig 6. At  $t=0.32$  sec capacitor voltage is increased up to 43.8 KV. During this mode of operation Total Harmonic Distortion (THD) of STATCOM output voltage is 8% having a peak value of fundamental component as 1.017 which is evident from fig. 5c.

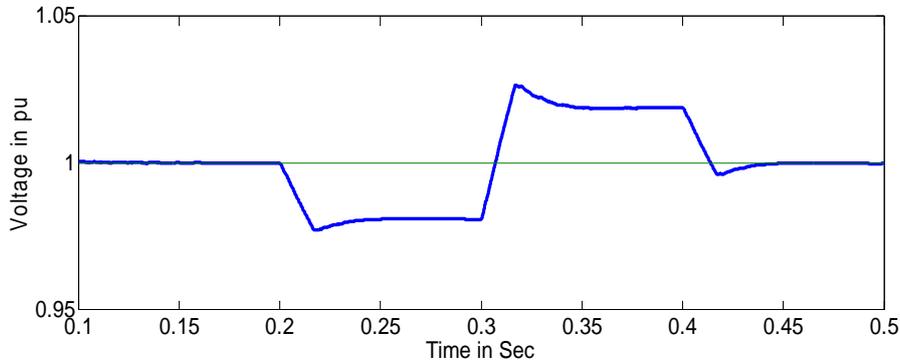


Fig.6a. 24-pulse measured voltage w.r.t. reference voltage

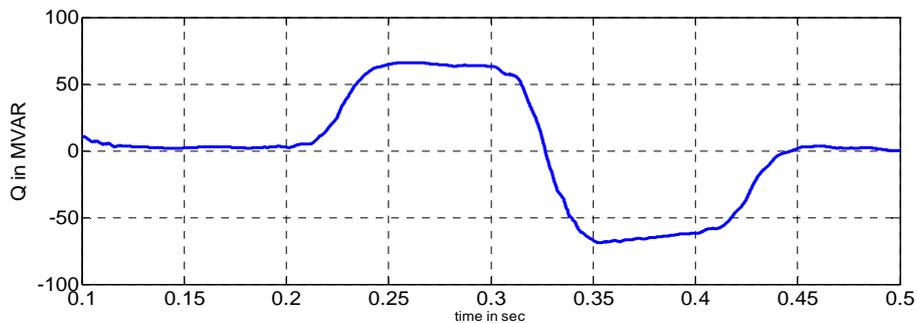


Fig.6b. 24-pulse STATCOM Reactive Power

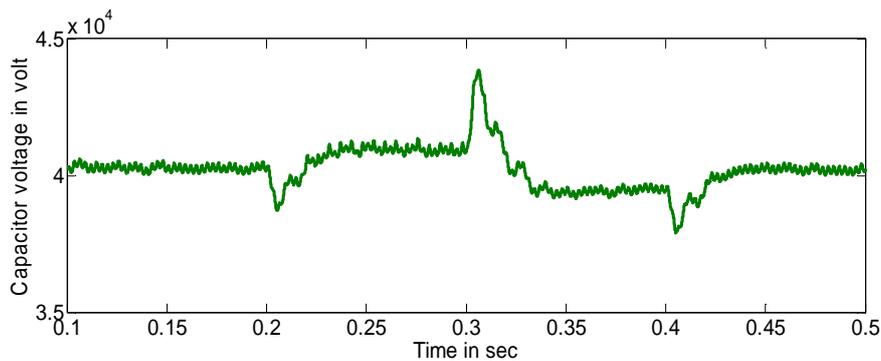


Fig.6c. 24-pulse DC capacitor voltage

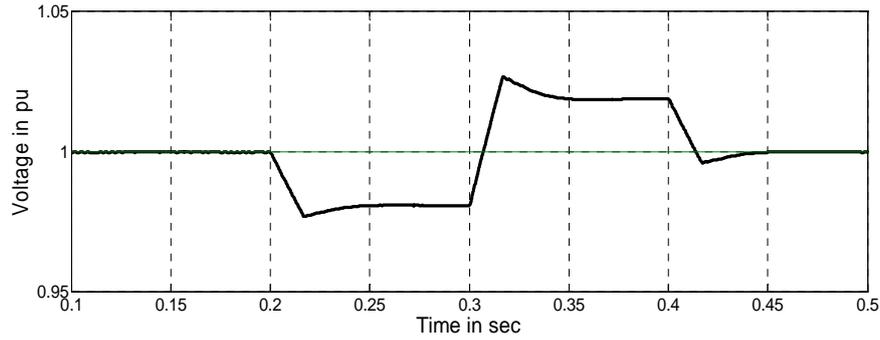


Fig.7a. 48-pulse STATCOM measured voltage w.r.t. reference voltage

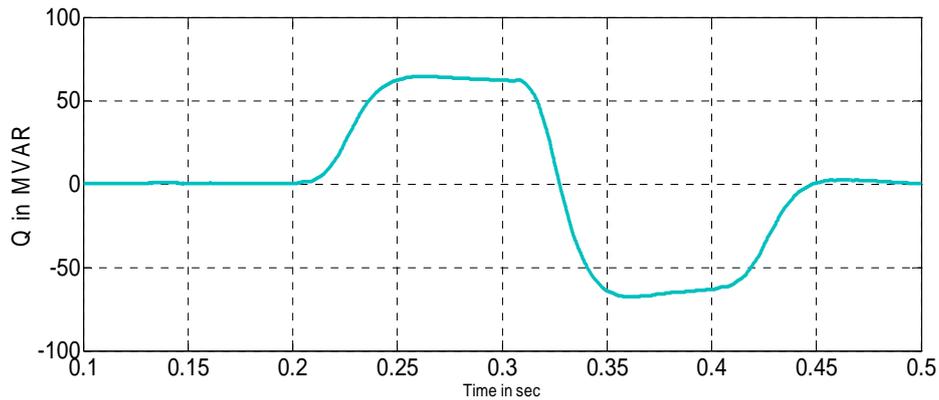


Fig.7b. 48-pulse STATCOM Reactive Power

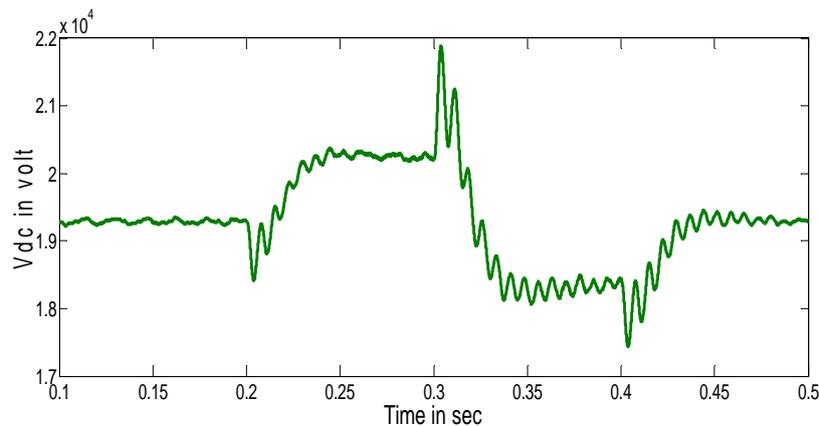


Fig.7c. DC capacitor voltage of 48-pulse STATCOM

During the same time period 0.2 sec to 0.3 sec, 12-pulse, 36-pulse, 48-pulse STATCOM limits the voltage reduction to 0.981 p.u.. But for this purpose the capacitor voltage has been increased to 84.8 KV in case of 12-pulse, 63.3 KV in case of 36-pulse, 21.9 KV in case of 48-pulse. Hence we can observe when number of pulse becomes 'x' times, the capacitor voltage required to compensate the same voltage is reduced by approximately 'x' times. For reference capacitor voltage of 12-pulse, 24-pulse, 36-pulse, and 48-pulse are tabularized in table no-III.

For harmonic comparison point of view THD of STATCOM output voltages of these four models is shown in fig. 5. THD for 12-pulse, 24-pulse, 36-pulse, 48-pulse in capacitive mode are found out to be 17.38%, 8%, 5.91%, and 4.38% respectively. Here also we can observe that as the number of pulses increased by 'x' times, THD reduced by 'x' times.

**B. Inductive Mode:**

Reference voltage is increased by 4 % to 1.04 at t=0.3 sec and set back to 1 p.u. at t=0.4 sec. considering the 48-pulse model of fig. 7, the voltage is reduced to 1.019 p.u. by absorbing a reactive power of Q= -67.45 MVAR and DC voltage is lowered to 17.5 KV. During this mode THD of this model is 5.10%.

Percentage THD of STATCOM output voltage in inductive mode is shown in fig. 8. We can deduce here that THD reduces with the increment of number of pulses. One point worth observing from table-III is THD in inductive mode is more than that of in capacitive mode. Harmonic content in system voltage for all the models is also monitored and mentioned in Table-III. THD in system voltage of 12-pulse and 48-pulse during inductive mode of operation is shown in fig. 9. In a similar fashion harmonic content in system voltage is also reduced with the increased number of pulses.

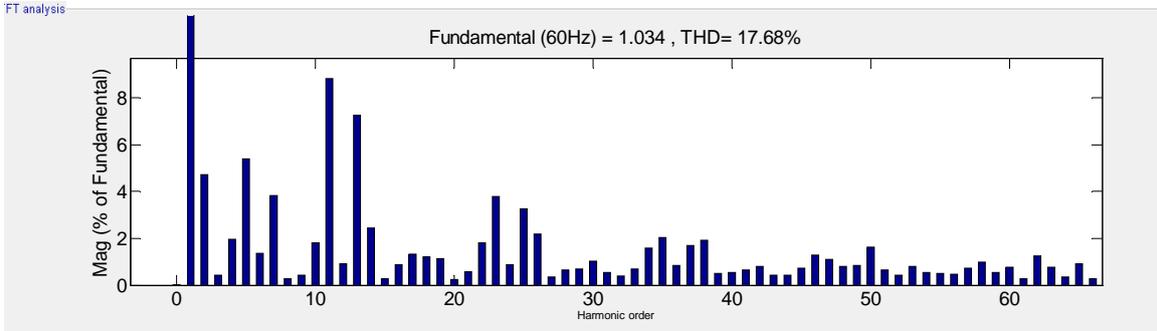


Fig.8a. THD in 12-pulse output voltage during inductive mode

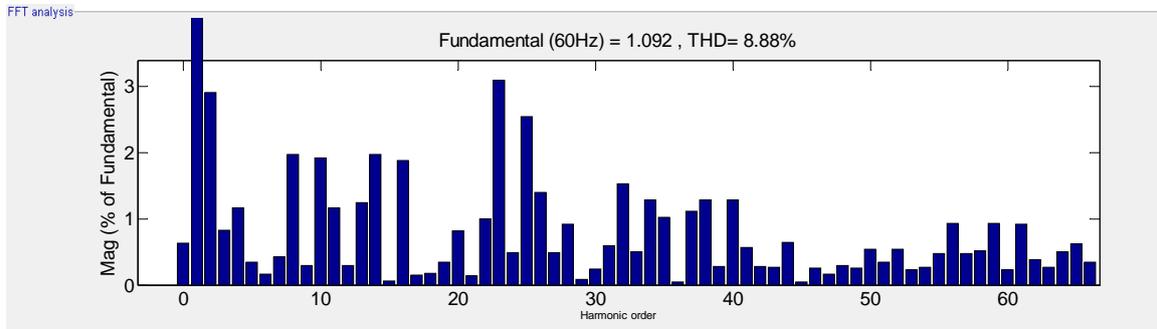


Fig.8b. THD in 24-pulse output voltage during inductive mode

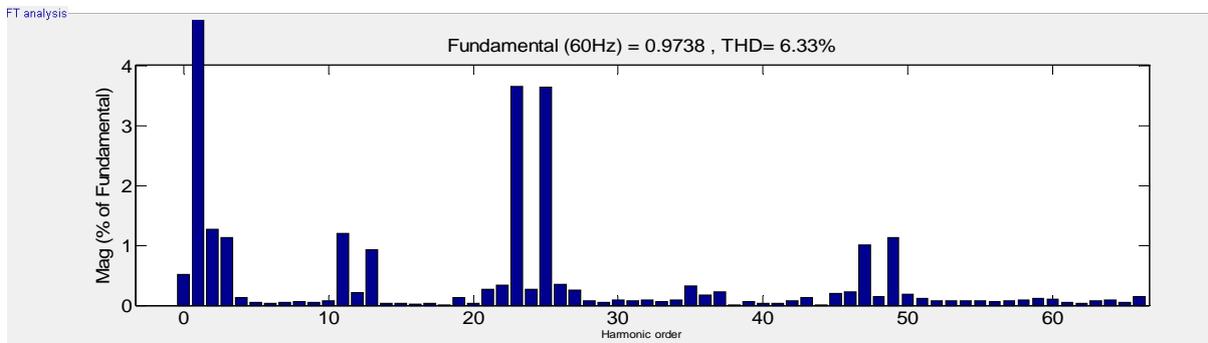


Fig.8c. THD in 36-pulse output voltage during inductive mode

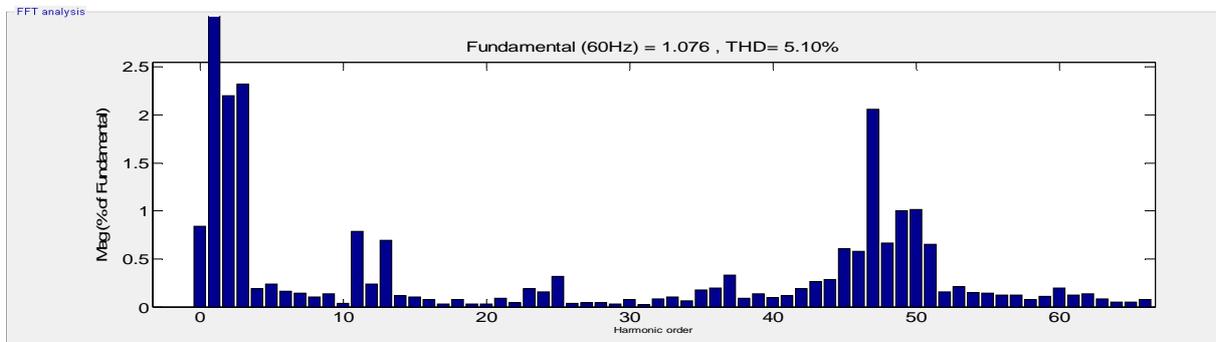


Fig.8d. THD in 48-pulse output voltage during inductive mode

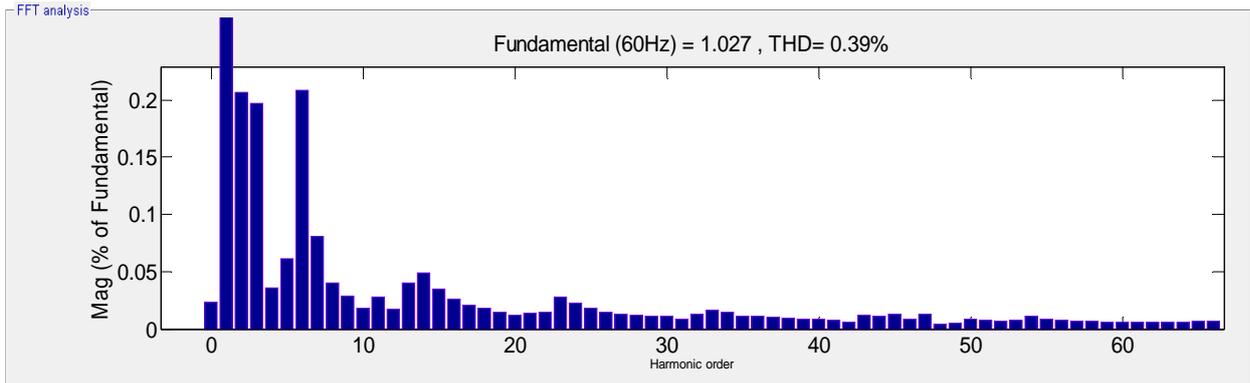


Fig.9a. THD in System voltage of 48-pulse STATCOM

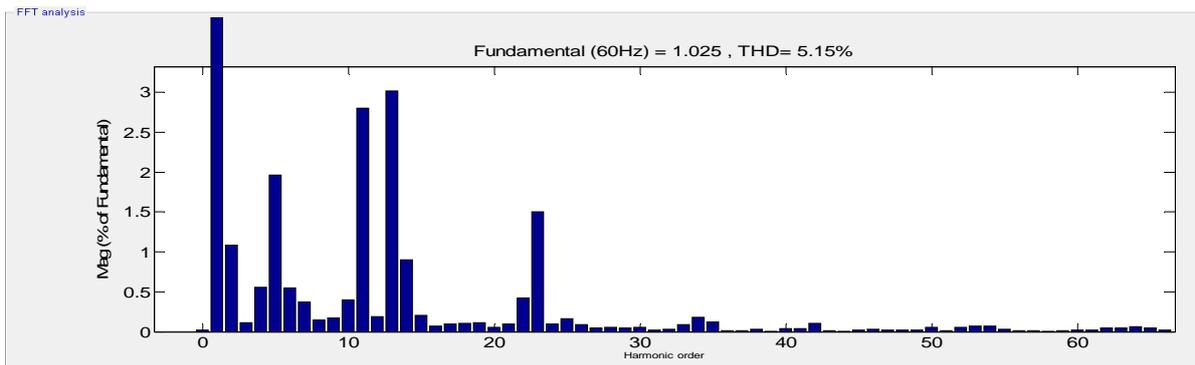


Fig.9b. THD System voltage of 12-pulse STATCOM

*C. Floating Mode:*

As discussed earlier, during this mode system voltage and STATCOM output voltage remains same; hence STATCOM remains inactive because there is no reactive power exchange. The 36-pulse STATCOM output voltage THD during this mode is shown in fig. 10 and THD of rest models are tabularized in table-III. We can observe that THD in case of floating mode is lower compared to the other two modes. We can also observe the system THD reduces with the increase of number of pulses from table no-III.

TABLE III  
Comparison of Performance of 12- pulse, 24- pulse, 36- pulse and 48- pulse STATCOM

	12- PULSE			24- PULSE			36- PULSE			48- PULSE		
	% THD OF STATCOM O/P	% THD OF SYSTEM VOLT.	V <sub>C</sub> REQUIRED	%THD OF STATCOM O/P	%THD OF SYSTEM VOLT.	V <sub>C</sub> REQUIRED	%THD OF STATCOM O/P	%THD OF SYSTEM VOLT.	V <sub>C</sub> REQUIRED	%THD OF STATCOM O/P	%THD OF SYSTEM VOLT.	V <sub>C</sub> REQUIRED
<b>INDUCTIVE MODE</b>	17.68%	5.15%	77.8KV	8.88%	1.16%	37.9KV	6.33%	1.32%	24.7KV	5.10%	0.39%	17.5KV
<b>CAPACITIVE MODE</b>	17.38%	4.99%	84.8KV	8%	1.13%	43.8KV	6.06%	1.01%	29.9KV	4.42%	0.13%	21.9KV
<b>FLOATING MODE</b>	17.31%	4.92%	-	7.8%	1.10%	-	6.01%	0.97%	-	4.01%	0.10%	-

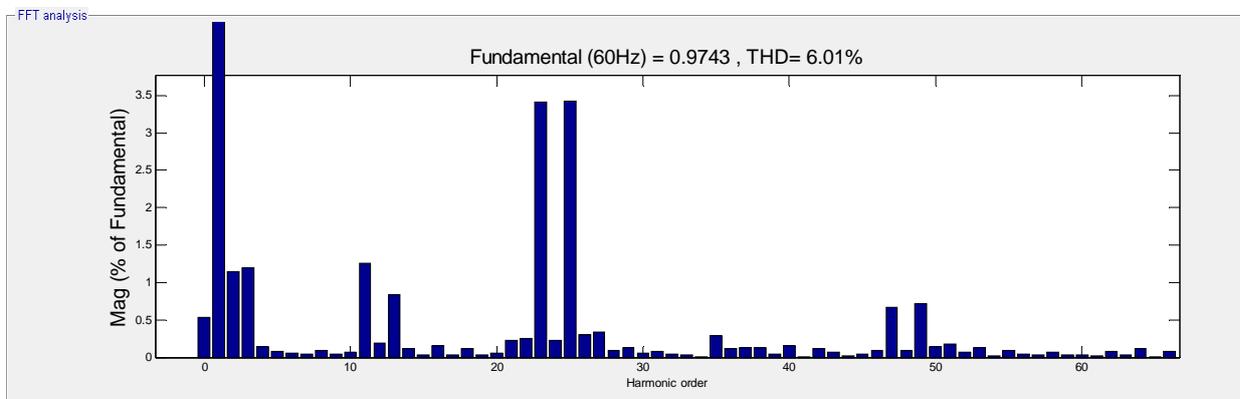


Fig.10. THD in 36-pulse output voltage during floating mode

**VII. CONCLUSION**

The models of 12-pulse, 24-pulse, 36-pulse and 48-pulse STATCOM are synthesized in MATLAB using three-level NPC based converter and valid results are shown through the simulation diagrams. The harmonic content of the STATCOM output voltage and system output voltage were observed in three different modes. From the observation it is concluded that percentage THD reduced by x times when number of pulses of a model are increased by ‘x’ times. With the increase of pulse number STATCOM output become more sinusoidal and harmonic content reduced. With higher pulse STATCOMs the harmonic content in STATCOM output voltage is successfully reduced as per IEEE 519 standard whereas harmonic content of grid system voltage is within the limit as per IEEE 519 standard in all the models designed in this paper [18].

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