Comparative Study of Multicarrier PWM Techniques for a Modular Multilevel Inverter

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***Abstract*— This paper presents the simulation of three phase five-level modular multilevel cascade inverter based on double-star chopper-cell (DSCC). The multicarrier PWM techniques such as Phase disposition PWM (PDPWM), Phase opposition disposition PWM (PODPWM), Alternate phase opposition disposition PWM (APODPWM), and Phase shift PWM (PSPWM) is employed and a comparative study is done based on the spectral quality of the load voltage and load current waveforms. Simulation has been carried out for various modulation indices using MATLAB/Simulink and the results are verified.**

Keyword- Modular Multilevel Converter (MMC), Double star chopper cells (DSCC), Multicarrier PWM (MCPWM), Total harmonic distortion (THD).

I. INTRODUCTION

Modular multilevel converters have great potential in high-power applications, such as dc interconnections, dc power grids, and off-shore wind power generation are in need of accurate power flow control and high-efficiency power conversion in order to reduce both their operating costs and their environmental impact [1]. High power converters for utility applications require line-frequency transformers for the purpose of enhancing their voltage or current rating. The use of line-frequency transformers, however, not only makes the converter heavy and bulky, but also induces the so-called dc magnetic flux deviation when a single-line-to-ground fault occurs [2].

Multilevel converters are used for achieving medium-voltage power conversion without transformers. Two of the representatives are: 1) the diode-clamped multilevel converter (DCMC); 2) the flying-capacitor multilevel converter (FCMC). The three-level DCMC or a NPC converter has been put into practical use. If a voltage-level number is more than three in the DCMC, inherent voltage imbalance occurs in the series-connected dc capacitors, thus resulting in requiring an external balancing circuit (such as a buck–boost chopper) for a pair of dc capacitors. Furthermore, a significant increase in the clamping diodes required renders assembling and building of each leg more complex and difficult. As for the FCMC, the high expense of flying capacitors at low carrier frequencies (say, lower than 1 kHz) is the major disadvantage of the FCMC.

The characteristics of the modular multilevel converter is low switching losses due to a considerably lower switching frequency ($f_s \approx 3f1$), compared to a 2-level equivalent. Apart from the lower switching frequency, the quality of the output voltage waveform is higher. Thus smaller and simpler harmonic filters are required. A short circuit at the DC-bus will not discharge the storage capacitors therefore fault recovery is very fast [2]. The modular multilevel converter provides simplicity of design and control, as well as scalability to various voltage and or power levels. Moreover, modular multilevel converter has the potential to improve the reliability, as a faulty module can be bypassed without significantly affecting the operation of the whole circuit.

The Modular Multilevel inverter is classified as Single Star Bridge Cells (SSBC), Single Delta Bridge Cells (SDBC), Double Star Chopper Cells (DSCC) and Double Star Bridge Cells (DSBC) [3].The double-star-configured MMC topology possesses the common dc-link terminals as shown in fig.1 (a), which enables dc-to-ac and ac-to-dc power conversion. However, the star/delta-configured MMC topology has no common dc-link terminals. As a result, it has no capability of achieving dc-to-ac and ac-to-dc power conversion although it can control active power back and forth between the three phase ac terminals and the floating dc capacitors. This means that the star/delta-configured MMC topology is not applicable to industrial motor drives, but it is suitable for STATCOMs and energy storage systems. Compared to SSBC, SDBC, DSBC configurations, DSCC is superior and widely used [19]-[23], because number of switches used in sub-module is half of bridge cell thereby switching losses reduces and efficiency of the converter increases. Also DSCC does not require grid inductor and it is connected to grid directly.

II. STRUCTURE OF MODULAR MULTILEVEL INVERTER

Fig. 1(a) and 1(b) shows the single phase and three phase equivalent circuit of five-level MMC with DSCC configuration, The converter has one leg comprises of two arms including the upper arm and the lower arm, with each arm having four Sub-Modules (SM) and two non coupled buffer inductors and an equivalent resistor [16]-[18] Each sub module comprises of two switches and one sub module capacitor as shown in fig. 1(c). The two non coupled buffer inductors are inserted into the arms, since they do not disturb operation or generate overvoltage for the semiconductors. The buffer inductor can limit the AC-current, whenever the DC-Bus is short circuited (fault condition) and it act as passive filter during normal condition [24], [25]. The DC Link of MMC is connected to high-voltage sources depending on the working purpose of the converter. The output of the converter is the connection point of the upper and lower arm which is connected to RL load.

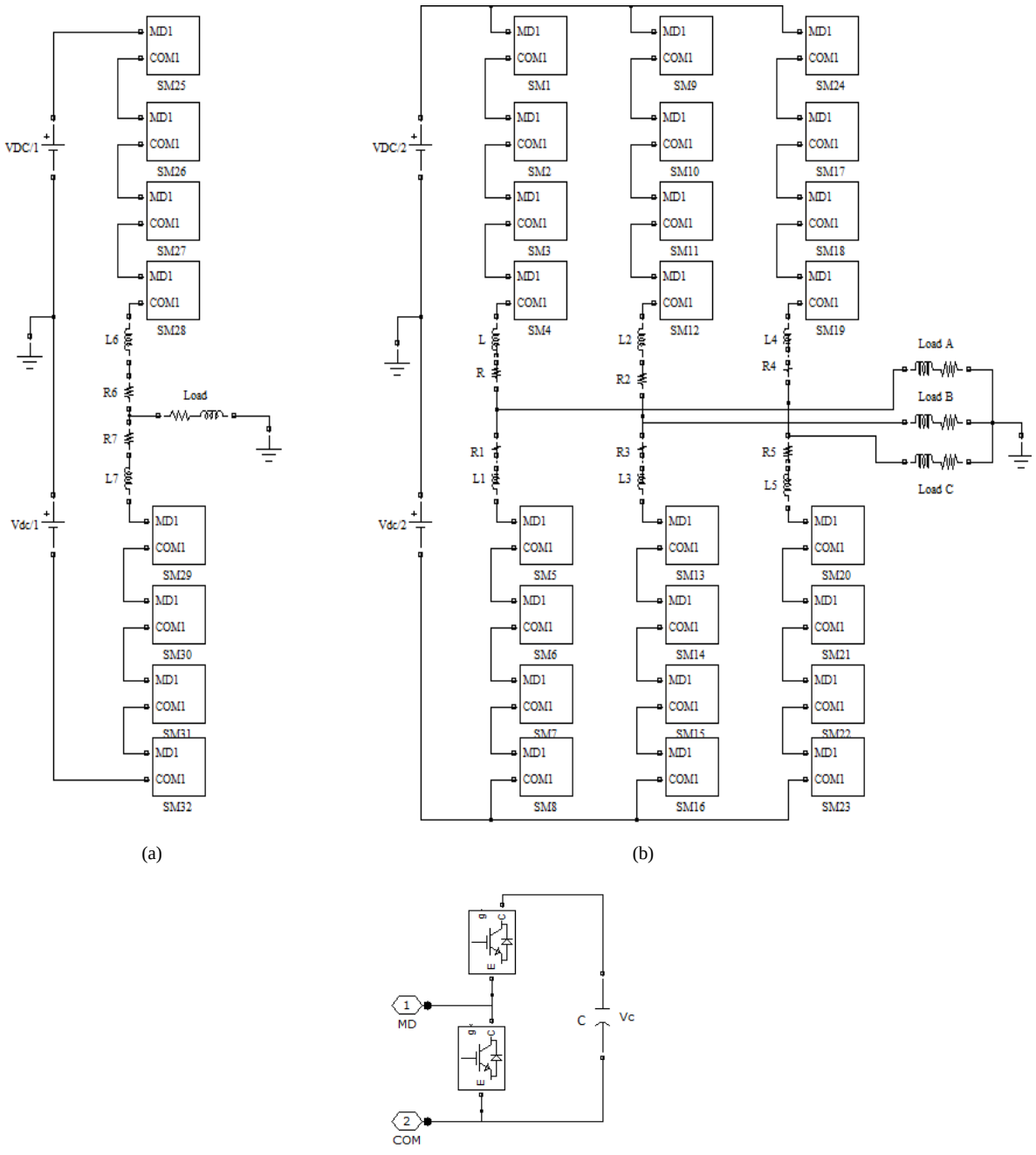

Fig. 1. (a) Single phase equivalent circuit of five-level modular multi-level inverter. (b) Three phase equivalent circuit of five-level modular multi-level inverter. (c). Bidirectional PWM chopper-cell with a floating dc capacitor.

TABLE I
Switching combinations for a 5-level Modular multilevel inverter

SM	Output Phase Voltage																																					
	$V_{dc}/2$	$-V_{dc}/2$	$V_{dc}/4$																$-V_{dc}/4$																			
S_{1T}	0	1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	1	1	1	1				
S_{2T}	0	1	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	1	1	1	1	1	1	1	1	0	0	0	0	1	1	1	1				
S_{3T}	0	1	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0				
S_{4T}	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1				
S_{5T}	1	0	1	1	1	1	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0				
S_{6T}	1	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0				
S_{7T}	1	0	1	1	1	1	1	1	1	0	0	0	0	1	1	1	1	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0				
S_{8T}	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1				

TABLE II
Switching combinations for a 5-level Modular multilevel inverter

SM	Output Phase Voltage																																					
	0V																																						
S_{1T}	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0				
S_{2T}	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1				
S_{3T}	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0				
S_{4T}	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	1	1	1	1	1				
S_{5T}	1	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0		
S_{6T}	1	1	0	0	0	1	1	1	0	0	0	1	1	1	0	0	0	1	1	1	0	0	0	1	1	1	0	0	0	1	1	1	0	0	0	1		
S_{7T}	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0		
S_{8T}	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	1		

The possible switching combinations for a 5-level modular multilevel inverter are summarized as Table I and II. In this table S_{jT} stands for the state (ON = 1, OFF = 0) of the top switch of j^{th} sub-module and the bottom switch of j^{th} sub-module is in complementary state.

III. MULTI-CARRIER PWM STRATEGIES FOR MODULAR MULTILEVEL INVERTER

Multi-Carrier PWM strategies is widely used, because it can be easily implemented to low voltage modules. MCPWM be classified as level shifted PWM (LS-PWM) and Phase shifted PWM (PS-PWM) techniques. The level shifted PWM (LS-PWM) are In Phase Diposition (PD), Phase Opposition Disposition (POD) and Alternative Phase Opposition Disposition (APOD) [6]-[11]. In general the amplitude modulation index (m_a) for level shifted PWM technique is defined as the ratio of amplitude of the reference sine wave (A_r) to the amplitude of the carrier wave (A_c) and it is given in equation (1).

$$m_a = \frac{2A_r}{(m-1)*A_c} \quad (1)$$

Similarly, the amplitude modulation index (m_a) for phase shifted PWM technique is given in equation (2).

$$m_a = \frac{A_r}{(\frac{A_c}{2})} \quad (2)$$

The frequency modulation index (m_f) for level shifted and phase shifted PWM techniques is defined as the ratio of frequency of the carrier wave (f_c) to the frequency of the reference sine wave (f_r) and it is given in equation (3).

$$m_f = \frac{f_c}{f_r} \quad (3)$$

A. Phase Disposition PWM (PDPWM)

In this method all the carriers above and below zero reference line are in same phase. If all the carriers are selected with the same phase, the method is known as Phase Disposition (PD) method [15], [26]. Carrier and reference wave arrangements are as shown in Fig. 2. The PDPWM is the widely used strategy for Modular Multilevel converters and conventional multilevel inverters because it provides load voltage and current with lower harmonic distortion [12]-[15].

The converter is switched to + Vdc / 2 when the sine wave is greater than both carriers, the converter switches to +Vdc / 4 when the sine wave is lower than the uppermost carrier waveform and greater than all other carriers, the converter is switched to zero when sine wave is lower than upper carrier but higher than the lower

carrier, the converter switches to - Vdc / 4 when the sine wave is higher than the lowermost carrier waveform and lesser than all other carriers and the converter is switched to - Vdc / 2 when the sine wave is less than both carrier waveforms.

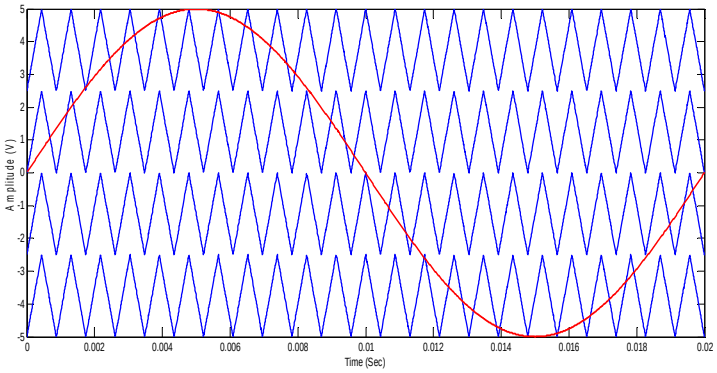

Fig. 2. Carrier arrangement for PDPWM strategy (m_a=1 and m_f=23)

B. Phase opposition disposition PWM (PODPWM)

In this method all the carriers have the same frequency and the adjustable amplitude (different or unequal amplitudes). But all the carriers above the zero value reference are in phase among them but in opposition (180 degrees phase shifted) with those below. Carrier and reference wave arrangements are as shown in Fig. 3.

The converter is switched to + Vdc / 2 when the sine wave is higher than both carrier waveforms, the converter switches to +Vdc / 4 when the sine wave is lower than the uppermost carrier waveform and greater than all other carrier, the converter is switched to zero when the sine wave is greater than the lower carrier waveform but less than the upper carrier waveform, the converter switches to - Vdc / 4 when the sine wave is higher than the lowermost carrier waveform and lesser than all other carriers and the converter is switched to - Vdc / 2 when the sine wave is less than both carrier waveforms [12]-[15].

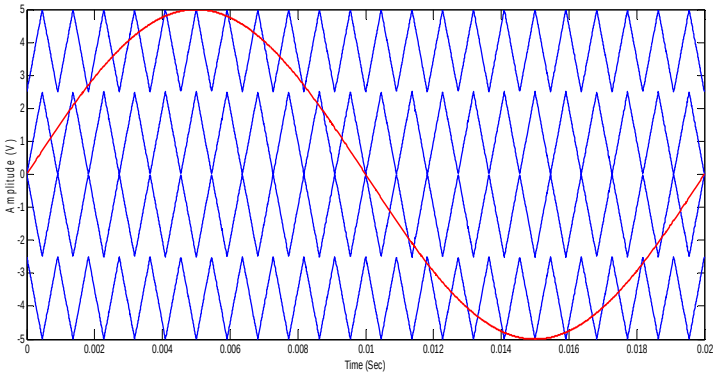

Fig. 3. Carrier arrangement for PODPWM strategy (m_a=1 and m_f=23)

C. Alternate phase opposition disposition PWM (APODPWM)

In this method all the carriers have the same frequency and the adjustable amplitude (different or unequal amplitudes). All the carriers have180^0 phase shift between them. The converter switches to Vdc/2 when the reference wave is higher than all carrier waves, the converter switches to $+V_{dc}$ / 4 when the sine wave is lower than the uppermost carrier waveform and greater than all other carrier, the converter switches to zero when the sine wave is lower than the two uppermost carrier waveform and greater than two lowermost carrier, the converter switches to - V_{dc} / 4 when the sine wave is higher than the lowermost carrier waveform and lesser than all other carriers and the converter switches to - V_{dc} / 2 when the sine wave is lesser than all carrier [13].

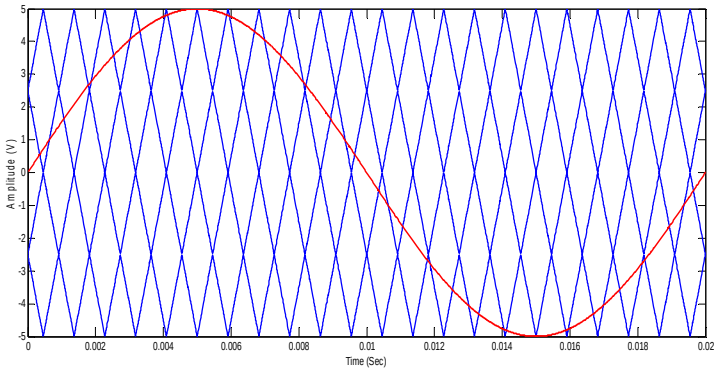

Fig. 4. Carrier arrangement for APODPWM strategy (m_a=1 and m_f=23)

D. Phase Shift PWM (PSPWM)

The phase shift multicarrier PWM technique is another type of multicarrier PWM strategy and has its performance parameters closest to PDPWM strategy [12]-[15]. It uses four carrier signals of the same amplitude and frequency which are shifted by 90 degrees to one another as shown in fig. 5.

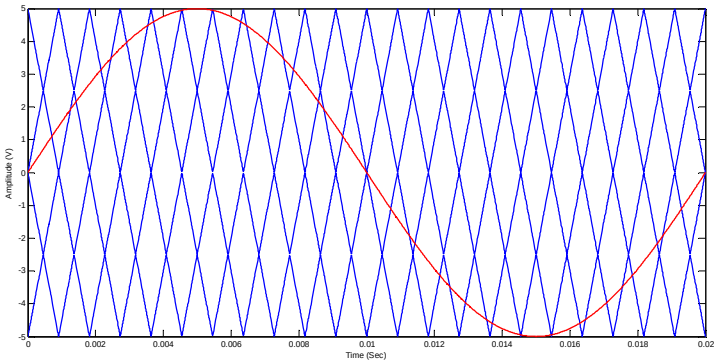

Fig. 5. Carrier arrangement for PSPWM strategy (m_a=1 and m_f=23)

IV. SIMULATION RESULTS

In order to verify the modulation method, a three phase five-level MMC-DSCC is simulated using Matlab/Simulink and its performance is studied for RL load.

TABLE III
Simulation Parameters

Parameters	**Values**
DC Voltage	500 V
No. of Sub-modules in each arm	4
Sub-module Capacitor C	2.5mF
Sub-module Capacitor Voltage	125 V
Arm Inductor L	1.0mH
Arm Equivalent Resistance	1.0Ω
Amplitude Modulation index	0.8
Frequency Modulation index	23
Carrier frequency	1150 Hz
Power frequency	50 Hz
Load	500Ω, 1H

The output phase voltage, line voltage and line current of three phase five-level modular multilevel inverter employing PDPWM is shown in Fig. 6, 7 and 8 and Fig. 9,10 and 11 shows the FFT analysis of the output phase voltage, line voltage and output line current for RL load. The Total Harmonic Distortion (THD) for phase voltage is 24.58%, for line voltage 16.85% and for phase current 1.90%.

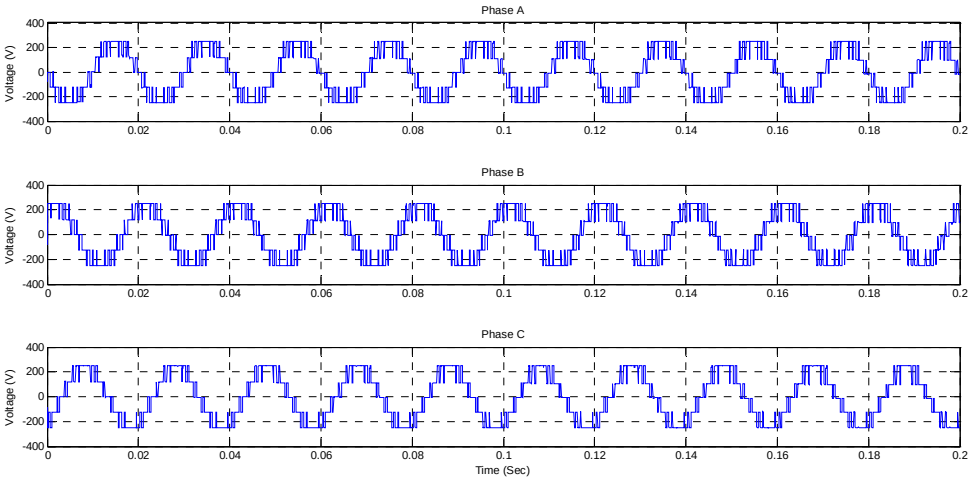

Fig. 6. Simulated phase voltage by PDPWM for RL load

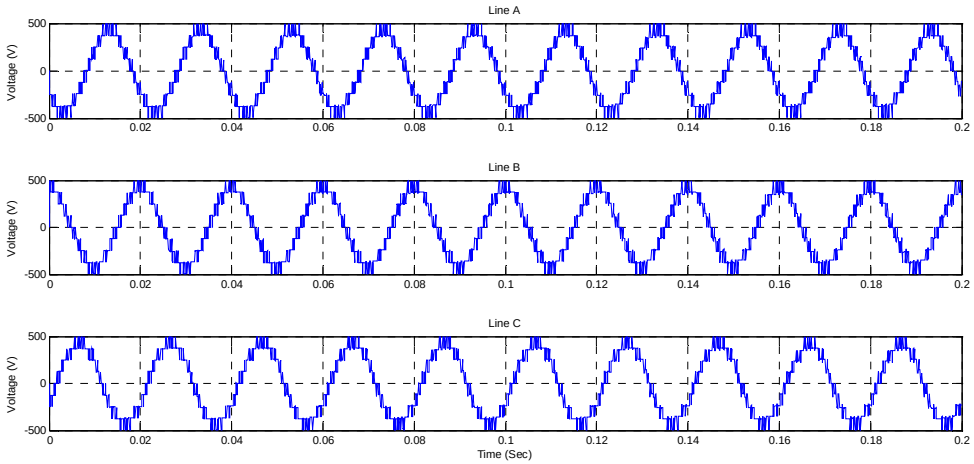

Fig. 7. Simulated line voltage by PDPWM for RL load

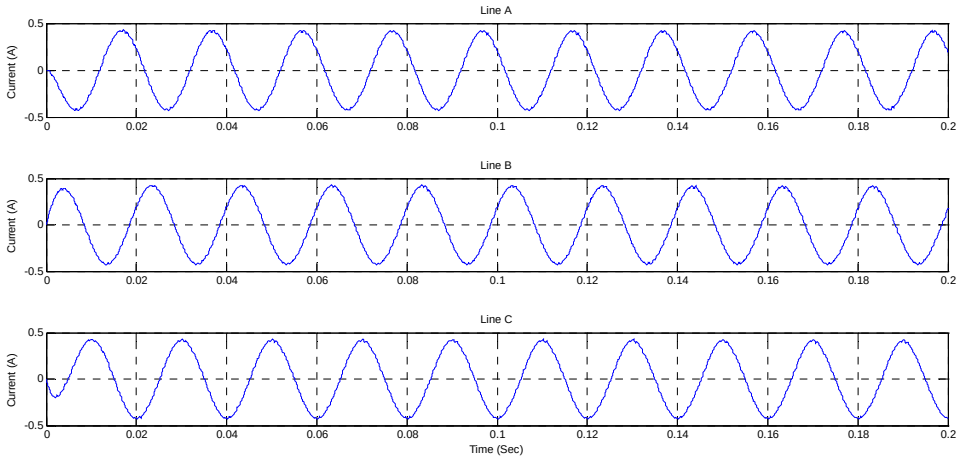

Fig. 8. Simulated line current by PDPWM for RL load

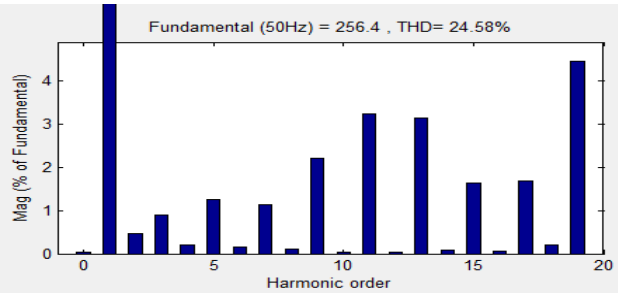

Fig. 9. Harmonic of the output phase voltage by PDPWM for RL load

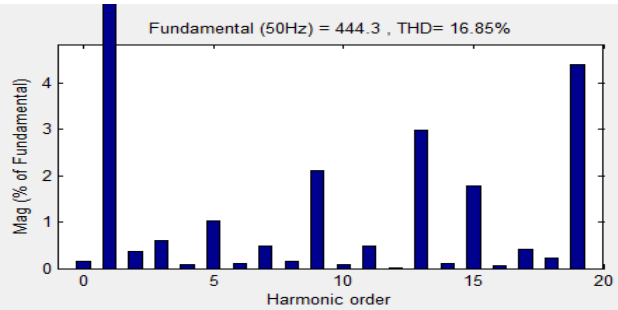

Fig. 10. Harmonic of the output line voltage by PDPWM for RL load

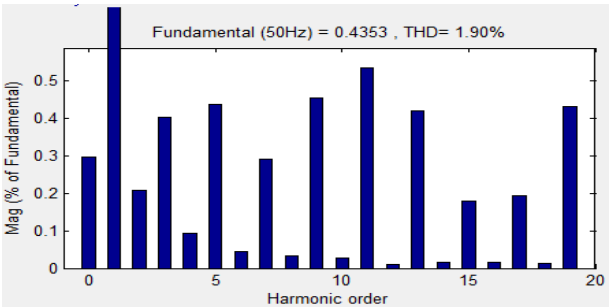

Fig. 11. Harmonic of the output line current by PDPWM for RL load

Fig 12, 13 and 14 shows the phase voltage, line voltage and line current of RL load and Fig. 15, 16 and 17 shows the harmonic spectrum of the phase voltage, line voltage and line current for RL load and it shows THD for phase voltage is 24.25%, line voltage is 18.44% and phase current 1.89%.

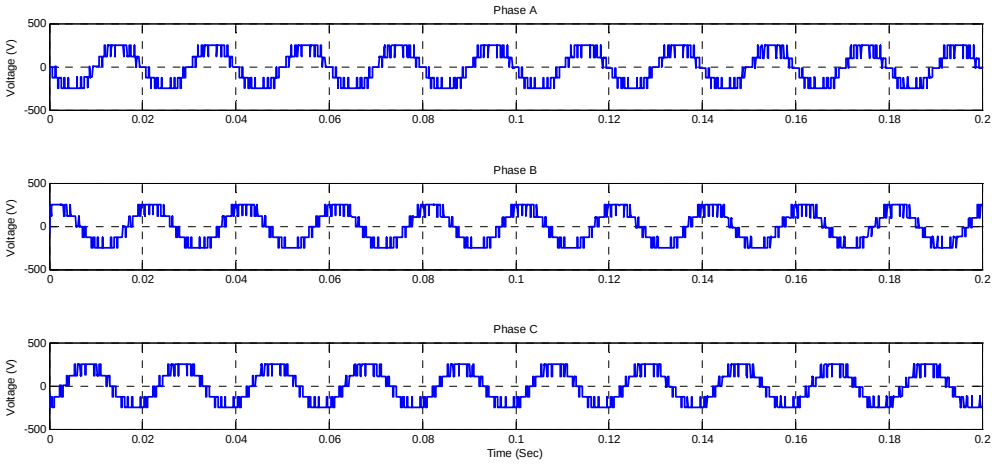

Fig. 12. Simulated phase voltage by PODPWM for RL load

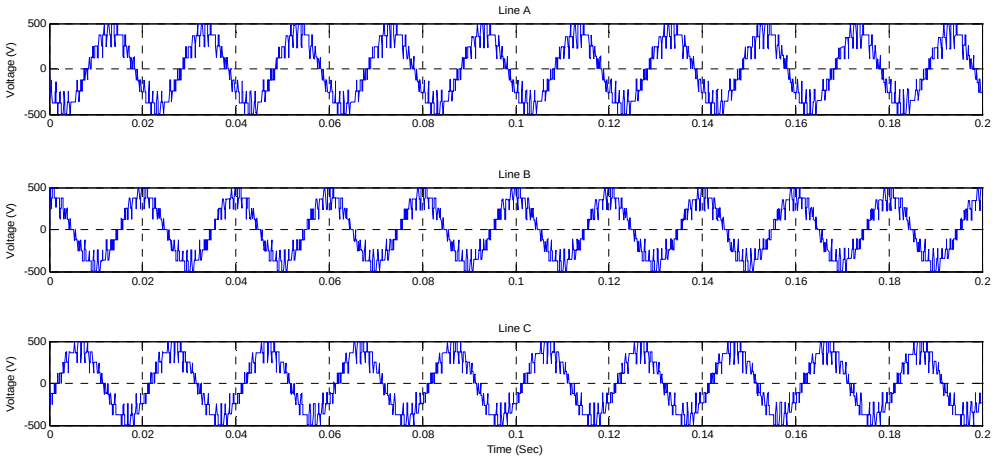

Fig. 13 Simulated line voltage by PODPWM for RL load

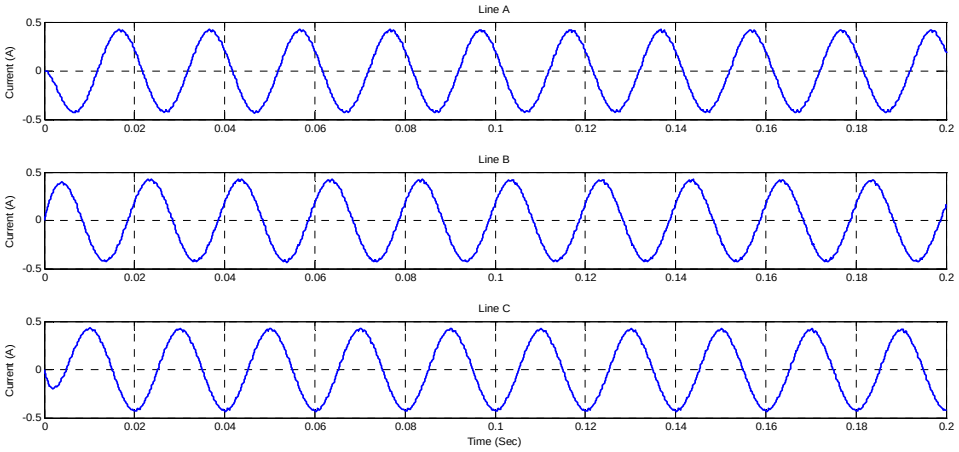

Fig. 14. Simulated line current by PODPWM for RL load

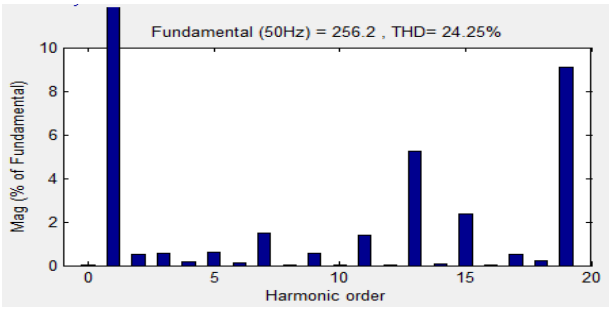

Fig. 15. Harmonic of the output phase voltage by PODPWM for RL load

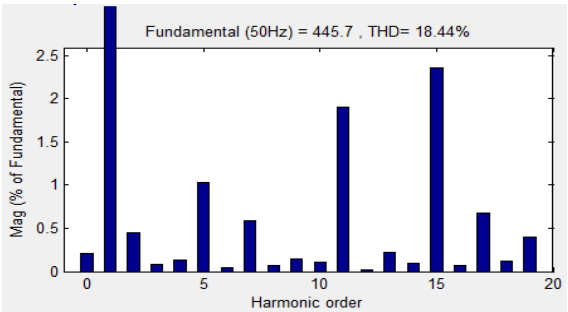

Fig. 16. Harmonic of the output line voltage by PODPWM for RL load

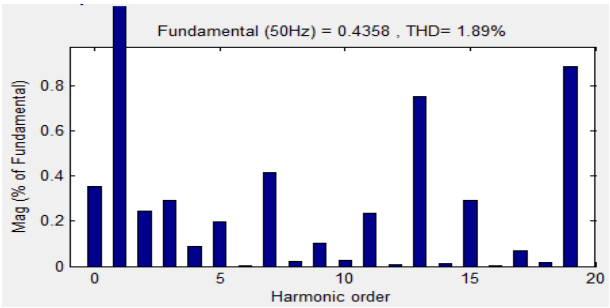

Fig. 17. Harmonic of the output line current by PODPWM for RL load

The load phase voltage, load line voltage and load line current employing APODPWM for MMC-DSCC is shown in the Fig. 18, 19 and 20. The harmonic analysis of the phase voltage, line voltage and line current for RL load is shown in the Fig. 21, 22, and 23. The THD value obtained for phase voltage is 25.28%, line voltage is 24.25% and line current is 1.97%.

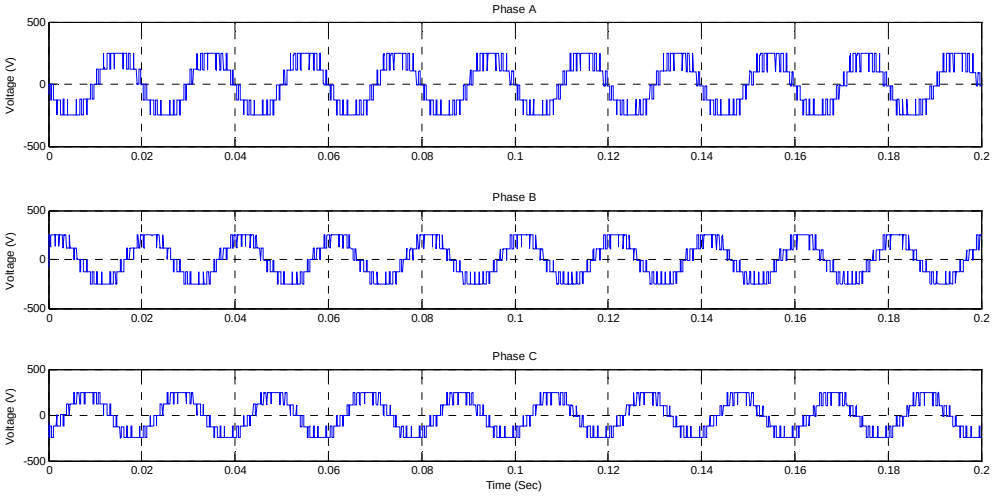

Fig. 18. Simulated phase voltage by APODPWM for RL load

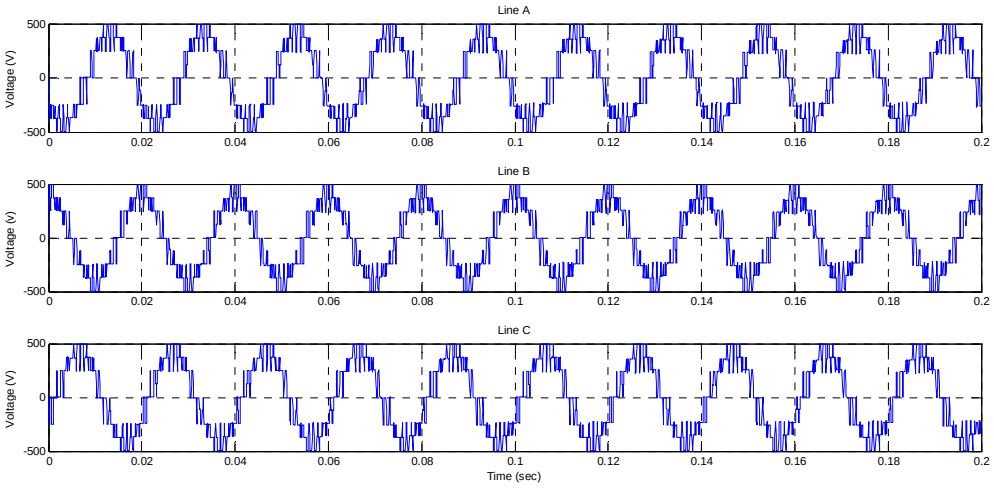

Fig. 19. Simulated line voltage by APODPWM for RL load

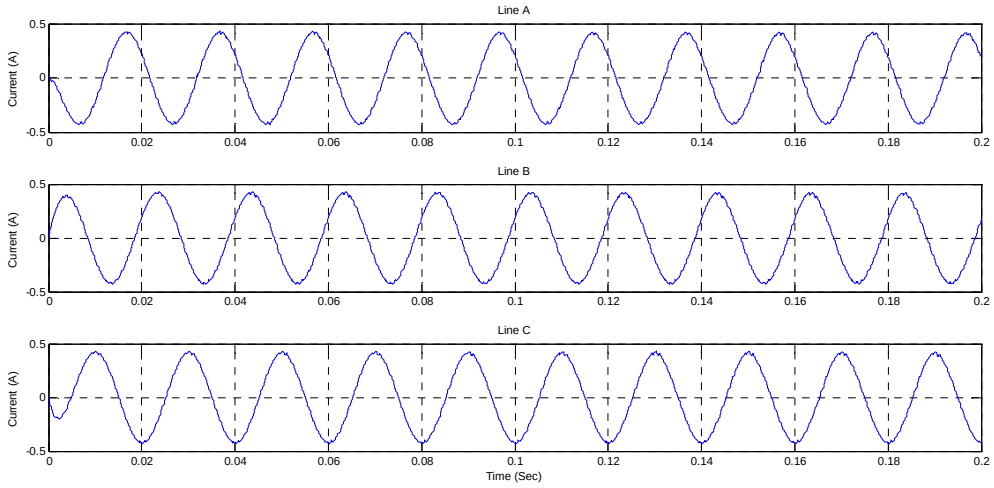

Fig. 20. Simulated line current by APODPWM for RL load

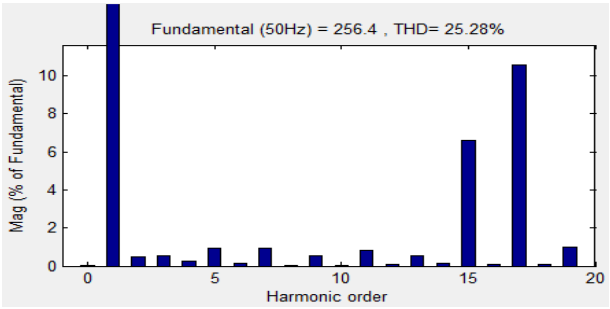

Fig. 21. Harmonic of the output phase voltage by APODPWM for RL load

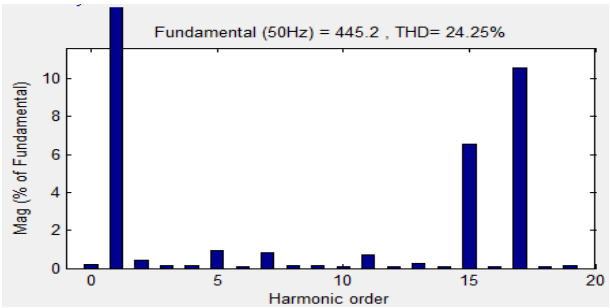

Fig. 22. Harmonic of the output line voltage by APODPWM for RL load

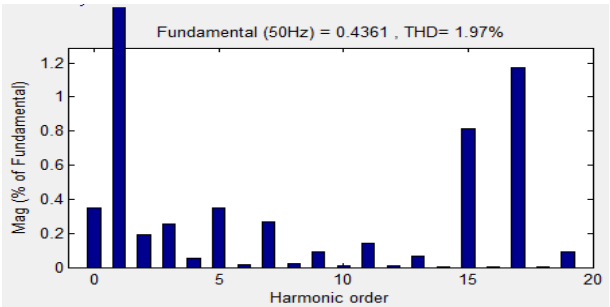

Fig. 23. Harmonic of the output line current by APODPWM for RL load

Fig. 24, 25 and 26 is the phase voltage, line voltage and line current of MMC-DSCC employing PSPWM strategy for RL load. The harmonic spectrum of the phase voltage, line voltage and line current for RL load is shown in the Fig. 27, 28 and 29 and the THD for phase voltage is 24.16%, line voltage is 23.47% and line current is 1.94%.

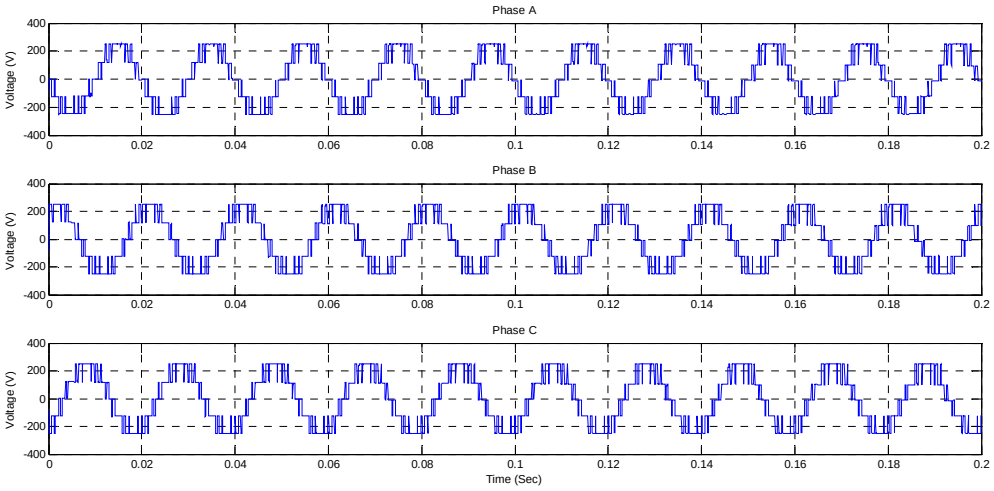

Fig. 24. Simulated phase voltage by PSPWM for RL load

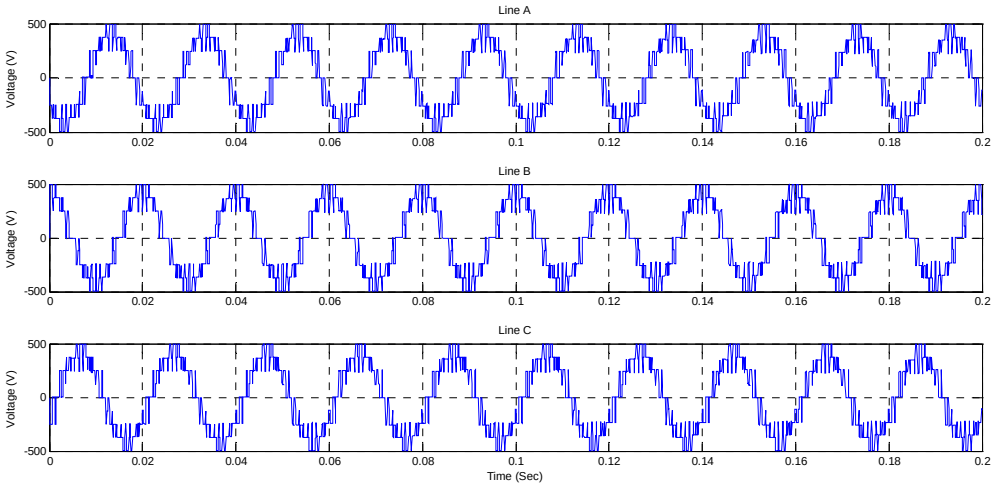

Fig. 25. Simulated line voltage by PSPWM for RL load

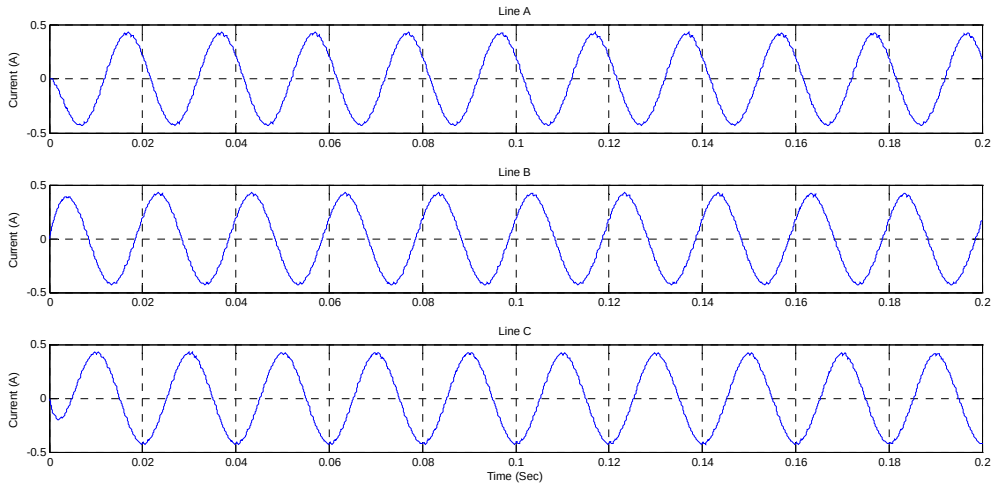

Fig. 26. Simulated line current by PSPWM for RL load

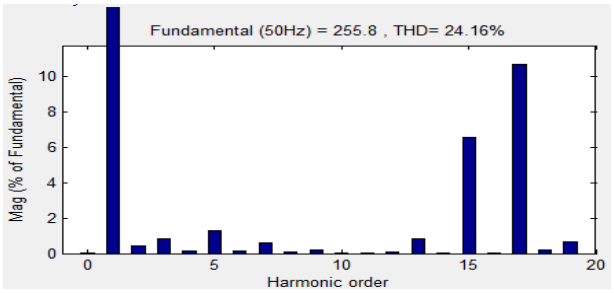

Fig. 27. Harmonic of the output phase voltage by PSPWM for RL load

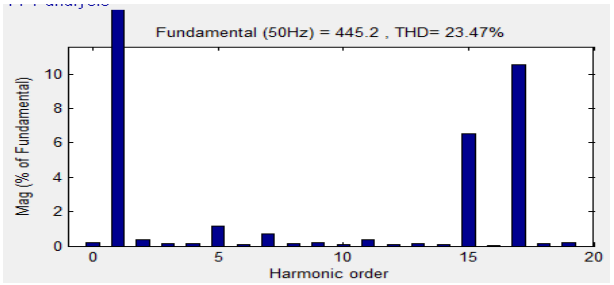

Fig. 28. Harmonic of the output line voltage by PSPWM for RL load

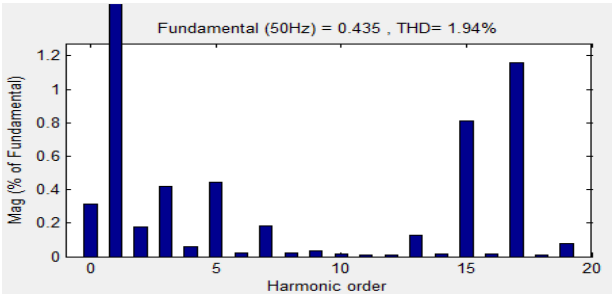

Fig. 29. Harmonic of the output line current by PSPWM for RL load

The comparison between PDPWM, PODPWM, APODPWM and PSPWM is shown in Table IV which clearly shows PDPWM strategy provides the better output phase voltage for different modulation indices. The normalized phase voltage for different modulation indices comparison is shown in Fig. 30.

TABLE IV
Phase voltage for different m_a

m_a	PD	POD	APOD	PS
0.6	147.3	146.9	145.5	145.9
0.7	170.7	170.8	171.3	170.7
0.8	196.4	196.8	196.1	196.6
0.9	221.5	221.8	221.6	221.8
1	247.2	246.2	246.9	247.5
1.05	256.2	256.1	256.4	256.4
AVERAGE	206.6	206.4	206.3	206.5

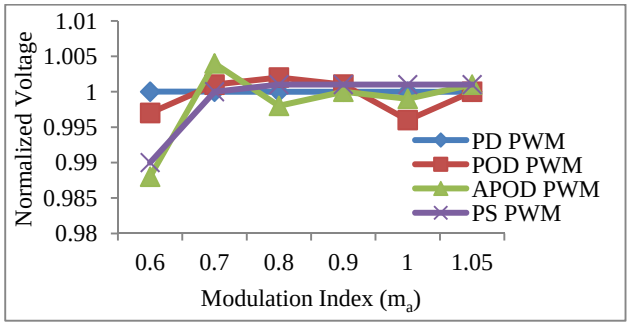

Fig. 30. Normalized phase voltage for different m_a

Table V shows that PDPWM strategy provides the better output line voltage for different modulation indices when compared to other PWM strategies and the normalized line voltage obtained for different modulation indices for PDPWM, PODPWM, APODPWM and PSPWM is shown in Fig. 31.

TABLE V
Line voltage for different m_a

m_a	PD	POD	APOD	PS
0.6	255.4	255.3	254.1	254.4
0.7	298.6	298.7	298.4	297.7
0.8	342.9	341.7	341.6	342.4
0.9	386.2	384.8	385.4	385.8
1	429.5	429.8	429.4	429.9
1.05	444.5	445.1	445.2	445.4
AVERAGE	359.5	359.2	359.0	359.3

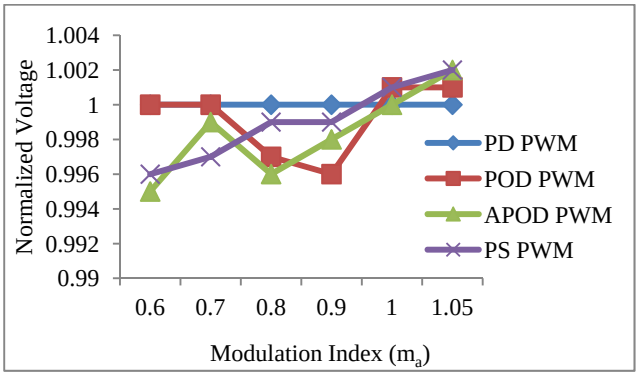

Fig. 31. Normalized line voltage for different m_a

The RMS line voltage for different modulation indices of MMC-DSCC employing PDPWM, PODPWM, APODPWM and PSPWM for RL load is shown in Table VI and the normalized output RMS line voltage for different modulation indices is shown in Fig. 32. It is observed that PDPWM strategy is the method which provides the better RMS output line voltage when compared to other PWM strategies.

TABLE VI
RMS value of line voltage for different m_a

m_a	PD	POD	APOD	PS
0.6	128.9	129.6	123.6	121.3
0.7	178.9	177.7	170.2	165.7
0.8	218.3	217.5	213.8	210.3
0.9	255.2	254.7	253.8	250.9
1	290.3	289.7	285.3	286.7
1.05	303.5	302.1	297.4	299.4
AVERAGE	229.2	228.6	224.0	222.4

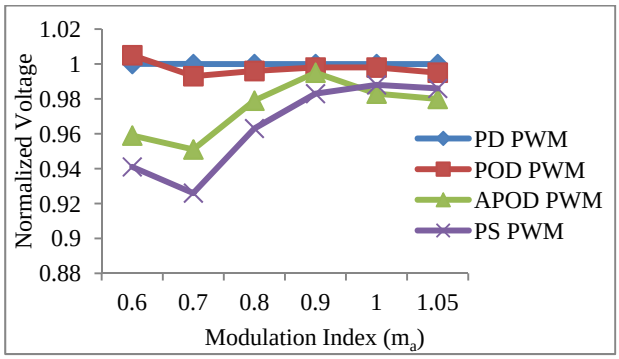

Fig. 32. RMS value of line voltage for different m_a

Table VII shows that PDPWM strategy provides the better output line current for different modulation indices, compared to PDPWM, PODPWM, APODPWM and PSPWM. Also the normalized output line current for different modulation indices is shown in Fig. 33.

TABLE VII
Line current for different m_a

m_a	PD	POD	APOD	PS
0.6	0.2516	0.2514	0.2494	0.2498
0.7	0.2925	0.2916	0.2927	0.2920
0.8	0.3356	0.3354	0.3347	0.3350
0.9	0.3773	0.3757	0.3771	0.3772
1	0.4207	0.4191	0.4199	0.4208
1.05	0.4353	0.4359	0.4361	0.4369
AVERAGE	0.3522	0.3515	0.3517	0.3520

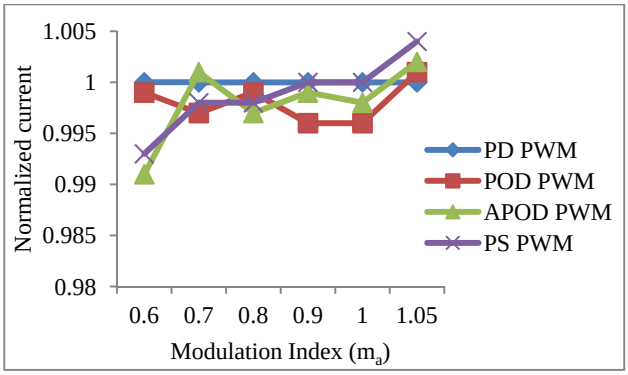

Fig. 33. Normalized line current for different m_a

The comparison between PDPWM, PODPWM, APODPWM and PSPWM is shown in Table VIII which clearly shows PDPWM strategy provides the output phase voltage with low harmonic distortion for different modulation indices. The normalized percentage THD for different modulation indices comparison is shown in Fig. 34.

TABLE VIII
% THD of Phase voltage for different m_a

m_a	PD	POD	APOD	PS
0.6	44.12	44.10	46.4	43.75
0.7	40.35	42.48	43.17	42.35
0.8	38.70	38.28	39.90	38.05
0.9	33.83	33.13	33.40	33.80
1	26.10	26.71	27.24	26.61
1.05	24.13	24.23	25.28	24.17
AVERAGE	34.54	34.82	35.90	34.79

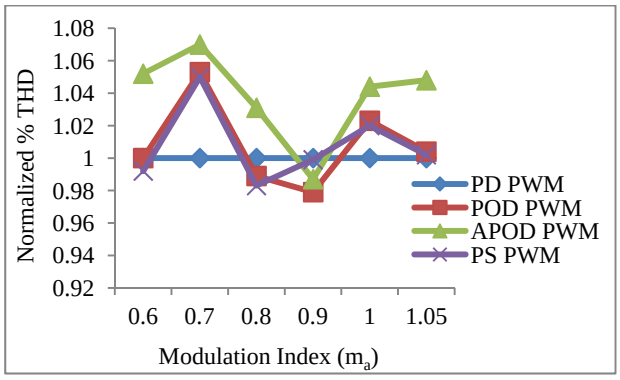

Fig. 34. % THD of Phase voltage for different m_a

Table IX shows the values of THD obtained for MMC-DSCC employing PDPWM, PODPWM, APODPWM and PSPWM and it shows that PDPWM strategy provides the output line voltage with low harmonic distortion for different modulation indices. The normalized percentage THD for different modulation indices is shown in Fig. 35.

TABLE IX
%THD of Line voltage for different m_a

m_a	PD	POD	APOD	PS
0.6	25.39	38.54	25.64	25.09
0.7	23.25	39.55	28.68	28.4
0.8	20.98	36.05	30.1	30.24
0.9	18.01	30.38	28.83	29.26
1	17.63	21.57	25.92	25.51
1.05	16.86	18.39	24.25	23.46
AVERAGE	20.35	30.75	27.24	26.99

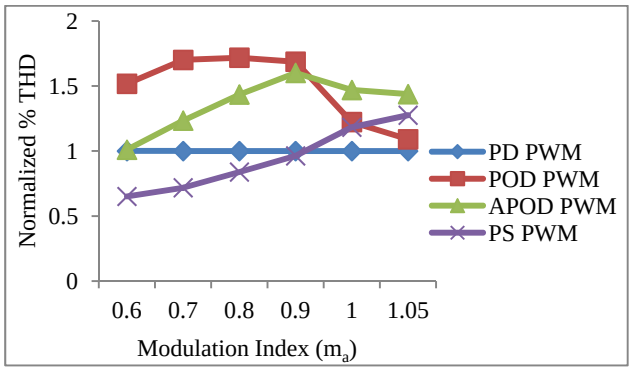

Fig. 35. % THD of line voltage for different m_a

The % THD for different modulation indices of PDPWM is less when compared to PODPWM, APODPWM and PSPWM as given in Table X. The normalized percentage of THD for different modulation indices is also shown in Fig. 36.

TABLE X
% THD of Line current for different m_a

m_a	PD	POD	APOD	PS
0.6	2.97	3.04	3.07	3.1
0.7	2.96	3.01	3.06	3.08
0.8	2.87	2.91	2.94	2.91
0.9	2.42	2.5	2.5	2.51
1	1.95	2.03	2.05	1.99
1.05	1.9	1.91	1.97	1.94
AVERAGE	2.51	2.57	2.6	2.59

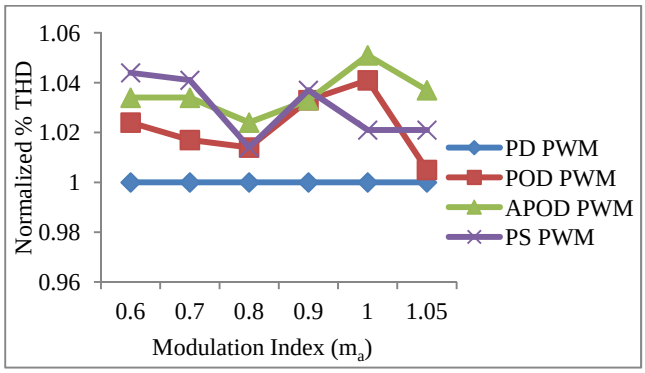

Fig. 36. % THD of line current for different m_a

V. CONCLUSION

In this paper, three phase five-level modular multilevel inverter based on double star chopper cells configuration employing PDPWM, PODPWM, APODPWM and PSPWM multicarrier PWM strategies with RL load is simulated using Matlab/Simulink software. The detailed comparison is done for the MMC-DSCC employing multicarrier PWM strategies based on the load phase voltage, load line voltage, load line current, V_{RMS} of load voltage and Total Harmonic Distortion. The PDPWM strategy produces RMS line voltage of 255.2V, THD of line voltage 18.01% and THD of line current 2.42% for the modulation index of 0.9. Thus PDPWM strategy is the best method providing the better RMS load voltage with low THD compared to other PWM strategies.

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