Design of Asynchronous Sequential Circuits using Reversible Logic Gates

Bahram Dehghan
Islamic Azad University, Sarvestan Branch, Department of Electrical Engineering, Sarvestan, Iran
Bahramdehghan1@gmail.com

***Abstract*— In recent literature, Reversible logic has become one of the promising arena in low power dissipating circuit design in the past few years and has found its applications in low power CMOS circuits , optical information processing and nanotechnology. The reversible circuits form the basic building block of quantum computers as all quantum operations are reversible. This paper presents asynchronous sequential circuits and circuits without hazard effect using reversible logic gates. I illustrate that we can produce AND, OR, NAND, NOR, EXOR and EXNOR outputs in one design using reversible logic gates. Also, I will evaluate the proposed circuits. The results show that reversible logic can be used to design these circuits. In this paper, the number of gates and garbage outputs is considered.**

Keyword- Asynchronous sequential circuits, Reversible circuits, Hazard effect

I. INTRODUCTION

Landauer has shown that for irreversible logic computations, each bit of information lost, produces kTln2 joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which computation is represented[1]. Bennett demonstrated that kTln2 energy dissipation would not occur, if a computation is carried out in a reversible way [2], since the amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. For irreversible logic, each bit of information lost produces kTln2 Joules of heat energy, where k is Boltzmann's constant and T is absolute temperature at which the computation is performed. For room temperature T, the amount of heat dissipated for one bit is small i.e. 2.9×10^{-21} J [3].
This heat dissipation extremely reduces the performance and lifetime of the circuits. The solution is to use revolutionary technology which enables extremely low power consumption and heat waste in computing[4].
These circuits can produce single output vector from each input vector, and conversely, there was a one-to-one mapping between input and output vectors. Therefore, an NXN reversible gate can be shown as

Iv=(I1,I2,I3,I4,……IN)
Ov=(O1,O2,O3,…….ON).

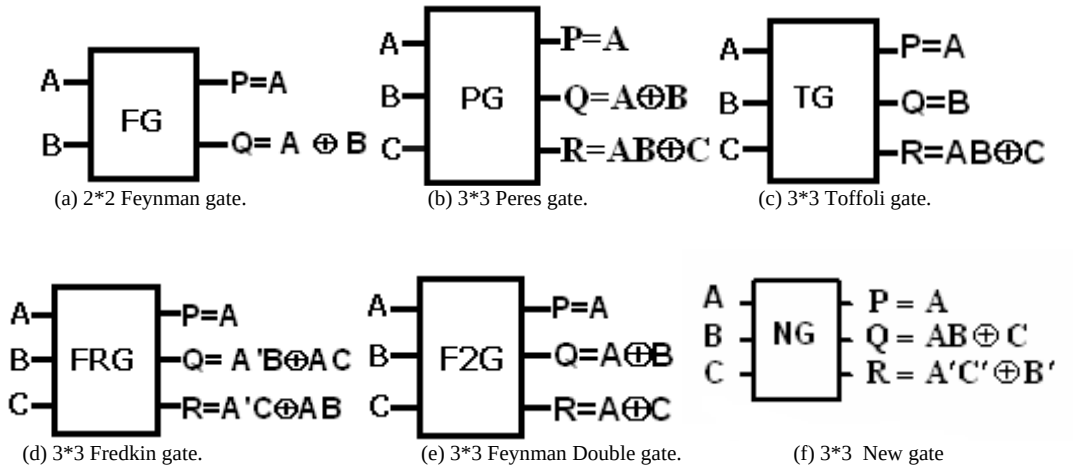
Where Iv and Ov can be shown the input and output vectors respectively. Classical logic gates are irreversible since input vector states cannot be uniquely reconstructed from the output vector states[5].
Firstly, in reversible circuit there should be no fan-out, that is, each output will be utilized only once. Secondly, for each input template there should be a unique output template.
Finally, the resulting circuit must be acyclic. Any reversible gate performs the permutation of its input patterns only and realizes the functions that are reversible. On the other hand, if a reversible gate has *k* inputs, and therefore *k* outputs, then we denominate it a *k*k* reversible gate.
Asynchronous circuits are circuits that have no global clock. Instead of using a global clock to synchronize events, asynchronous circuits use local handshaking between modules to synchronize when and where essential. There has been a revitalization of interest in the design of asynchronous circuits due to their potential benefits in performance, robustness, modularity, and decreased power consumption[6].
It will be explained further in the next sections.

II. REVERSIBLE QUANTUM GATES AND CIRCUITS

A gate is reversible if there is a separate output assignment for each separate input. Classical reversible logic gates called reversible gates are ones which act on binary digits or bits. They are implemented in various technologies such as CMOS, Optical and nanotechnology techniques. Quantum gates on the other hand, operate on qubits. A qubit is a unit of quantum information. That information is demonstrated by a state vector in a two-level quantum mechanical system which is formally equivalent to a two-dimensional vector space over the complex numbers [7].
The memory units of a classical discrete computer are usually taken as bits, two-valued classical variables. By analogy, we consider a two-valued quantum variable, called a qubit, which may be simulated by a two-level quantum system. assume the levels, or eigenstates of the quantum variable, are labeled |0> and |1>. This has a direct correspondence with the discrete states of a classical bit, 0 and 1 [8].

III. Basic Reversible Logic Gates

There exist many reversible gates in the literature. Among them 2*2 Feynman gate (FG)[4], depicted in Fig. 1a, 3*3 Peres gate (PG), depicted in Fig. 1b, 3*3 Toffoli gate (TG)[4], depicted in Fig. 1c and 3*3 Fredkin gate (FRG)[4], depicted in Fig. 1d and 3*3 Feynman Double gate(F2G) in Fig.1e and 3*3 New gate in Fig.1f have been studied extensively. Because of their simplicity and quantum realization cost there are design approaches and tools that incorporate them separately or in combination with each other[9].

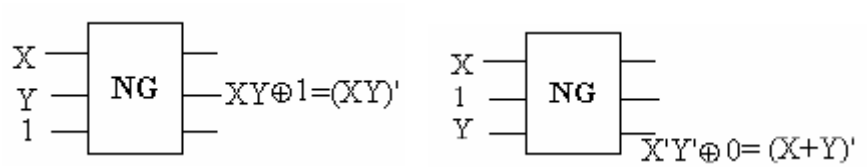


(a) 2*2 Feynman gate. (b) 3*3 Peres gate. (c) 3*3 Toffoli gate.

(d) 3*3 Fredkin gate. (e) 3*3 Feynman Double gate. (f) 3*3 New gate

Fig. 1. Some well-known reversible logic gates[9].

Figure 2.a and Figure 2.b show the implementation of the New gate as NAND and NOR functions respectively[5].



(a) (b)

Fig. 2. New Gate as (a) NAND Function (b) NOR Function.

IV. Asynchronous Circuits

Asynchronous circuits are becoming more traditional. Most commonly they occur in the interfaces and the glue logic that binds the components of a system. One proof for this is that asynchronous logic is appropriate to delay variations and components designed to function asynchronously can be more easily composed[10]. The most obvious model to use for asynchronous circuits is the same model used for synchronous circuits[11].Specifically, it is assumed that the delay in all circuit elements and wires is known, or at least bounded. Asynchronous circuits is not yet a well-established and widely-used design methodology. Asynchronous circuits are basically different; they also assume binary signals, but there is no common and discrete time. This difference gives asynchronous circuits intrinsic properties that can be extracted to advantage in the areas listed and motivated below. The interested reader may find further introduction to the mechanisms behind the advantages mentioned below in:

Low power consumption, High operating speed, Less emission of electro-magnetic noise, Better composability and modularity[10].

V. Hazards

In a synchronous circuit a clock defines when a signal is sampled. The value of the signal is only necessary near the sampling clock edge, allowing the designer to largely ignore any extraneous signal transitions. In contrast, an asynchronous circuit is constantly sampling its signals. Therefore, any extraneous transitions (“hazards”) may cause incorrect results, and thus must be avoided.

Hazards may be inherent in a Boolean function or arise because of how it is implemented. For example, if both inputs to an XOR are allowed to change simultaneously, there is an inevitable hazard since one input may change before the other. Hence, slight differences in signal arrival times will cause the circuit to produce spurious transitions. Asynchronous circuits either do not utilize elements with inevitable hazards, or do not permit the hazardous situations to occur[12].

VI. Reversible Equivalent Gates Used For Designing Sequential Circuits

The reversible gates utilized to design the conventional logic are so chosen to minimize the number of reversible gates used and garbage outputs generated.

The classical logic gates such as AND, OR, NAND, NOR, EXOR and EXNOR are not reversible, but we can generate these outputs using reversible logic gates. for example, All mentioned outputs can be achieved with the following circuit. Table I shows the evaluation of the mentioned circuit.

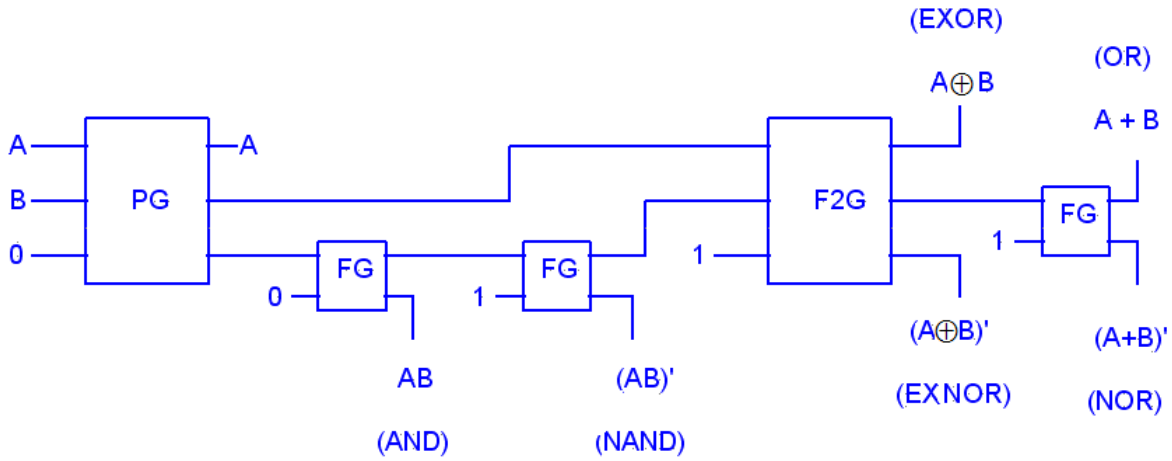


Fig. 3. Generate all well-known classical logic gates.

TABLE I. Evaluation Of The Proposed Circuit

	No of gates	Garbage Outputs
Proposed Circuit	5	1
Existing One	None in literature	None in literature

In the existing literature, designs of reversible sequential circuits are offered that are improved for the number of the garbage outputs and reversible gates. First, I introduce a circuit without Hazard in Figure 4.

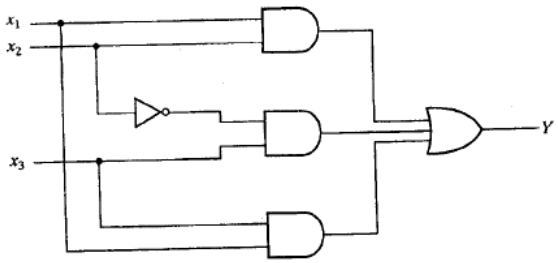


Figure 4. Circuit without hazard

Figure 5 shows the circuit without hazard which is designed from the reversible equivalent gates.

The proposed circuit of the Figure 5 is evaluated in terms of number of reversible gates used and garbage outputs produced. Table-II shows the evaluation of the proposed circuit.

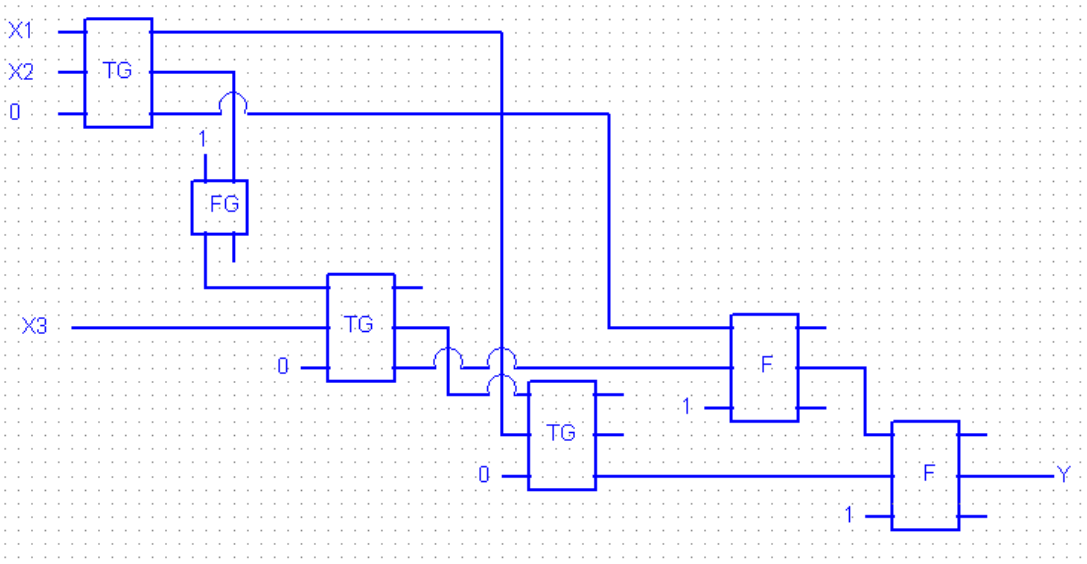


Fig. 5. Circuit without hazard using reversible logic gates

TABLE II. EALUATION OF THE PROPOSED CIRCUIT

	No of gates	Garbage Outputs
Proposed Circuit	6	8
Existing One	None in literature	None in literature

A method for preventing static Hazard in asynchronous sequential circuits is SR latch circuit. This function is implemented with two NAND gates.
if Q= 1 then the output Q' is equal to 0. If two of the three input NAND is temporary 1, then the output of NAND gate will be equal to 0; because Q' is kept at zero. Hence, hazard effect is not in the output.
Figure.6 can be used for building asynchronous sequential circuits without hazard. Figure.7 shows the Circuit Implementation by latch using reversible logic gates. Table-III shows the evaluation of the proposed circuit.

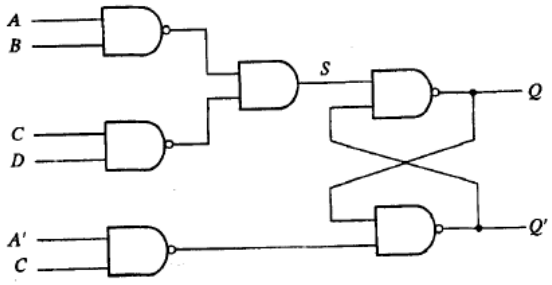


Fig. 6. implementation using latch

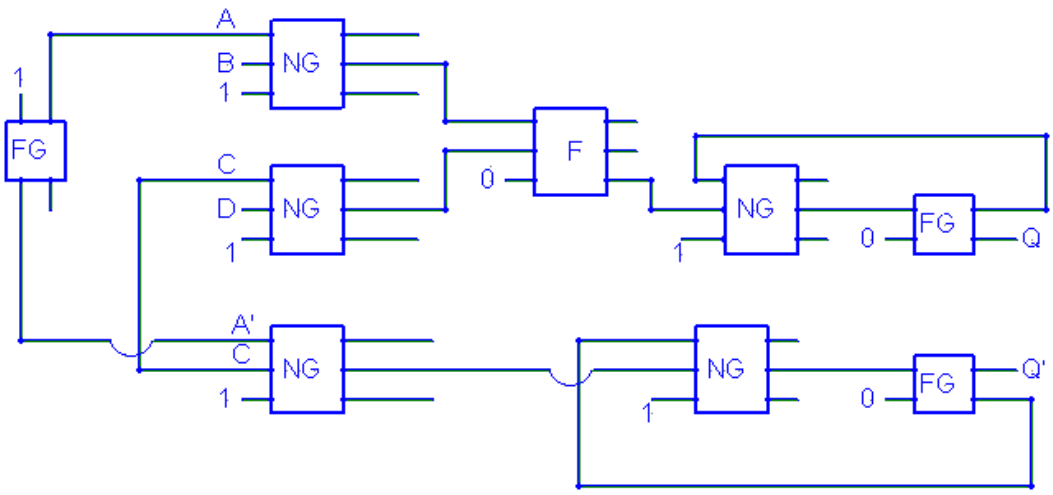


Fig.7. The Circuit Implementation by latch using reversible logic gates.

TABLE III. EVALUATION OF THE PROPOSED CIRCUIT

	No of gates	Garbage Outputs
Proposed Circuit	9	13
Existing One	None in literature	None in literature

Although most digital circuits are designed as synchronous, but sometimes asynchronous circuits be used. One sample of T flip-flop was shown in figure 8.

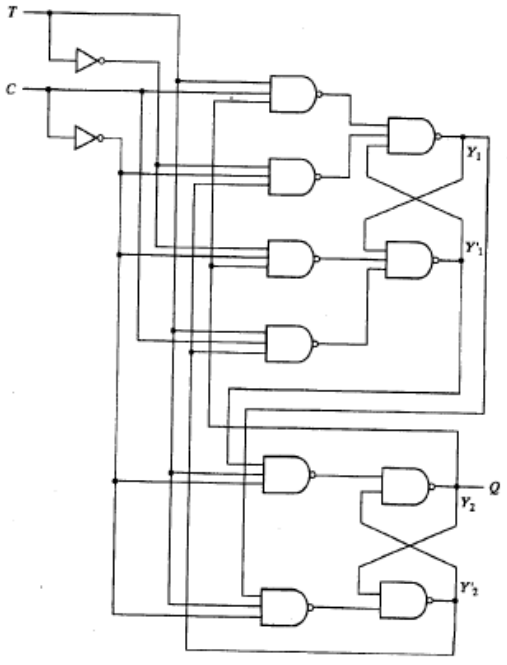


Fig.8. T flip flop sensitive to falling edge clock

Figure.9 shows the Circuit Implementation using reversible logic gates. Table-IV shows the evaluation of the proposed circuit.

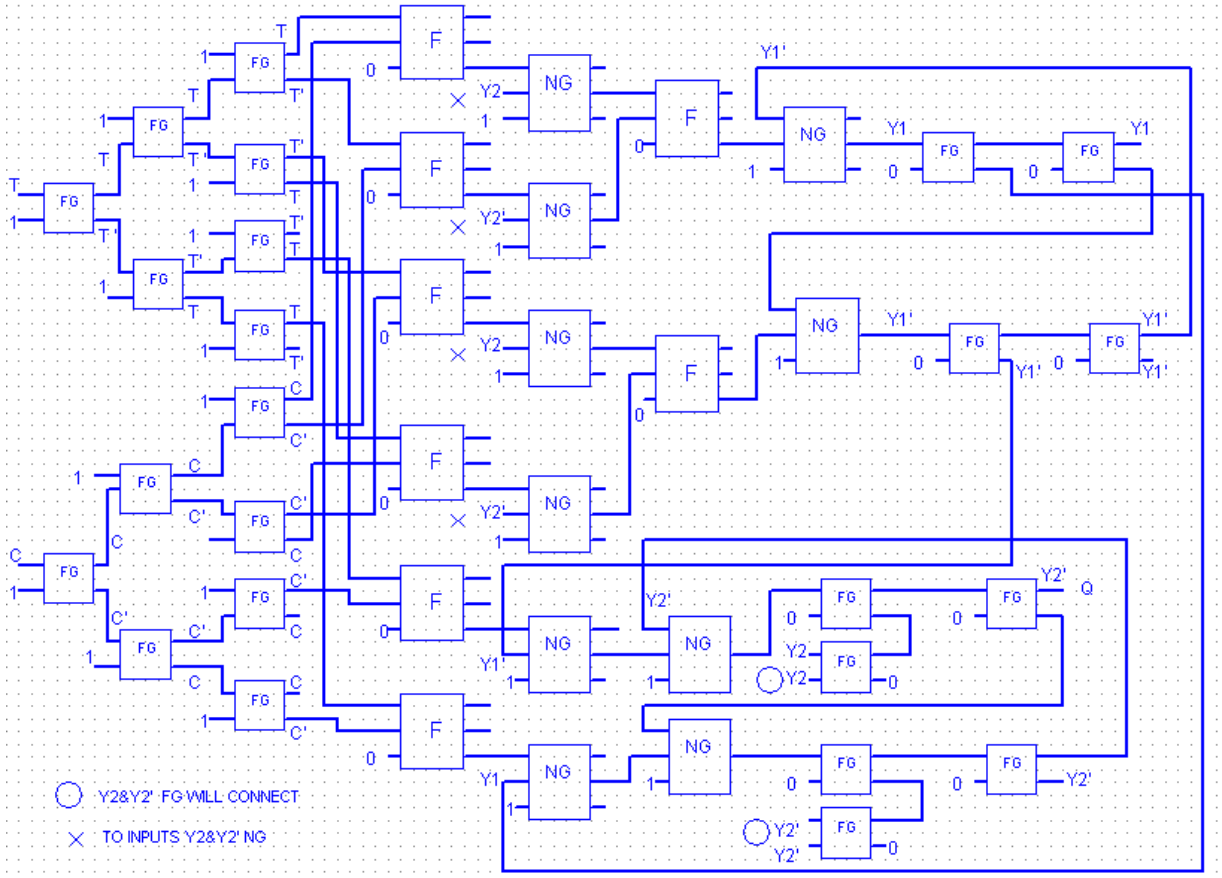


Fig.9. T flip flop sensitive to falling edge clock using reversible logic gates.

TABLE IV. EVALUATION OF THE PROPOSED CIRCUIT

	No of gates	Garbage Outputs
Proposed Circuit	42	40
Existing One	None in literature	None in literature

VII. CONCLUSION

Reversible logic can be employed to design information lossless circuits, and therefore, has the potential of reducing power consumption dramatically [13]. This paper presents a design of asynchronous sequential circuits using reversible logic gates. Novel Reversible Asynchronous circuits are designed using Feynman Gate, New Gate,Toffoli Gate and Fredkin Gate. In this paper, Asynchronous sequential circuits, the number of gates and garbage outputs were studied. Classic gates with 3 inputs will require more than 2 inputs of reversible logic gates. Most of the digital circuits are designed as synchronous, but sometimes we need asynchronous circuits. Although the design of asynchronous sequential circuits is more complicated, but using reversible logic acquires less garbage outputs. In recent studies, design of asynchronous sequential circuits using reversible logic gates has been considered less than the synchronous sequential circuits. For the first time, these designs has been done.

REFRENCES

[1] R. Landauer, “Irreversibility and Heat Generation in the Computational Process”, IBM Journal of Research and Development, 5, pp. 183-191, 1961.
[2] C.H. Bennett , “Logical Reversibility of Computation”, IBM J. Research and Development, pp. 525-532, November 1973.
[3] Dmitri Maslov, “Reversible logic synthesis”, University of New Brunswick, September 2003.
[4] X. Susan Christina and M.Sangeetha Justine, “Realization of BCD adder using Reversible Logic”, International Journal of Computer Theory and Engineering, Vol.2, No.3, June, 2010.
[5] H. Thapliyal and H.R. Arabnia,” Reversible Programmable Logic Array (RPLA) using Fredkin & Feynman Gates for Industrial Electronics and Applications” International Conference on Embedded Systems and Applications(ESA'06),LasVegas, U.S.A, June 2006

[6] Eric Robert Peskin," Protocol Selection, Implementation, And Analysis For Asynchronous Circuits", School of computing the university of Utah, August 2002
[7] Phillip Kaye, Raymond Laflamme, Michele Mosca "An Introduction to Quantum Computing" Oxford University Press Jan 2007eBook-LinG, ISBN 0-19-857000-7.
[8] Ashok Muthukrishnan," Classical and Quantum Logic Gates", Rochester Center for Quantum Information (RCQI),Sep 1999
[9] http://arxiv.org/ftp/arxiv/papers/1008/1008.3340.pdf
[10] Jens Sparsø," Asynchronous Circuit Design", Technical University of Denmark 2006. http://www2.imm.dtu.dk/~jsp
[11] Scott Hauck," Asynchronous Design Methodologies", *Proceedings of the IEEE*, Vol. 83, No. 1, pp. 69-93, January, 1995.
[12] Scott Hauck, Steven Burns, Gaetano Borriello, Carl Ebeling, " An FPGA For Implementing Asynchronous Circuits"**,** *IEEE Design & Test of Computers*, Vol. 11, No. 3, pp. 60-69, Fall, 1994.
[13] Hafizur Rahaman, Dipak K. Kole, Debesh K. Das, Bhargab B. Bhattacharya," On the Detection of Missing-Gate Faults in Reversible Circuits by a Universal Test Set", 21st International Conference on VLSI Design, IEEE 2008.