Design of Low Noise 16-bit CMOS Digitally Controlled Oscillator

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***Abstract*—In this paper, a new differential delay cell is proposed and 16-bit Digital Controlled Oscillator (DCO) based on proposed delay cell is designed. The 16-bit DCO consist of 4-stages differential delay cell in ring structure and a digital control scheme has been used to improved noise characteristics. The structure of the DCO utilizes dual delay path techniques to achieve high oscillation frequency and a wide tuning range. The DCO circuit has been simulated in SPICE with 0.5µm technology operating with supply voltage of 5V. DCO achieved a controllable frequency range of [1.7324-4.8649] GHz with a tuning range of 3.1325GHz (≈64%). The measured output noise is -161.2dB/Hz and the total harmonic distortion have been found 75.4865dB with 6666H control word. The phase noise in proposed DCO design is -179.4dB/Hz at a frequency of 1.7324GHz.**

Keyword- CMOS, digital controlled oscillator, dual delay path technique, PLL, voltage controlled oscillator.

I. INTRODUCTION

With the growing density of component in submicron technology, the need for high operating speed and low power consumption is increasing day by day. In order to support such high speed operation of electronic systems, the clock generation and data recovery system must operate at high frequencies.

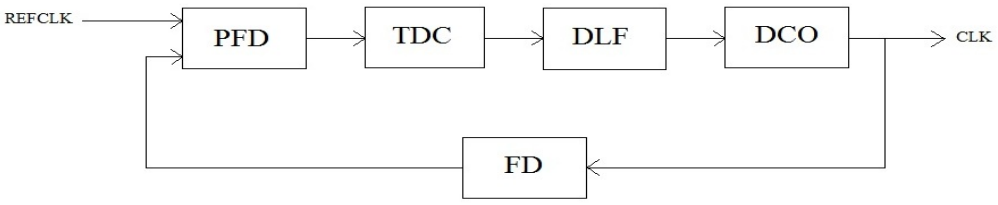

Fig. 1. Block diagram of ADPLL

Digital phase locked loop is widely used circuit for clock generation and data recovery (CDR) in modern communication systems. All digital phase locked loop (ADPLL) has replaced the conventional PLL circuits and are easier to port into a different process technology. These ADPLL have short lock time. As shown in Fig. 1 the ADPLL consists of five blocks: a phase frequency detector (PFD), a time to digital convertor (TDC), a digital loop filter (DLF), a DCO and a frequency divider (FD). Digital controlled oscillator (DCO) is most critical block in ADPLL system. To implement a wide frequency range ADPLL, the DCO must have a wide oscillation frequency range. Digital controlled oscillators (DCO's) have been used in frequency synthesis and clock recovery due to accurate frequency locking and stability in operation as compared to analog counter parts. Frequency variation is achieved either through charging MOSFET driving strength or fine tuning capacitive loading [2]. The design topologies of most DCO's are based on inverter based ring oscillators [3], [4]. These oscillators suffer from the phase noise and their effectiveness is reduced in communication system. A 3.3 GHz LC-based DCO circuit based on incrementally sized and matched varactor banks has been reported [5]. It achieves both the higher frequency resolution and a large frequency tuning range with a small differential nonlinearity. A 900 MHz, voltage controlled oscillator (VCO) in a 0.6µm CMOS technology using a differential delay cell has been reported in [6]. It generates 450 MHz (≈50%) tuning range operating in the range of 750 MHz to 1.2 GHz. DCO circuits with XNOR gates also have reported in [7]. Many of these circuits suffer from small tuning range and limited oscillation frequency

In this paper, 16-bit DCO designs using differential delay cell 0.5µm CMOS process technology have been reported. These designs uses the differential delay cell with 16-bit digital control word and provides controllable

frequency range of [1.7324-4.8649] GHz with a tuning range of 3.1325 GHz (≈64%). The paper is organized as: Section II, discuss the detail circuit operation of proposed differential delay cell and dual delay path technique. In section III the results of DCO have been obtained and compared. Finally conclusions have been presented in section IV.

II. DCO CIRCUITS

A. DCO Design with Differential Delay Cell

Fig. 2 shows a four input differential delay cell. The cell can be divided into three sub-blocks: the differential input block, the CMOS latch block and the acceleration block. The differential input block is composed of two NMOS transistors M5 and M6 and it is used to accept the signal which comes from the digital loop filter. A pair of PMOS load transistor M1 and M4 is used to constitute a CMOS latch block. The strength of latch block is controlled by the digital bits of pass transistor band implemented by two sets of parallel MOSFET switches for the two feedback path by a 16-bit control register. The CMOS latch block is major part in the delay cell and its strength will affect the oscillation frequency. A pair of PMOS transistor M2 and M3 is added to PMOS load of the delay cell which acts as an acceleration block. Acceleration blocks speed up the oscillation frequency and reduce the noise.

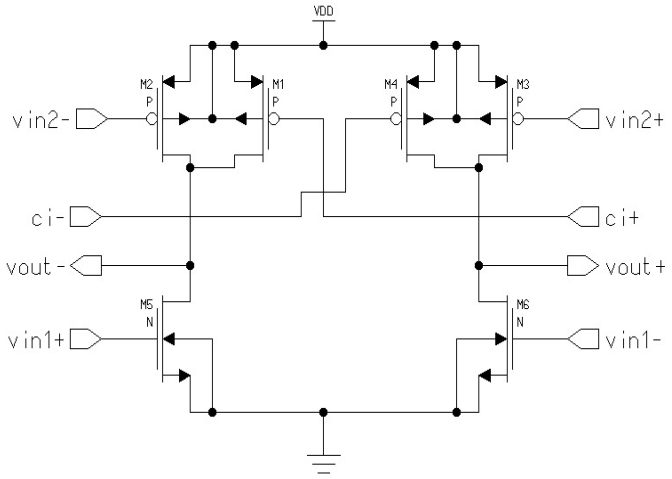

Fig. 2. The four input differential delay latch cell

B. DCO Structure with Dual Delay Paths

In the conventional ring oscillator, the oscillation frequency is determined as: f_{osc} = 1/2Nt. Here f_{osc} is the oscillation frequency. N is the number of stages and t is the unit delay time of each delay cell. Therefore the frequency of oscillator is depends on delay time of each delay element. The delay time cannot be smaller than that of a single inverter, so the maximum frequency of the oscillator is limited by the delay time of the basic inverter delay cell. To overcome this frequency limitation problem, skewed delay scheme is used [6]. Fig. 3 shows the DCO structure with dual delay path technique. Dual delay path scheme means in the same DCO, both skewed delay paths and normal delay paths existed. The DCO uses the even stage skewed dual delay path scheme which enable higher operating frequency and wider tuning range. The skewed signal is taken from outputs of two stages before the current delay cell. This skewed signal turn on the PMOS prematurely during output transition. This compensate for the performance of PMOS which is usually slower than NMOS. The output node of the delay cell will be pre charged by the PMOS transistor M3 or M4. As a result, the output node can charge to high voltage faster and can obtain higher operating frequency. This technique reduced the rise time of the output signal and contributes to reducing the phase noise of the overall oscillation [6], [9]. When the skewed signal increases, the speed and power consumption also increase. Further increases skewed signal, reduced the speed of the DCO due to direct path formation between power supply and ground. For practical applications, skewed should be small compared with the total period to get higher speeds with allowable power consumption penalty. In Fig. 3, the normal delay paths are shown by thick lines and skewed path are represented as thin lines.

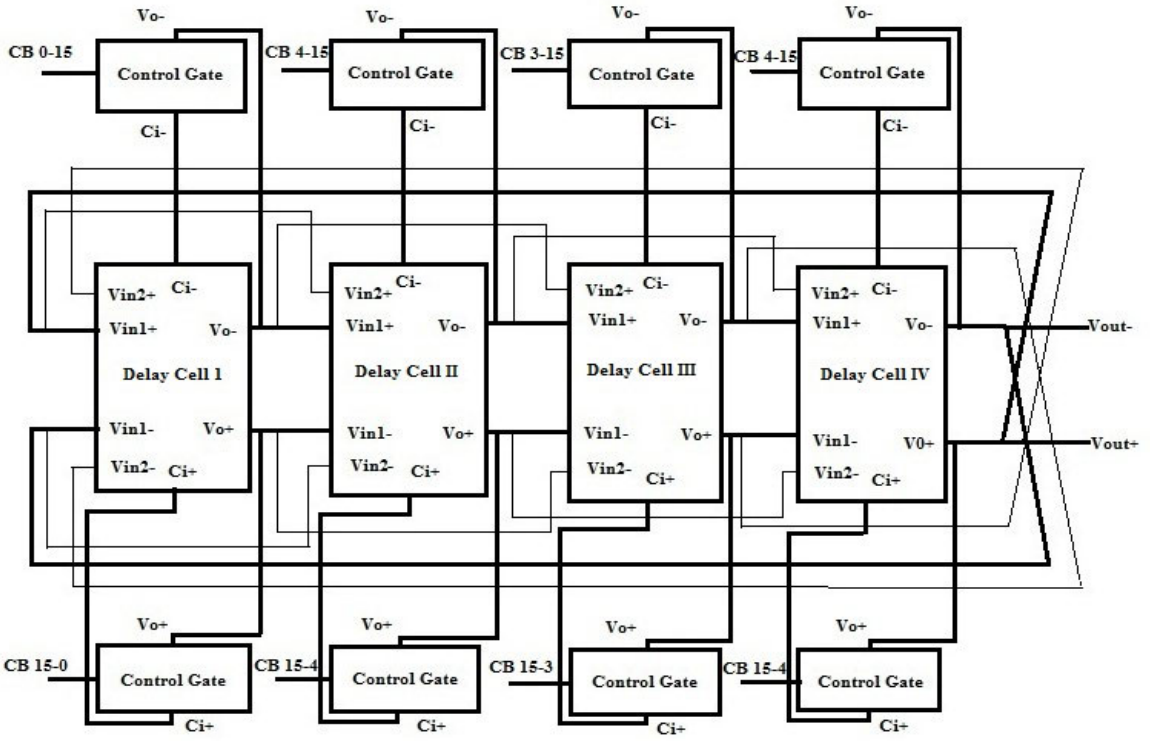

Fig. 3. DCO structure with dual delay paths scheme

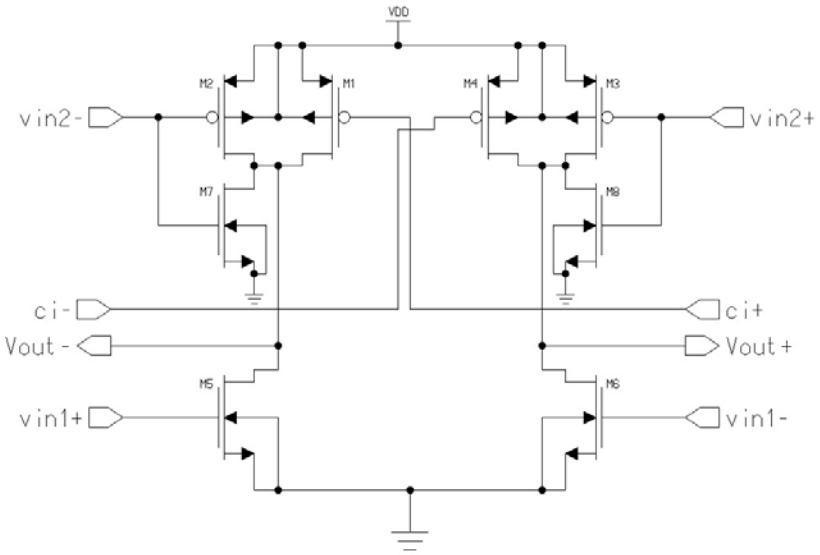

Fig. 4. The proposed four input differential delay latch cell

Fig. 4 shows the proposed delay cell for digitally controlled oscillator (DCO). In the proposed delay cell, a pair of NMOS M7 and M8 is added to the acceleration block. These transistors used to pre-discharge the output nodes. Consequently the acceleration block can reduce the rise time and fall time of the output signal. Due to the effect of pre-discharge, the oscillation frequency of new delay cell is higher than conventional delay cell. Fig. 5 shows the 16-bit DCO design using a 4-stage proposed differential delay cell.

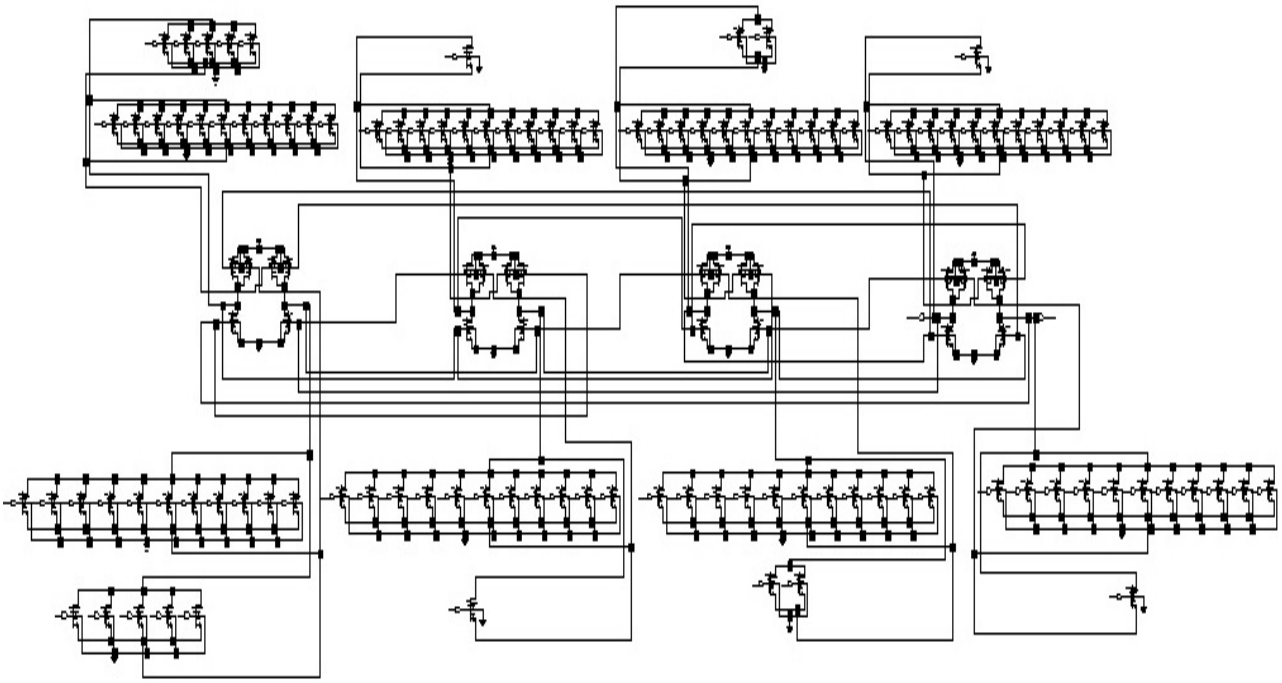

Fig. 3. A 16-bit digital controlled oscillator using a 4-stage proposed differential delay cell

III. RESULTS AND DISCUSSIONS

All The 16-bit digital controlled oscillator (DCO) has been designed and simulated using SPICE in 0.5μm CMOS technology with supply voltage of 5V.

TABLE I

IMPACT OF CONTROL BIT ON OUTPUT FREQUENCY

Control bits				Conventional DCO	Proposed DCO
CB12-15	CB 8-11	CB 4-7	CB 0-3	Frequency (GHz)	Frequency (GHz)
F	F	F	F	1.5672	1.7324
F	F	3	3	1.5692	1.7335
F	0	0	0	1.6073	1.7758
D	0	0	0	1.7012	1.8792
C	0	0	0	1.7516	1.9353
A	8	8	8	1.8386	2.0304
A	8	0	0	1.8397	2.0323
A	4	0	0	1.8552	2.0482
9	0	0	0	1.9350	2.1368
6	6	6	6	2.1468	2.3756
5	5	0	0	2.2589	2.5001
5	1	0	0	2.2836	2.5292
4	8	0	0	2.3516	2.6088
4	5	0	0	2.3829	2.6460
3	8	0	0	2.5312	2.8153
1	5	1	2	3.4821	3.8913
0	0	0	0	4.4916	4.8649

Table I shows the impact of each control bit on the output frequency. The frequency range of [1.7324-4.8649] GHz with a tuning range of 3.1325GHz (≈64%) has been achieved. The output waveform of conventional and proposed 16-bit DCO's are shown in Fig. 6 & 7. Further Fig. 8 shows the relationship between control word and output frequency. It has been observed from the results that with decrease in control bits the output frequency and total harmonic distortion (THD) is increased. Total harmonic distortion is found 75.4865dB at 6666H control word for the DCO output signal. The measured result of the output noise is -161.2dB/Hz at 6666H control word. The phase noise of DCO design in 0.5µm technology is –179.4dB/Hz at the frequency 1.7324GHz is shown in Fig. 9. Simulation results show the speed performance of the proposed DCO is better than conventional DCO. Table II shows comparison of results.

TABLE II

COMPARISON OF PERFORMANCE OF 16-BIT DCO

Results	16-bit conventional DCO	16-bit proposed DCO
Frequency Range	1.5672 - 4.4916 GHz	1.7324 -4.8649 GHz
THD	75 dB	76 dB
Output Noise	-146 dB/Hz	-161.2 dB/Hz
Phase Noise	-178.2 dB/Hz	-179.4 dB/Hz

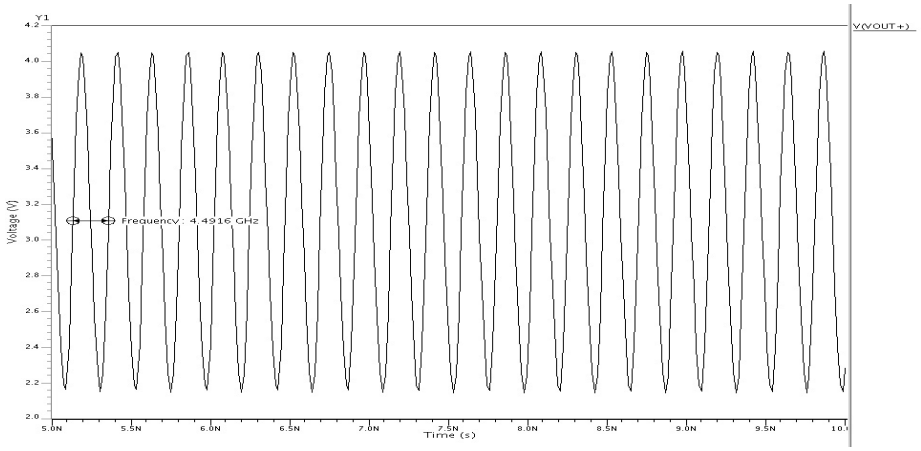

Fig. 6. Output waveform of conventional DCO at 0000H

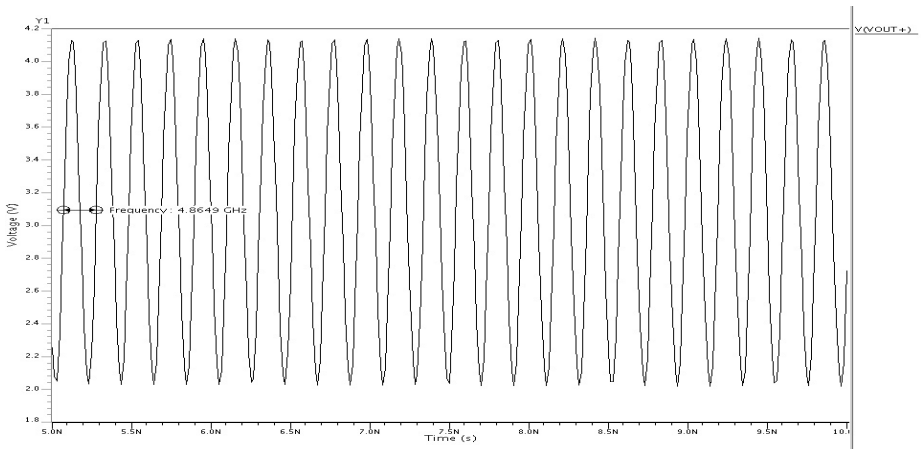

Fig. 7. Output waveform of proposed DCO at 0000H

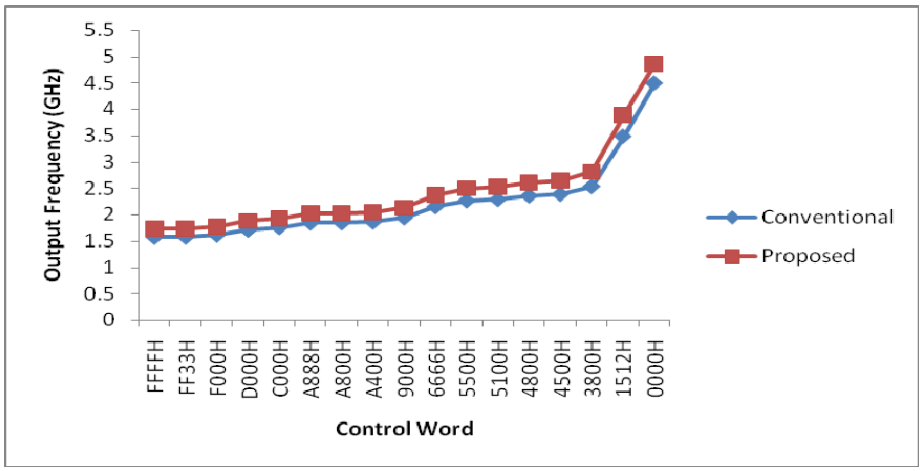

Fig. 8. Relationship between output frequency and control word

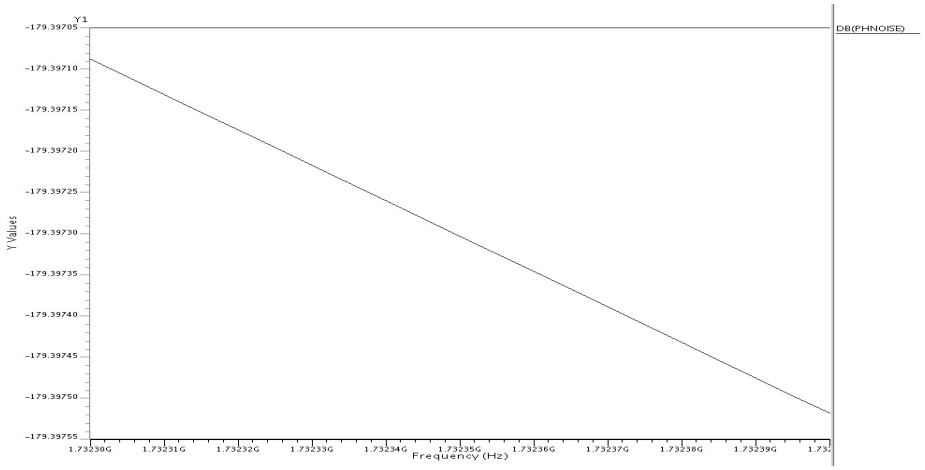

Fig. 9. Phase noise of DCO at FFFFH control word

IV. CONCLUSION

In this paper, a new differential delay cell is proposed and a 16-bit digital controlled oscillator (DCO) is designed with delay cell. In new differential delay cell, pair of NMOS transistors are added to acceleration block which reduce the rise time and fall time of the output signal. This increase the oscillation frequency, total harmonic distortion (THD) and reduce the phase noise of the digital controlled oscillator (DCO). DCO circuits have been designed in 0.5µm technology with supply voltage of 5V. It has been observed from the results that with change in control word from FFFFH to 0000H, a controllable frequency range of [1.7324-4.8649]GHz with a tuning range of 3.1325GHz (≈64%) has been achieved. The phase noise of proposed DCO design in 0.5 µm technology is -179.4dB/Hz at the frequency 1.7324GHz. The proposed DCO shows the features of wider operating frequencies and lower phase noise for high frequency application.

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