Design and Implementation of Seven Level Cascaded H-Bridge Inverter Using Low frequency transformer with Single DC Source

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***Abstract* — A cascaded H-Bridge Seven level inverter using low frequency transformer with single DC source is proposed. The proposed configuration reduces the complexity in design and modularity when compared to conventional method which also provides reduced switching losses and harmonics. A multilevel shifted carrier based sinusoidal PWM switching scheme is utilised to reduce the complexity in control design. Therefore an identical H-bridge module is used to improve manufacturability and modularity. The circuit performance is simulated using PSIM and experimental results are tested using laboratory prototype.**

***Keywords*— Multi-level inverter, cascaded, H-Bridge, transformers, multilevel shifted PWM**

I. INTRODUCTION

Nowadays multilevel inverter (MLI) plays a vital role in the field of power electronics and being widely used in many industrial and commercial applications. Moreover the advantages like high quality power output, low switching losses, low electro-magnetic interference (EMI) and high output voltage made multilevel inverter as a powerful solution in converter topology. Generally multilevel inverter configuration is classified into (1) Diode clamped multilevel converter [17], [21]-[22] (2) Flying capacitor multilevel converter (FCMC) [17]. (3) Cascaded multilevel converter (CMC)[14]-[19],[15].The operation of all these three configurations were compared and analysed in terms of reliability, feasibility and efficiency. The system reliability is not directly relative to the number of components used. Among the above said configuration CMC requires individual voltage source for each H-Bridge module for obtaining synthesised ac output whereas FCMC and DCMC requires more number of capacitors and diodes respectively for their operation[11]-[22],[27] and these multilevel inverter also requires complex PWM control.

A Seven Level Cascaded H-Bridge Inverter Using Low frequency transformer with Single DC Source is presented which overcomes the disadvantage of conventional CMC by employing low frequency transformers with single DC source. Using this proposed model number of DC sources are reduced thus decreasing the complexity and cost of the design. Also a low frequency transformer provides galvanic isolation and is used to obtain the required output voltage level with reduced harmonic components. Relay angles of the converter is obtained based on linearization method and this approach is useful in elimination of lower order harmonics. In this paper a seven level inverter configuration was analysed using PSIM and the same is implemented using hardware prototype.

II. GENERALISED H-BRIDGE CASCADED TOPOLOGY

Fig.1(a) shows the basic H-Bridge cascaded topology and the operational waveforms is shown in fig.1(b). For obtaining a three level output a basic H-Bridge topology requires one DC source along with four MOSFET switches and one balancing capacitors.Inorder to obtain consequent levels we need a same set of topology as shown in fig.1(a) which increases the number of components needed which in turn creates design complexity and increases the cost and number of components used[1],[2],[7]-[9],[13].It is also found that the maximum output voltage cannot exceeds the sum of voltage of individual sources which becomes the major setback of this topology. Therefore in an application which requires high output voltage from low voltage level, it needs H-bridge module in addition or step-up transformers. To overcome this proposed configuration is employed as in fig 2(b).

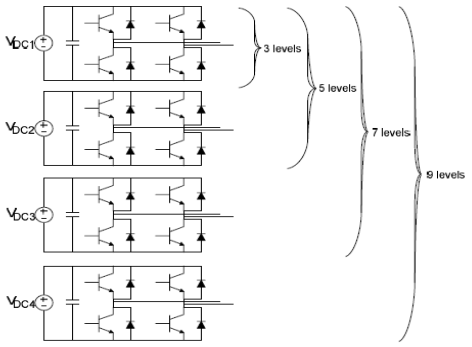


Fig.1(a) Traditional cascaded H-bridge cell multilevel inverter (nine levels)

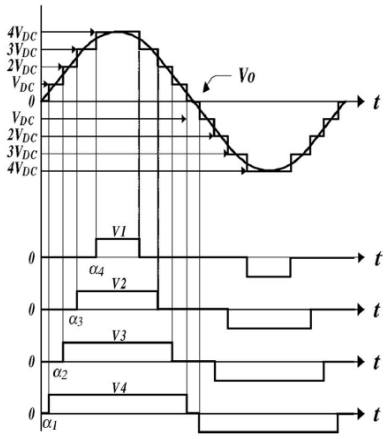


Fig 1(b). Operational waveforms

III. CONFIGURATION OF PROPOSED MULTILEVEL INVERTER

A. *Configuration of proposed circuit*

Proposed configuration block diagram is shown in Fig.2 (a). Circuit configuration of proposed seven level H-Bridge cascaded multilevel inverter (CMLI) as in Fig.2 (b) in which single DC source is linked to the H-bridge modules which are connected in parallel along with series connected cascaded transformer in the secondary side. From the operation point of view each and every H-bridge circuit produces 3-level output (+Vdc , 0 , -Vdc) and every transformer secondary is series connected to obtain the required output voltage. In the proposed configuration output voltage depends on transformer turns ratio and input DC voltage. Harmonic components present in the inverter output voltage is reduced by filtering which is provided by the transformer leakage reactance effect.

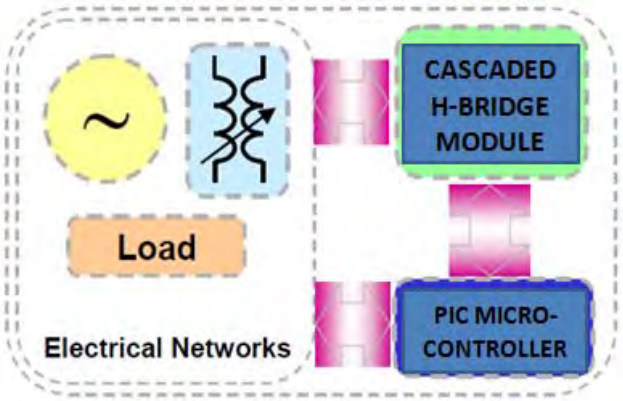


Fig 2(a) proposed configuration block Diagram

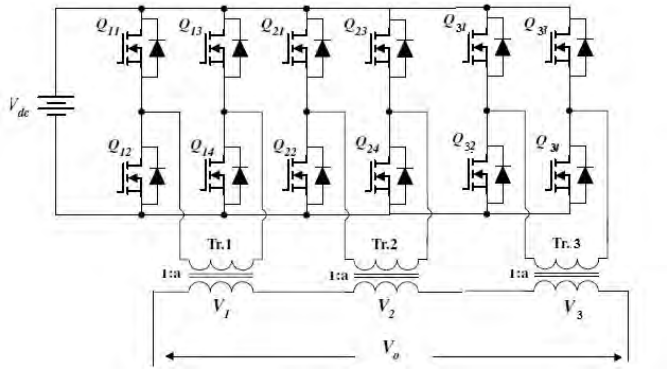


Fig 2(b) Circuit configuration of proposed multilevel inverter

It is also found that variation in turns-ratio of output cascaded transformers results in unbalance power distribution of power in individual transformer, creating power rating divergence in each H-Bridge inverter module and also makes manufacturing of transformer complex.

In order to make the transformer rating same and producing equal power distribution a multilevel-shifted carrier based sinusoidal PWM switching scheme is employed [28]. The validity of a proposed cascaded H-Bridge seven level inverter is verified using PSIM and the same is tested experimentally using laboratory prototype.

TABLE I
Components comparison for 5-level inverter

components	Diode clamped	Flying capacitor	Cascaded H-Bridge	Proposed configuration
Switch	8	8	8	8
Diode	12	0	0	0
Capacitor	4	10	2	0
Input DC source	1	1	2	1
Output transformer	1	1	1	2

B. ***switching pattern***

Fig 3 shows the switching pattern of proposed configuration in which k is the number of transformers used then the respective switching angles are given by α1,α2,α3.....αk and the required output voltage is obtained by varying the switching angles.

The proposed multi-Level Inverter has parallel connected H-Bridge module to synthesise 7-level output. Since each and every H-Bridge module can produce +Vdc, 0, -Vdc then required final voltage (Vo) is obtained by the sum of the output voltage of each cascaded transformers having series connected secondary. In the proposed model employing single DC source the number of output voltage level and number H-Bridge module relation is given by

$$Vo = 2n+1 \qquad (1)$$

Where n- number of individual H-Bridge module

Staircase switching method employing Multilevel carrier shifted PWM (MSPWM) scheme is utilised as shown in fig 5.Output pulses produced by each H-Bridge module during fundamental switching period having unique lower and upper level as shown in fig.7. Similarly other levels also have different solution which meets their corresponding requirements. Conduction angle (α) is the control factor for each H-Bridge module therefore the proposed circuit shown in fig.2 have control factors α1, α2, α3 respectively.

The effective output voltage based on these control factors is given by

$$V_O = V_{dc}\sqrt{\frac{2}{\pi}\left(8\pi - \alpha_1 - 3\alpha_2 - 5\alpha_3\right)} \qquad (2)$$

A suitable solution must be found to diminish the harmonic components present in the output voltage. Harmonic and output voltage fundamental components are analysed by using fourier series expansion as the ultimate output voltage is an odd function and the Fourier series co-efficient is given as

$$b_n = \frac{4}{\pi}\left[\int_{\alpha_1}^{\alpha_2} V_{dc}\sin(n\theta)d\theta + \int_{\alpha_3}^{\alpha_2} 2V_{dc}\sin(n\theta)d\theta + \int_{\alpha_3}^{\frac{\pi}{2}} 3V_{dc}\sin(n\theta)d\theta\right]$$

$$b_n = \frac{4V_{dc}}{n\pi}\left[\cos(n\alpha_1) + \cos(n\alpha_2) + \cos(n\alpha_3)\right] \qquad (3)$$

The value of control factor is determined from above equation from which we can find higher magnitude of a fundamental component with lower harmonics. The effectual value of fundamental and harmonic component is obtained from equation yields

$$V_1 = \frac{4V_{dc}}{\sqrt{2\pi}}\left[\cos(n\alpha_1) + \cos(n\alpha_2) + \cos(n\alpha_3)\right] \qquad (4)$$

$$V_h = \sqrt{\sum_{n=3,5,7...k}^{\infty} b_n^2} \qquad (5)$$

THD is obtained using equation (4) & (5) which is given by

$$THD = \sqrt{\sum_{n=3,5,7...k}^{\infty} V_n^2}$$

$$THD = \sqrt{\left(\frac{\pi(8\pi - \alpha_1 - 3\alpha_2 - 5\alpha_3)}{4(\cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3)}\right) - 1)} \qquad (6)$$

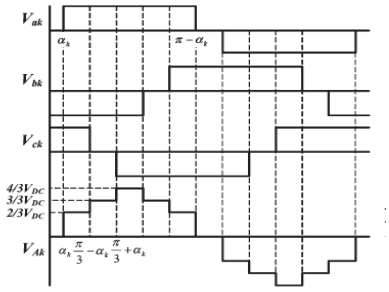


Fig 3 Switching pattern $0 \leq \alpha k \leq \pi/6$

IV. **SIMULATION RESULTS**

Fig.4 shows the simulation of proposed configuration using PSIM in which input dc voltage is 25V and turns ratio of each transformer is maintained as 1:3 in order to produce a output voltage of 225V.Since it is a 7-level inverter, the number of carriers required is six. Each carriers are arranged in a level shifted manner as shown in fig.5 where the positive side carrier and reference is compared to get the gating pulse for the period of 0 to π whereas negative side carrier and reference are compared to get the gating pulse for a period of π to 2π which is then applied to the corresponding switches.

It is also found that switching angle varies simultaneously for different values of modulation index as shown in the fig.6 for modulation index 1 switching angle of first transformer is found to be 11.75 and the extinction angle value is 168.3 producing a output voltage of Vp1 as displayed in fig 7(a).Similarly switching angle of 31.2 and 58.65 is found for the second and third transformer with corresponding extinction angle of 148.8 and 121.4 producing the output voltage of Vp2 and Vp3 respectively as in fig.7(b) and fig.7(c). Seven level output shown in fig.8 is obtained by connecting the cascaded transformer secondary in series.

TABLE II
Simulation Parameters

Input Source voltage(Vin)	25 V
Inverter switching frequency	2 KHZ
Load	R=100 ohm , L=30mH
Output current frequency	50 HZ
Cascaded transformers turns ratio	1:3
Output AC voltage	225 V

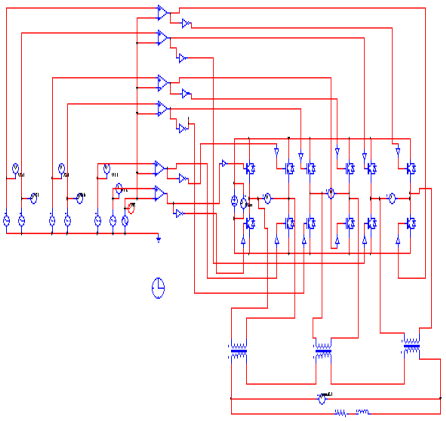


Fig 4. Simulation of Seven level circuit configuration using PSIM

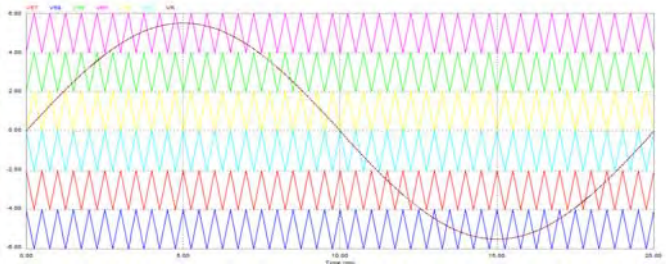


Fig 5.Mutilevel shifted carrier Pulse Width Modulation (MSPWM)

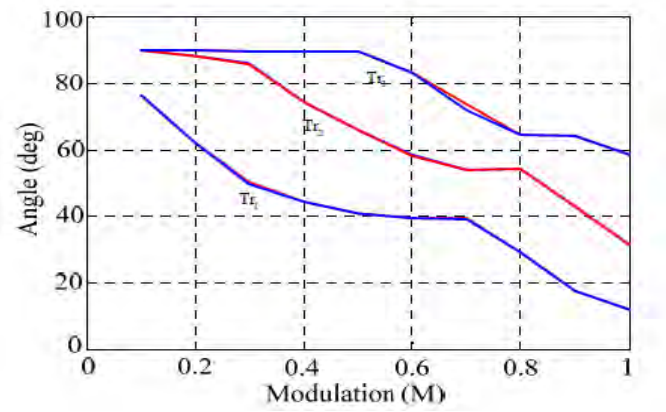


Fig 6. Modulation index variation with respect to switching angle

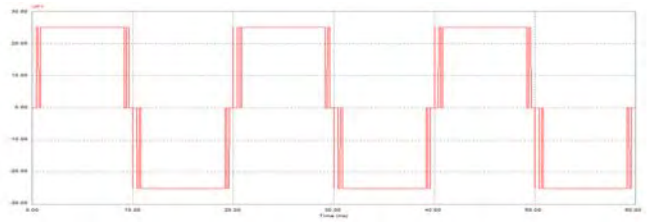


Fig 7(a) Output of first transformer Vp1

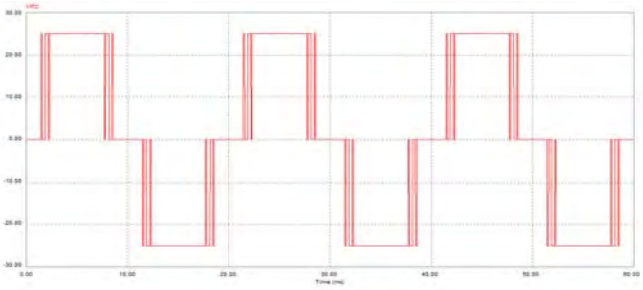


Fig 7(b) Output of second transformer Vp2

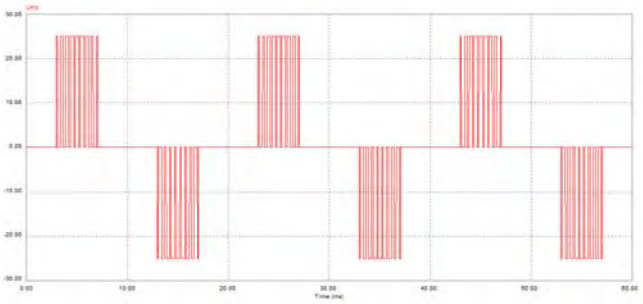


Fig 7(c) Output of third transformer Vp3

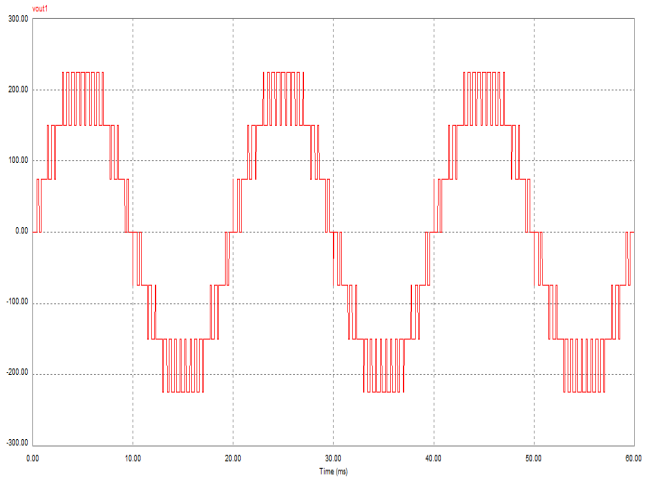


Fig 8. Seven level simulated output using PSIM

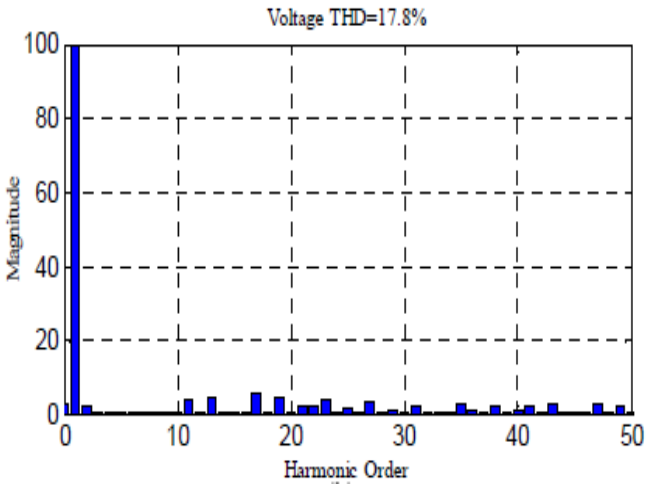


Fig 9. THD analysis

V. EXPERIMENTAL RESULTS

The validity of the proposed seven level inverter circuit configurations in tested with the laboratory prototype as shown in fig.10 which is identical to the simulated circuit. It comprises of three H-bridge module having twelve MOSFET (IRF540) switches along with their driver circuits and PIC 16F877A controller board which is used for generating gate pulses to the corresponding switches and three series connected cascaded transformers in order to obtain the seven level output.

Fig.11 shows the experimental waveforms of the proposed circuit. The transformer turns ratio is maintained at 1:3 to all the three output transformers in order to maintain the equal power distribution among them and to equalize maximum magnetic flux which links between them. The required seven level output voltage is obtained by series connected output transformers in the secondary side which is shown in fig.12

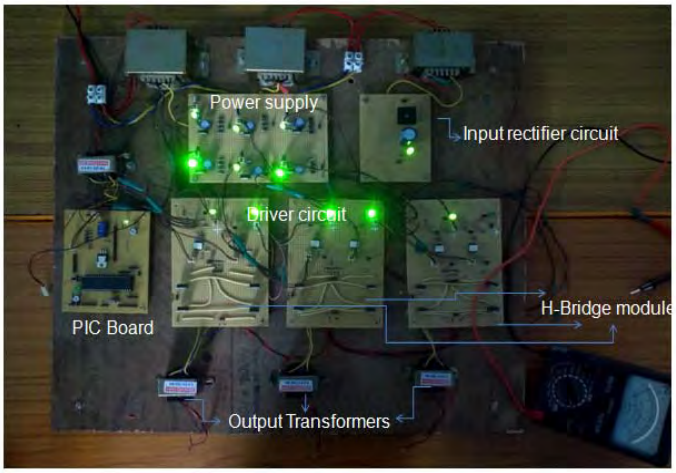
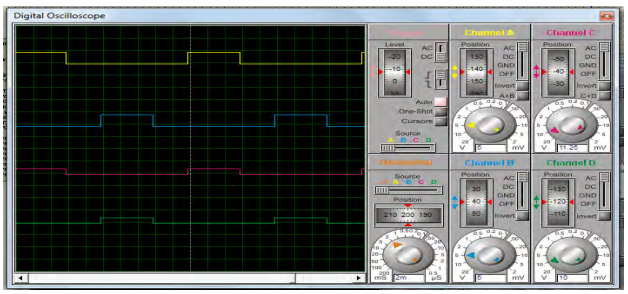
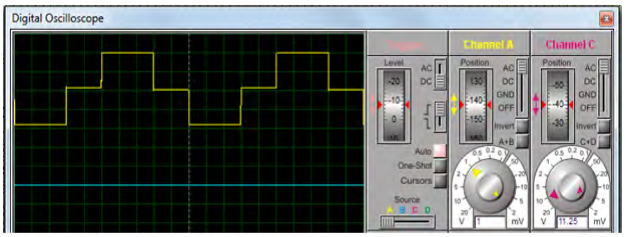


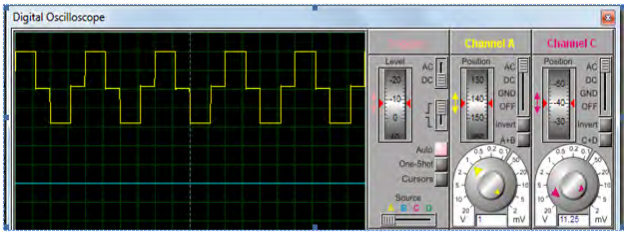
Fig 10. Photograph of Hardware prototype



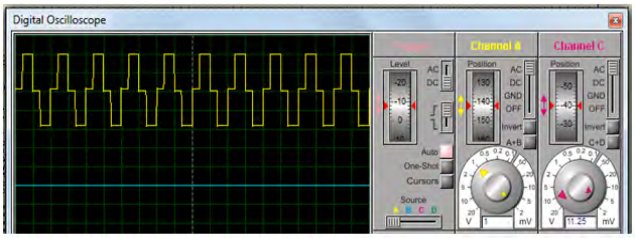
(a)



(b)



(c)



(d)

Fig 11 (a) Gate pulses for first H-Bridge module (b) output of first H-Bridge module (c) output of second H-Bridge module (d) Output of third H-Bridge module

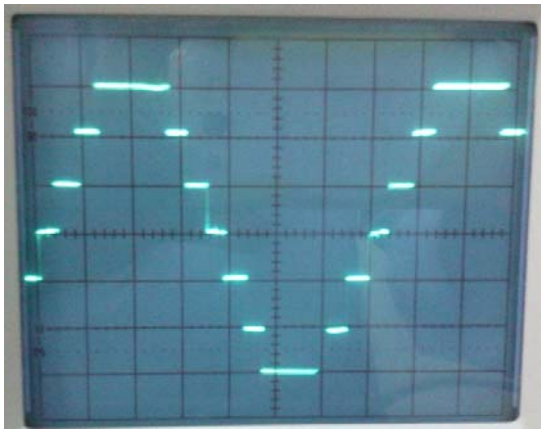


Fig 12 Seven level hardware output

VI CONCLUSION

This paper cascaded H-bridge Seven level inverter using low frequency transformers with single DC source is proposed. The proposed circuit produces required seven level output voltage having low harmonics with reduced number of components when compared to conventional methods. Harmonic spectrum for seven level output voltage is analyzed to prove its efficiency in reducing output harmonic components. Simulated and experimental output waveforms were shown to prove the reliability and feasibility of the circuit.

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