

# Design of a Digital Register (Stand-Alone) through the use of a Mixed Embedded Platform

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**Abstract** - This paper shows the design and implementation of a digital register, only using a microcontroller to acquire and process the information and a very low-cost FPGA to display the information processed on a CRT screen, all without the need of using a personal computer or any external device. In general terms it is proposed the design of a Stand-Alone device that with a keyboard and a screen perform all the functions of a personal computer in the task of registering, processing, storing, visualizing and generating the necessary supports in a basic marketing transaction of products.

**Keyword** - FPGA, Microcontroller, VHDL, Stand-Alone.

## I. INTRODUCTION

The development of low power electronic solutions supported on programmable logic devices grows day by day, this fact is reflected in the large number of specific high-performance solutions and developments based on FPGA architecture (Field Programmable Gated Arrays)[1], [2],[3], generally said solutions are oriented to applications that require a high level of information processing without making use of conventional computing units[4]; in this area of development is where the FPGA intervene as practical and fully functional solutions thanks to properties such as its architecture flexibility and its low cost and in the reduction of execution times [5].

One of the advantages associated with this technological development trend over digital programmable devices, is the possibility of incorporating and integrating different types of architectures (hardware and software) in order to offer a feasible and fully functional solution to a specific problem[6],[7]. Regarding this type of implementations, it is important to highlight the differentiation in terms of the distribution of tasks and activities to be developed for each of its parts, since what is sought is to take full advantage of the capabilities and advantages of the devices to be used (microcontrollers, DSP or FPGAS). Working with mixed platforms allows managing the design in such a way that each operating block is in charge of the best task it can develop thanks to the structural advantages associated with its respective architecture (HW / SW)[8],[9].

This paper establishes a proposal for the design of a digital register for commercial transactions, based on a mixed architecture consisting of two functional blocks associated with a 32-bit microcontroller[10] and an ICE 40 FPGA. In the development of the document it can be seen the diagram of basic blocks by which the prototype is formed, flow diagrams and code structures associated with the proposed design and some metrics of the implementation.

## II. METHODOLOGY

In the development of this work, it is sought to describe a Stand-Alone system that replaces a personal computer or a SOB with a custom designed hardware at a very low cost.

### A. Definition of the system

The block diagram of the system shown in Fig. 1 shows the generalized block diagram, in which it is shown how a microcontroller and the FPGA perform in a coordinated manner the tasks necessary to comply with the requirements of the system.

Being a mixed design must know the advantages of each device, in order to manage the input information in the best way, the FPGA is chosen to perform the tasks of visualization and memory management and the microcontroller takes care of manage the information both input, and the processing required to perform.

The microcontroller is responsible for making the user interface using a USB keyboard and a bar code reading gun which are the data entry of the system, in addition the information will be stored on an SD card as backup of the transactions made.

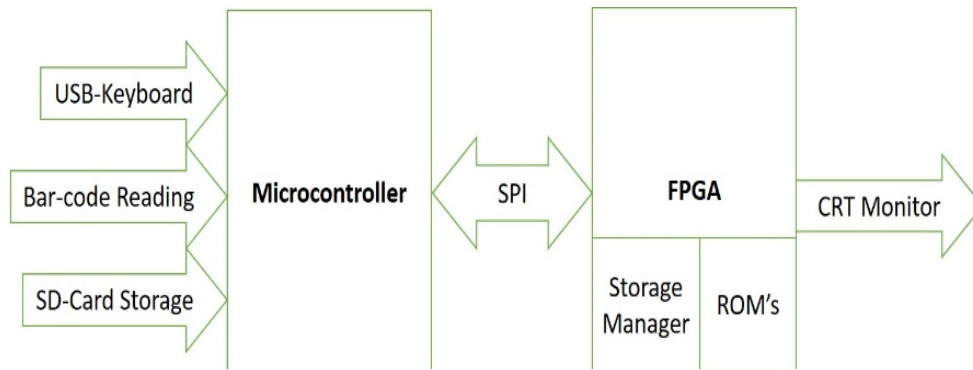


Fig 1. General Block Diagram

On the other hand, the FPGA is in charge of the visualization, communications and to carry out a control of the system by means of a state machine, in such a way that it unloads to the microcontroller of the tasks of high speed and handling of data memory.

*B. Design of electronic control unit in FPGA*

It has a very low-cost FPGA (less than 5 USD), which has just the necessary ports to perform the tasks of visualization on a CRT screen using the VGA protocol, which requires synchronization and control signal management with strict time limitations, in addition to a minimum memory space to store the images and characters to be displayed. On the other hand, it has the logic and speed necessary to perform communication tasks with the microcontroller through a SPI port Fig. 2, the data to be displayed and stored will be exchanged, in this case the microcontroller will process the acquired information and the programmable logic device performs a search in its internal memory to carry out the translation of binary information in Ascii format to its respective ROM memory that will be copied into the memory used to display the data in the VGA; after that the system is responsible for refreshing the information shown in the VGA port Fig 3. (Formatting of the information)

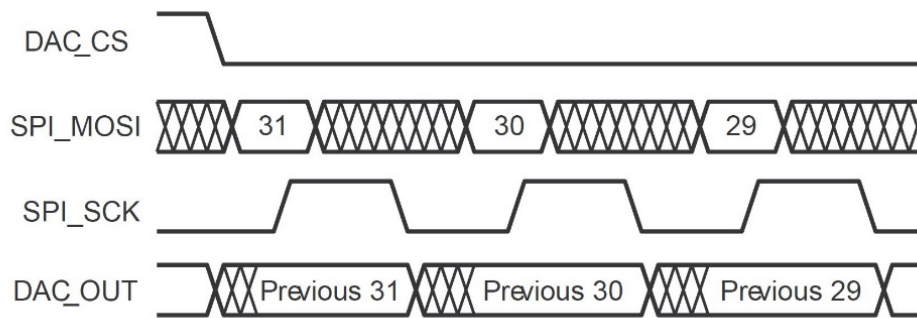


Fig 2. SPI communication waveforms [11]

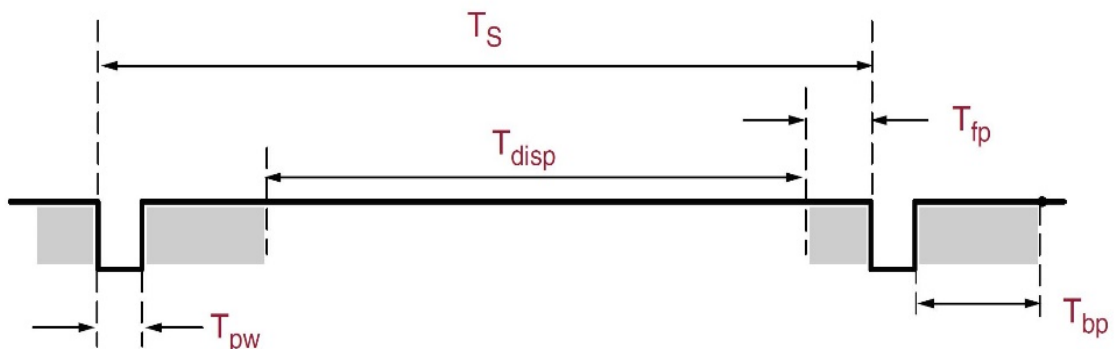


Fig. 3. VGA control timing [11]

*C. Integration of peripherals with microcontroller (Keyboard, SD card, thermal printer)*

The growth in complexity, robustness and quantity of peripherals that currently has a microcontroller, makes it possible to build a complete application with all the necessary resources, in this case a 32-bit microcontroller from the ST company is used, which has a hardware for the handling of a keyboard by USB, along with the memory and handling of the protocol, that makes that with a simple library the data is acquired in ASCII, besides that the Cortex M4 family has a floating point unit which makes that the microcontroller performs complex operations in a few clock cycles. When having the data of the transactions a series of calculations is executed, building a library that looks for the products, its cost and deductions (data stored in the SDcard), this library is written in a C ++ code compatible with any of ARM architecture, with data types, objects and classes easily modifiable to different possible new scenarios, the microcontroller has all the hardware, both the SPI module, the memory and the logical structure to store and read the data. Thanks to the fact that this microcontroller has several communication ports, the storage memory of the data is handled by an SPI, by another different SPI port it exchanges information with the FPGA, and by a serial port type UART it carries out the communication with the thermal printer.

**III. PROPOSED ARCHITECTURE**

Being a mixed solution, the designer must choose which task should be done with hardware and software, in such a way that the advantages of the two devices to be used are exploited, the FPGA is used for high processing and high-speed things but that do not require complex protocols or systems. In this case the FPGA will be responsible for being the auxiliary memory of the microcontroller, storing in RAM memory the operation data, performs tasks of transforming the information to be visualized in the CRT screen by means of the VGA protocol, besides that it is in charge of processing the information sent by the microcontroller through the SPI port; the internal block diagram of the solution that specifies in detail the internal operation by means of a Data-path Fig. 4, has functional blocks commanded by a control unit that is described in using a finite state machine Fig. 5 which acts as the control unit of the embedded hardware solution.

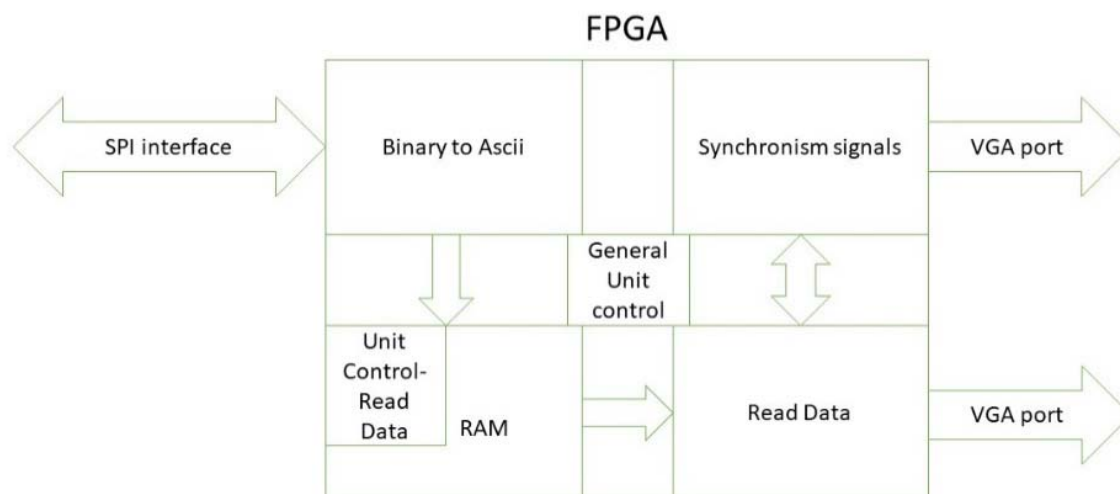


Fig. 4. FPGA Data path

Regarding the source code of the microcontroller, it was sought to carry out a programming that has the philosophy of RTOS, bread making a planning of tasks for each of the parts and modules involved, in general a specific task of data entry was performed by the keyboard, which attends the task when it receives an interruption, this task requires a space in memory that is shared to perform the search in the SD-Card, this task is responsible for performing a search in the external memory and return with the data, In addition to having a task of communications with the FPGA, where the data to be displayed is sent, in addition to the moment of requiring the generation of the invoice, there are some functions that perform the printing in the format pre-established by the business establishment.

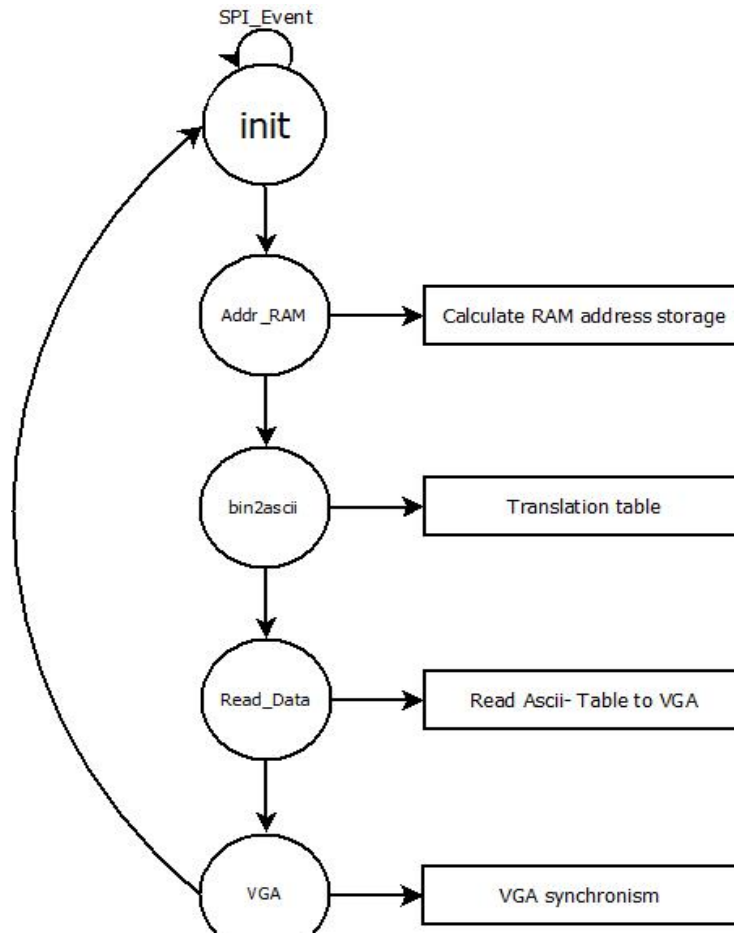


Fig. 5 State machine- FPGA system control unit

In this case, each task is handled with a function in C ++, so a diagram of classes Fig. 6 is shown, which gives a global idea of how the data interacts within the general solution, on the other hand a diagram is also shown of the basic flow of the solution Fig. 7, where the software embedded in the microcontroller is described in a general manner.

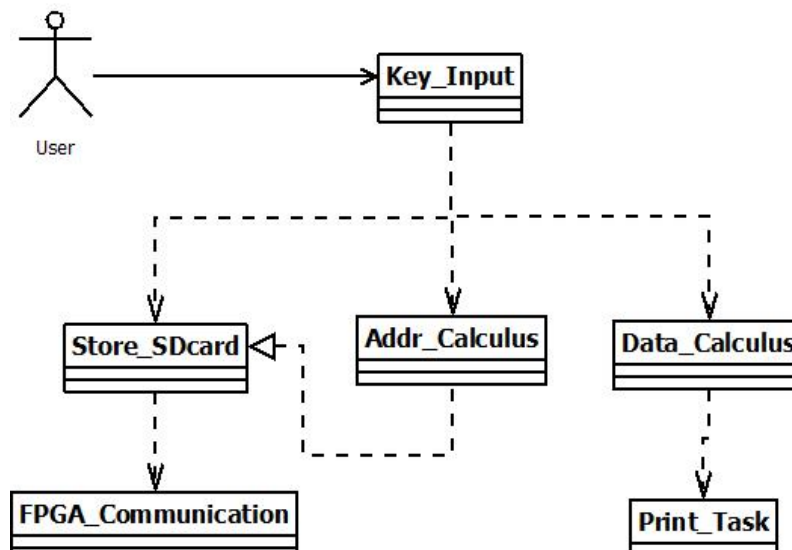


Fig. 6. Class Diagram over the microcontroller

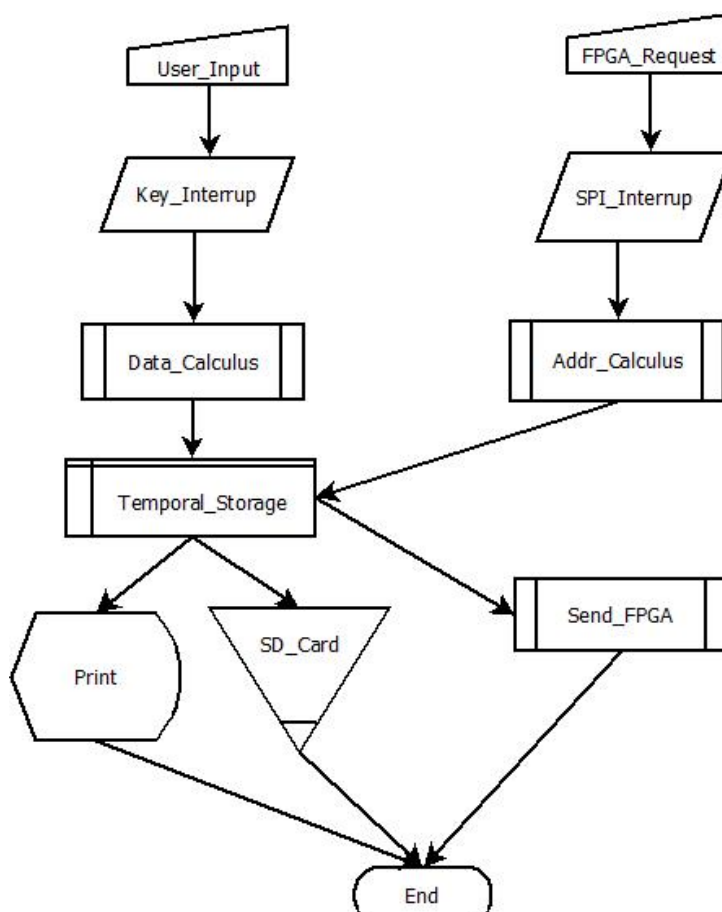


Fig. 7. Flowchart on the microcontroller

#### IV. RESULTS

##### Implementation metrics

The ICE 40 FPGA from Lattice was used, which has been cataloged in the last two years as the cheapest programmable logic device in the market, this device is suitable for portable embedded solutions due to its low power consumption, only about 25 micro watts, the hardware embedded solution was made in VHDL, and for the realization of the tests the Lattice iCEstick Evaluation Board Fig. 8 was used, which has "cores hardware" of SPI both for the configuration of the device and in this case for the communication between the PLD and the microcontroller, it has a dedicated hardware for handling CRT screens through VGA, since it has the RGB interface, 7: 1 LVDS and MIPI DPI / DBI, together with these capacities it has up to 128 K of RAM in functional blocks within of the same device, which perfectly meet the internal storage needs for the work of exchange of information and management of the necessary images to be displayed on the CRT screen.

As for the software embedded solution, it was made using the Core F446RE platform, using a standard C ++ code and the free platform for programming Mbed on-line microcontrollers, which allows the code to be scalable to any other compatible ARM device of any type of manufacturer, this device works at 180Mhz, with one cycle of machine per Hertz, in addition to this has a FPU (Float point Unit) of double precision, a feature that makes it performs any calculation in very few clock cycles, has 512 KB of Flash, and 128 KB of RAM, which is more than enough for the application, has 4 SPI ports with independent hardware that are useful for the interface with the SD-Card and high-speed communication with the FPGA, 4 serial ports RS232 for handling the thermal printer, plus a USB-OTG port that has the memory, speed and external hardware needed to operate a standard computer keyboard, together with embedded RTC hardware to save the record of the exact date and time of any transaction made. In this case, the embedded software does not exceed 30% of the capacity of the microcontroller, written in tasks and standard libraries functions for handling the used peripherals.

## V. CONCLUSIONS

The use of 32-bit microcontrollers accompanied by FPGA in a mixed solution, allows for a completely independent development, without requiring modules, peripherals or any external memory, which, in this case, is applied to a point solution with only two data inputs and simple functions in terms of the complexity of the algorithm, the devices used have the ability to handle the amount of memory needed to perform this application. This solution was made with very low-cost hardware elements, not using the entire hardware resource available in the devices used, in such a way that it supports possible improvements and extensions.

On the other hand, since the system does not run under any operating system and all the hardware is totally free, it does not have additional licensing costs, possible problems with viruses or all the inconveniences that the register systems have using a personal computer, in addition to this the size of the final device is reduced, which makes it versatile in its use, this also reduces the costs of manufacturing, maintenance and possible repairs.

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## REFERENCES

- [1] R. Jeyakumar, M. Prakash, S. Sivanantham, and K. Sivasankaran, "FPGA implementation of edge detection using Canny algorithm," IC-GET 2015 - Proc. 2015 Online Int. Conf. Green Eng. Technol., pp. 1–4, 2016.
- [2] K. Pal, S. Rana, V. Kumar, A. K. Dagar, A. Chandel, and A. Kataria, "FPGA Implementation of Steinhart – Hart Equation for Accurate Thermistor Linearization," vol. 18, no. 6, pp. 2260–2267, 2018.
- [3] T. Hu and T. Ikenaga, "FPGA Implementation of High Frame Rate and Ultra-Low Delay Vision System with Local and Global Parallel based Matching," pp. 286–289, 2017.
- [4] T. N. Son, T. M. Hoang, N. T. Dzung, N. H. Giang, and I. Technology, "Fast FPGA Implementation of YUV-based Fractal Image Compression," pp. 440–445, 2014.
- [5] O. Grairi, "Design and Implementation of a Versatile Display System based on FPGA for Embedded Systems," pp. 2–6, 2015.
- [6] T. Pozna, "Raspberry Pi as a Measurement System Control Unit," pp. 2–5, 2014.
- [7] R. Szabo and A. Gontean, "Mouse and display driver on a single microchip tested on FPGA and built for an ASIC," 2016 IEEE 22nd Int. Symp. Des. Technol. Electron. Packag. SIITME 2016, pp. 118–121, 2016.
- [8] Y. Xu, Q. Zhou, L. Gong, M. Zhu, X. Ding, and R. K. F. Teng, "High-Speed Simultaneous Image Distortion Correction Transformations for a Multicamera Cylindrical Panorama Real-time Video System Using FPGA," vol. 24, no. 6, pp. 1061–1069, 2014.
- [9] E. Zheng, Z. Song, and L. Ma, "Data acquisition and VGA display controller based on NiosII," ICSPPS 2010 - Proc. 2010 2nd Int. Conf. Signal Process. Syst., vol. 3, pp. 417–421, 2010.
- [10] H. K. Singh, A. Chauhan, S. Sreelal, S. Sreeekumar, and A. B. Diagram, "High-capacity Data Acquisition System based on Cortex-M3 for Aerospace Applications," no. 978.
- [11] XILINX, "Spartan-3A/3AN FPGA Starter Kit Board User Guide", 2008.