

# Energy Efficient Design of Logic Circuits Using Adiabatic Process

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**Abstract-** In today's electronic industry the Low power has emerged a principle theme. The most important features of modern electronic equipment is energy efficiency, it is designed using high speed and its portable applications. Power consuming can be reduced by adopting different style which is said to be excellent solution to low power electronic appliances. The adiabatic logic will be used as an efficient energy technique for digital designs in this paper. The proposed system offers low power dissipation when compared to conventional CMOS logic [1-6]. This paper provides full adder in various adiabatic logic styles and its results are compared to conventional CMOS logic. This simulation output specifies that proposed system is beneficial for various low power digital applications.

**Keywords-** Adiabatic logic, Charge improvement, Low power, Energy efficient digital designs, Sinusoidal power clock.

## I. Introduction

Power consumption plays a major role in the today's VLSI technologies. In today's world many of the electronic appliances are portable, they require more battery storage which can be solved only using low power circuits that are internally structured. Thus the efficiency of energy has become an important distress in the portable devices to get good results with less power dissipation. Once the power dissipation in a equipment is increased means additional design is important to cool the equipment and safeguard the equipment from thermal breakdown. This output leads to increase in total area of component. In order to solve these problems the power consumption of the design is to be decreased by including various low power styles. The circuit will be more efficient if the power dissipation is lower. In some of the previous decades CMOS tool plays a vital role in creating less power overwhelming equipments. CMOS plays a superior role while comparing with various logic families and previous low power designs. During to the switching of the devices from one to another state and due to the charging and discharging of load capacitor in the output terminal the power consumption is taking place in conventional CMOS design. By reducing the voltage supply, terminal capacitance value and switching of devices the power dissipation in conventional CMOS technology can be decreased. But by replacing the values of such parameters will corrupt the performance of device. Therefore for an efficient low power consumption compare to CMOS technique adiabatic technique will be provide better results. This proposed model is based on energy recovery principle with energy efficient technique known as adiabatic logic.

In this paper instead of discharging, the regained energy is returned back to power supply that decreases the whole power consumption. Here the results of full adder is calculated using various adiabatic logic and its output is compared with conventional CMOS design. As full adder is one of the basic building block of adder designs, this paper is concerned on its design. The performance was evaluated in various adiabatic styles of ECRL, PFAL, 2-PASCL, and PFAL&2-PASCL. Simulation results shows that the proposed technique is efficient over the conventional CMOS design in terms of power dissipation.

## II. CONVENTIONAL CMOS LOGIC

In conventional CMOS design constant voltage supply VDD is used. Energy is dissipated due to switching action of the transistor. 0-VDD Switching. When low voltage supply is given as input capacitor of then output node charges to VDD energy due to the supply is given by  $E = CL \cdot VDD^2$ .

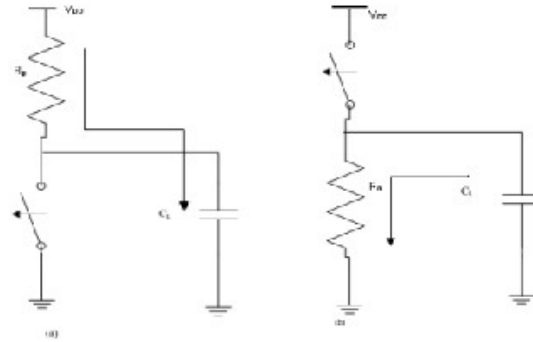


Fig1. Charging and discharging of conventional type –CMOS logic.

Energy collected at the capacitor  $E(CL) = CL \cdot VDD^2 / 2$ . Half of the supply energy will be dissipated in the PMOS[3]. During  $VDD=0$  no energy transfer takes place through PMOS but energy is transferred through NMOS. In conventional design 3 types of power dissipation dynamic switching, short circuit dissipation, leakage dissipation. Dynamic switching[9] is the most dominant type of switching. The switching power depends only on the supply voltage, the shifting frequency, the starting and ending voltages, and the corresponding capacitance of a switching terminal [10]. In order to reduce the power dissipation reduction of VDD supply voltage must be done or node capacitance CL must be reduced. Instead of varying these parameters adiabatic logic design is preferred over conventional CMOS logic design.

#### A. Conventional CMOS Design (Full Adder)

In this design PMOS pull up network as well as NMOS pull down network is used input source is given VDD supply.

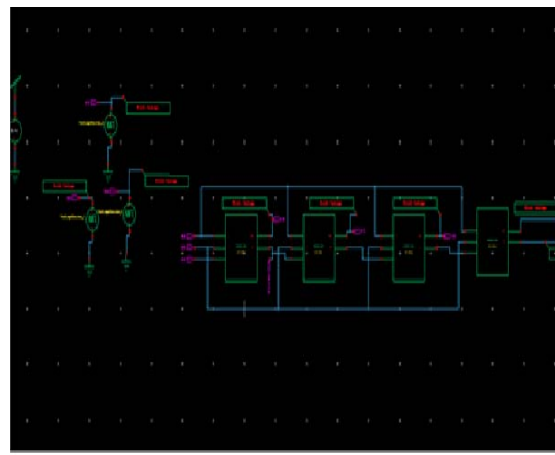


Fig 2. CMOS full adder design using tanner

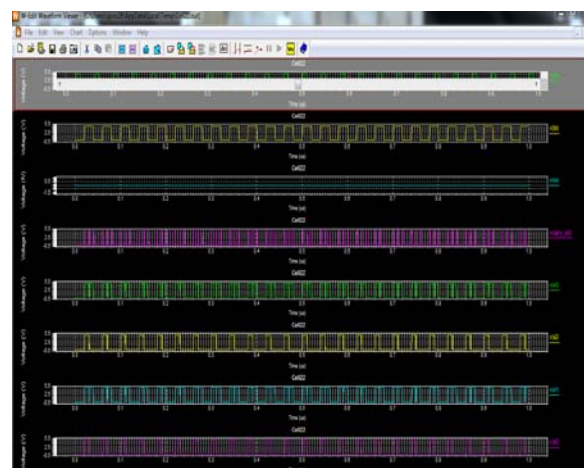


Fig 3. O/P Wave form of conventional CMOS full adder.

Table 1. POWER REPORT (VIA TANNER)

1)	Total Power from time 0 to 1e-007
2)	Average power consumed -> 1.259367e-002 watts
3)	Max power 1.259367e-002 at time 0
4)	Min power 1.259367e-002 at time 1e-007

### III. ADIABATIC CMOS LOGIC DESIGN

Incase of improving the efficiency, operation of Adiabatic logic design is chosen. The amount of energy repeating [1] is achieved by adiabatic technique which is defined using voltage swing and switching speed. Modification of circuit is done to recover power in order to avoid wastage of power into the ground by using ramp powered signal.

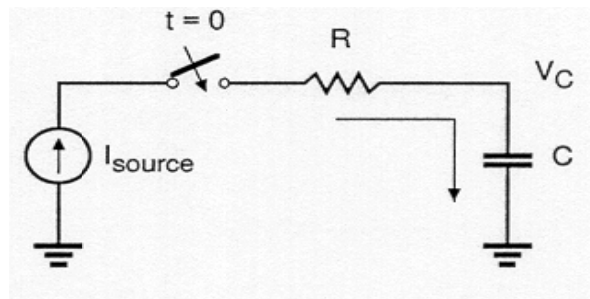


Fig 4. Electric circuit model of adiabatic circuits.

The above figure shows electric circuit model of the circuit which comprises of resistor in series with capacitor. Here the Ramped clocked signal is used as supply to the source rather than dc voltage source it has used in the conventional circuits.

*Important parameters and derivation of energy dissipation:-*

Constant current source is used as

$$\text{Estimated current } i(t) = cdv/dt$$

$$\text{Energy during charging } E = i^2 * R * T_{on}$$

$$\text{Voltage across the switch } V = i * R$$

$$\text{Energy due to adiabatic process } E_{ad} = R * (C * VDD)^2 / T_{on}$$

Where,

R :- Resistance offered by the mosfet

C:- Capacitance of the node

TON:-Charging time of the capacitor

#### A. Phases of Ramped Clock Signal

In adiabatic logic circuits ramped signal used as a supply uses 4 –phases, as has been listed below:-

1. Evaluation phase
2. Hold phase
3. Recover phase
4. Wait phase

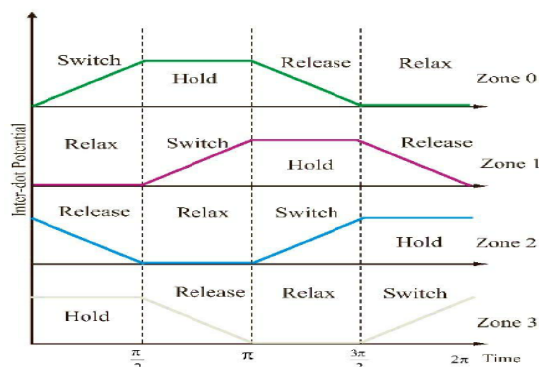


Fig 5. Clock phases of adiabatic logic.

1. *Evaluation phase or Switch phase:* It is the transition phase of the output .It takes place when the capacitor voltage changes from 0 to VDD .Energy is supplied by the source in this phase.
2. *Hold phase:* It is the stable phase of the output or also called as steady output phase. Output is held high at VDD State.
3. *Recovery or Release phase:* In this recovery phase energy given to the capacitor is again taken back by the source hence no energy gets wasted to the ground
4. *Wait phase:*It is similar to hold phase but output is at lowstate.

#### A.Types of adiabatic logic

Various types of adiabatic logic circuits are discussed below . Most of these are associated with the designs of logic circuits.They can be classified into 2 types based on types of energy recovery logic:

1. Partial Adiabatic Logic which includes Efficient Charge Recovery Logic and Positive Feedback Adiabatic Logic.
2. Fully Adiabatic Logic which includes 2-Phase Adiabatic Stratic Clock cmos Logic.

##### 1. Efficient Charge Recovery Logic (ECRL)

In this type of logic it comprises of two blocks of N-MOSFET blocks one with normal input and other with complementary input output obtained are dual in both buffered form as well as complementary form. Also it has two pmosfet circuits,ECRL cannot able to choose the power clock [7]which performs like quasi adiabatic logic technology [2]. ECRL narrates a technique of performing similar pre-charge and evaluation.

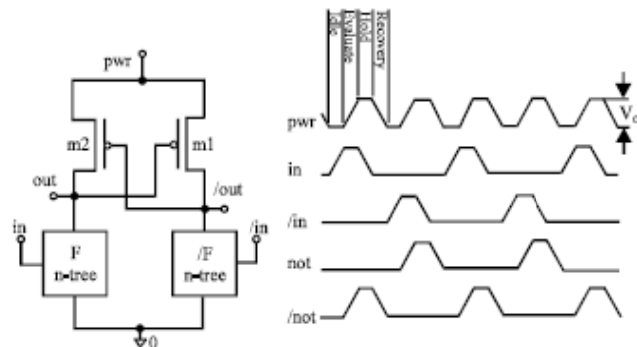


Fig 6. ECRL design

Logic function in ECRL inverter is, when power clock goes up starting from zero to VDD, output stays in ground level and when power clock reaches at VDD, outputs 'out' and '/out' hold logic value zero and VDD respectively. This output values will be used for the next stage x. When power clock falls from VDD to zero, '/out' returns its energy to power clock which recovers the delivered charge.

##### 2.Positive Feedback Adiabatic Logic (PFAL):

In ECRL Logic both buffered as well as complementary outputs may have the same output at one stage this leads to dual race around problems, output degradation takes place. Since the PMOS circuit is parallel connected with the N-input blocks hence the effective resistance reduces as energy dissipation is directly proportional to resistance energy dissipation also reduces. Logic function in PFAL is, when power clock goes up from zero to VDD, output (out) stays at ground level and /out follows power clock. When power clock arrives at VDD, out and /out hold logic value zero and VDD. This output values can be used for the next stage. When power clock falls from VDD to zero, /out returns its energy to power clock which recovers delivered charge.

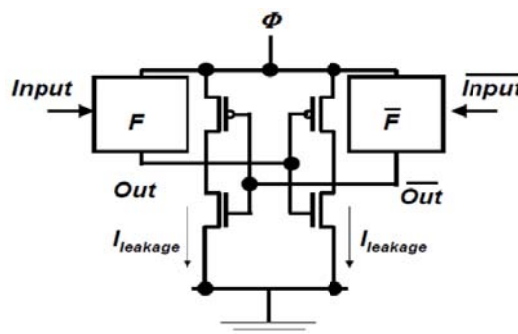


Fig 7. PFAL design

### 3.2-Phase Adiabatic Stratic Clock cmos Logic (2-PASCL) :

The Two Phase Adiabatic Static Clocked Logic (2-PASCL) uses two phase clocking split level sinusoidal power supply's it has both symmetrical and unsymmetrical power clocks where one clock is in phase while the other is out of phase[8]. The circuit has two diodes in its construction where one diode is placed between the output node and power clock, and another diode connected between one of the terminals of NMOS and power source. Both the MOSFET diodes are used to repeat charges from the output terminal and to increasing the discharging speed of input signal nodes.

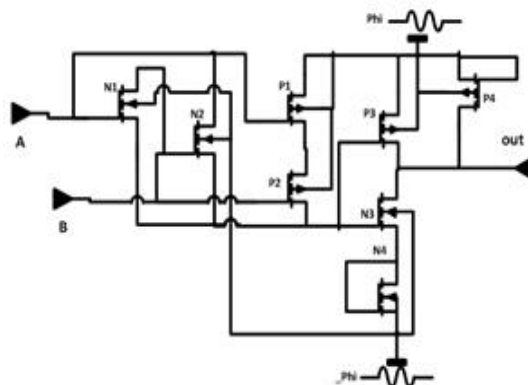


Fig 8. 2-PASCL logic.

The circuit operation is divided into two phases “hold phase” and “evaluation phase”. During the evaluation phase, the power clock swings up and power source swings down. During the hold phase, the power source swings up and power clock swings down.

## IV. PROPOSED DESIGN OF FULL ADDER

### A. ECRL DESIGN (FULL ADDER)

It uses only two PMOS transistors with 2 N-Blocks one with buffered input other with complementary input. Dual outputs are obtained in buffered as well as inverted output. It has 2 separate circuits for sum as well as carry.

Table 2. Power report of Conventional cmos design using tanner

1)	Total Power from time 0 to 1e-006
2)	Average power consumed -> 2.707394e-003 watts
3)	Max power 6.320614e-002 at time 2.0525e-008
4)	Min power 1.699895e-009 at time 0

### Simulation using Tanner (ECRL Sum Design)

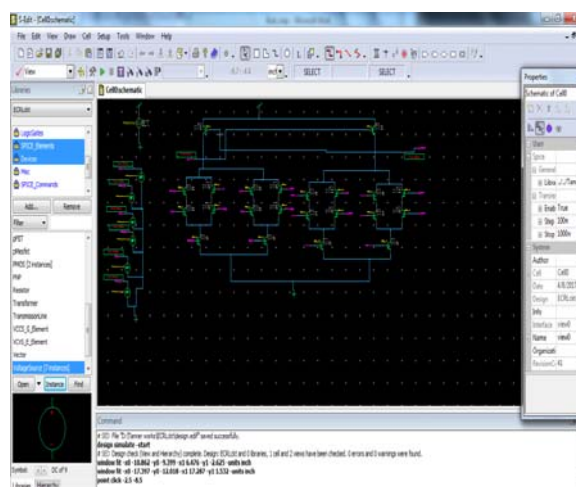


Fig 9. ECRL (sum circuit) design using Tanner.

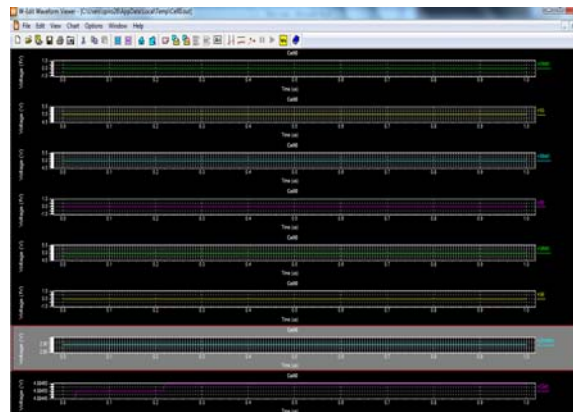


Fig 10. O/P Wave form of( ECRL sum circuit).

Table 3. Power report of (ECRL sum) logic.

1)	Total Power from time 0 to 1e-006
2)	Average power consumed -> 3.031571e-003 watts
3)	Max power 3.031571e-003 at time 0
4)	Min power 3.031571e-003 at time 6.25e-009

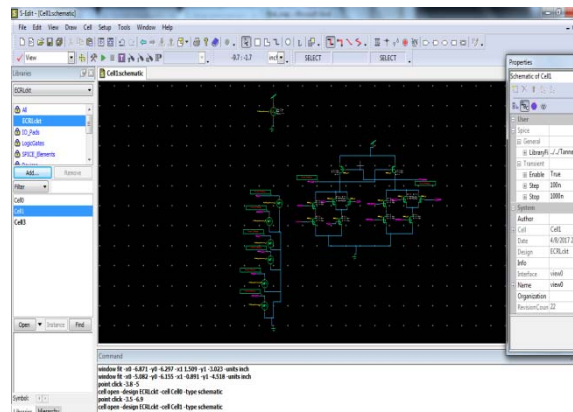


Fig 11. ECRL (carry circuit) design using Tanner.

Table 4. Power report of ECRL carry circuit.

1)	Total Power from time 0 to 1e-006
2)	Average power consumed -> 2.707394e-003 watts
3)	Max power 6.320614e-002 at time 2.0525e-008
4)	Min power 1.699895e-009 at time 0

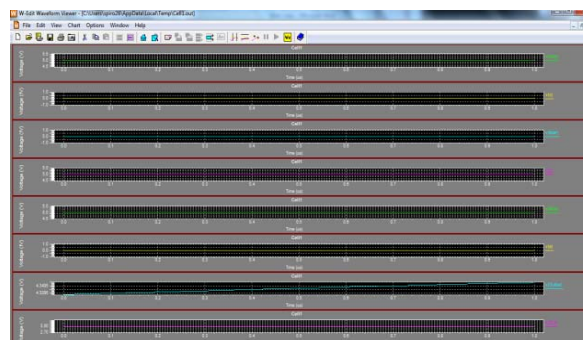


Fig 12. O/P Waveform of (ECRL carry circuit)



### A. PFAL DESIGN (FULL ADDER)

In this circuit PMOS network is connected parallel to the n block inputs. It comprises of n block inputs as well as complementary inputs. Outputs are obtained in both buffered as well as complementary form. It has both sum as well as carry circuit.

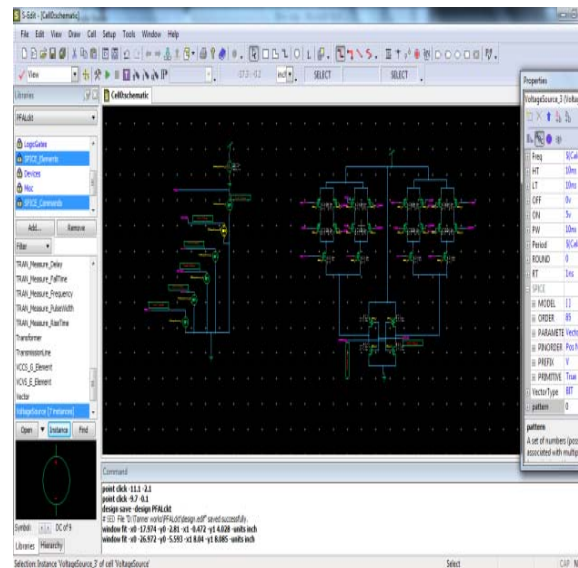


Fig 13. PFAL sum circuit design using tanner

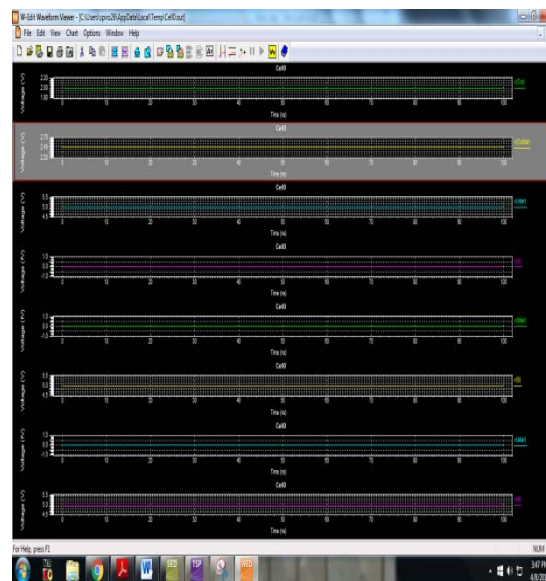


Fig 14. O/p Waveform of (PFAL sum circuit).

Table 5. Power report of PFAL (sum) circuit.

1)	Total Power from time 0 to 1e-006
2)	Average power consumed -> 5.442615e-003 watts
3)	Max power 5.442615e-003 at time 0
4)	Min power 1.168993e-008 at time 1e-009

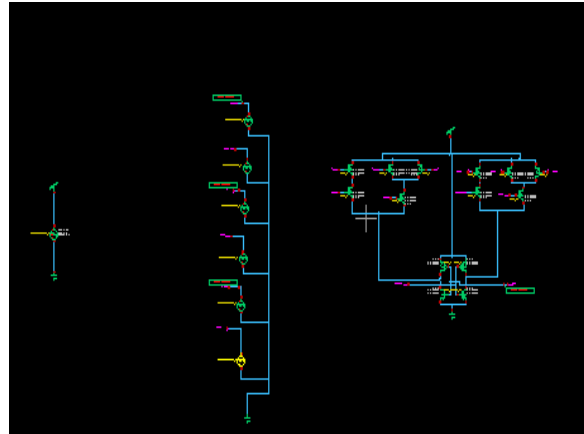


Fig 15. PFAL carry design using tanner.

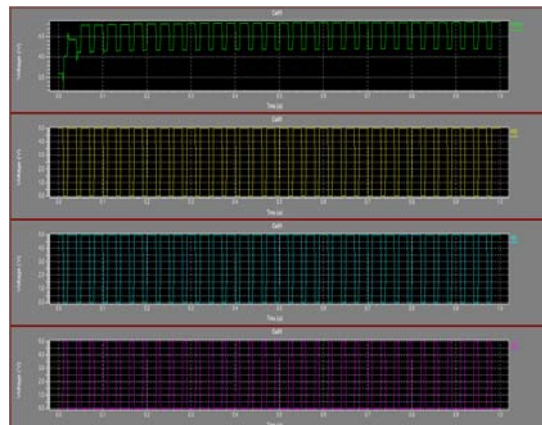


Fig 16. O/P Waveform of PFAL carry.

Table 6. Power report of PFAL carry circuit (VIA TANNER).

1)	Total Power from time 0 to 1e-006
2)	Average power consumed -> 5.385758e-004 watts
3)	Max power 1.750994e-002 at time 2.09714e-008
4)	Min power 1.699895e-009 at time 0

### B.2-PASCL DESIGN (FULL ADDER)

This design consist of two diodes in itsconstruction.One diode is placed between the output node and power clock. Another diode is connected between one terminals of NMOS and power source. This has a separate sum as well as carry.

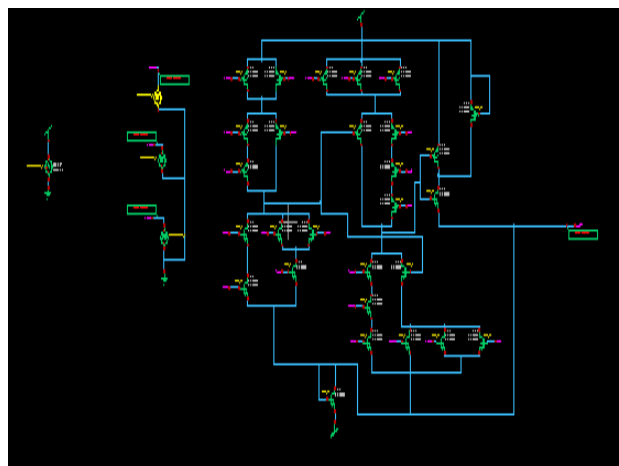


Fig 17. 2-PASCL sum design using tanner



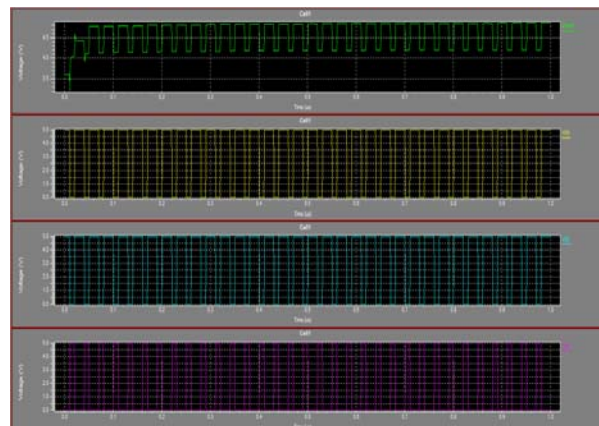


Fig 18. O/P Wave form of 2-PASCL sum.

Table 7. Power report of 2-PASCL sum.

1)	Total Power from time 0 to 1e-006.
2)	Average power consumed -> 4.500492e-005 watts.
3)	Max power 2.049301e-003 at time 1.1e-008.
4)	Min power 5.240466e-010 at time 1e-008.

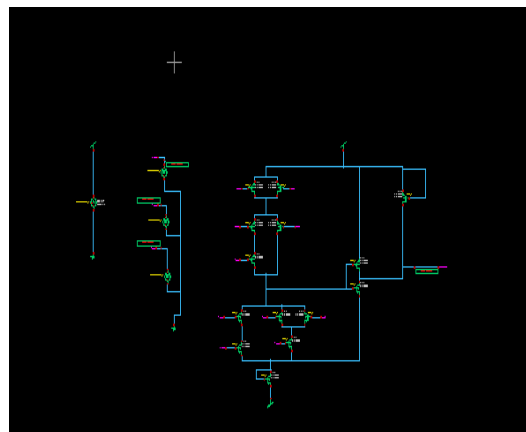


Fig 19. 2-PASCL design of carry circuit.

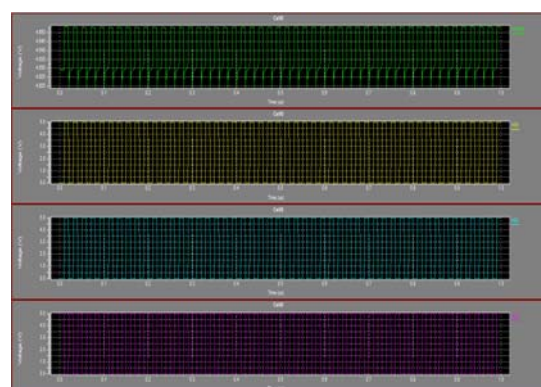


Fig 20. O/P Waveform of 2-PASCL carry

Table 8. Power report of 2-PASCL carry.

1)	Total Power from time 0 to 1e-006
2)	Average power consumed -> 2.440594e-004 watts
3)	Max power 1.001503e-003 at time 1.1e-008
4)	Min power 2.694776e-010 at time 0

Table 9. Types of logic vs power dissipation.

Types of logic	Power Dissipation
Conventional CMOS design	12.59 milliwatts
ECRL (sum + carry)	8.47 milliwatts
PFAL (sum + carry)	3.23 milliwatts
2-PASCL (sum + carry)	4.44 milliwatts

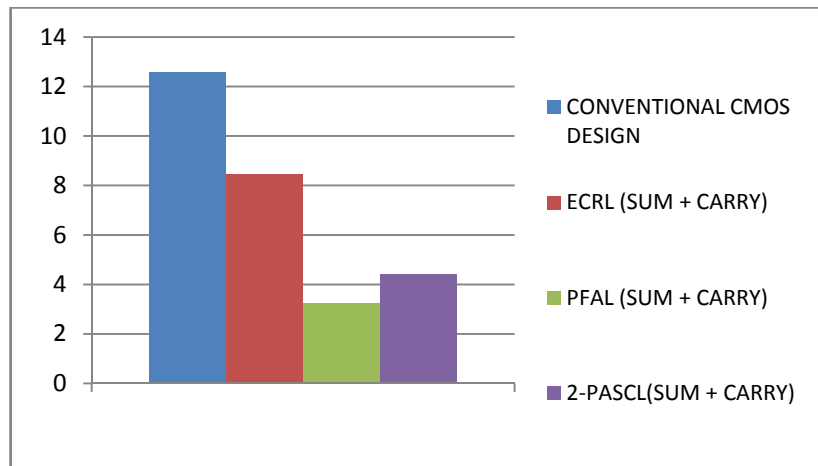


Fig 21. Bar graph representing power dissipation in various adiabatic logic in milliwatts.

Table 10. Efficiency of various adiabatic logics in Percentage.

TYPES OF LOGIC	EFFICIENCY
ECRL	32.72%
PFAL	74.34%
2-PASCL	64.73%

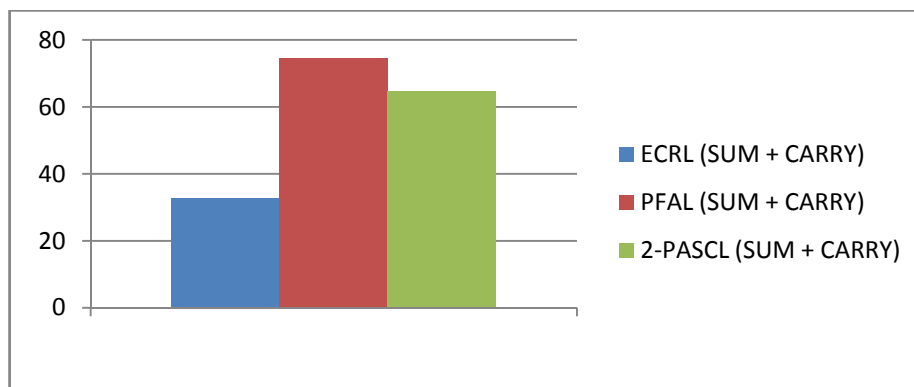


Fig 22. Bar graph representing efficiency in various adiabatic logic.

From this logic it is inferred that PFAL logic dissipates less power as compared to other types of logic.

## V. CONCLUSION

Hence it is observed that, Adiabatic CMOS circuits can be efficiently used to implement a digital circuit design using gradually rising and falling power-clock. Retractable cascade power clocks or multiple phase power clocks with memory schemes can be used in large circuit design with low power consumption. The adiabatic circuit design can be further improved by introducing conventional power supply. Further to improve switching speed of adiabatic circuit as compared to CMOS logic we can design new adiabatic circuits with much better switching speed.

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