

OBIST Method for Fault Detection in CMOS Complex Digital Circuits

R. H. Khade^{#1}, D.S. Chaudhari^{*2}

[#]Research Scholar, Department of Electronics and Telecommunication Engineering
Government College of Engineering, Jalgaon, India
¹rhhkade@mes.ac.in

^{*}Department of Electronics and Telecommunication Engineering
Government College of Engineering, Jalgaon, India
²ddsscc@yahoo.com

Abstract – The paper deals with an oscillation based built-in self-test (OBIST) technique to test faults in complex CMOS digital circuits (CCDCs). It focuses on stuck-at-faults, open or short faults, parametric gate delay faults. The method converts complex CMOS digital circuit under test (CCDCUT) to an oscillator and the output pulses are measured for fix time duration. Discrepancy in the number of pulses is used to judge circuits with catastrophic faults as well as parametric gate delays beyond the threshold limit which is set by designer. The advantage of this method is it does not need external test vector input or complex response analyzer. Universal gates and CCDCs are used to assess and substantiate the usefulness of proposed method. The simulation results show that the proposed method is quite proficient to improve diagnostic accuracy. Fault coverage for catastrophic faults is almost 100%. For $\pm 10\%$ deviation in parameters outside tolerance range limit 100% fault coverage is obtained. The yield loss is around 5% in the tolerance range limit.

Keywords - Built-in self-test, catastrophic faults, complex CMOS digital circuit, complex CMOS digital circuit under test, fault-free complex CMOS digital circuit, oscillation based built-in self-test.

I. INTRODUCTION

Manufacturing very high speed CCDCs is the aftereffect of incessant advancement in semiconductor technology. The advantages of CCDCs are they need fewer MOSFETs and are fast due to single level circuits. The main desideratum of the manufacturer is to provide fault-free high performance circuits at low price. Fault-free chips are needed to reduce the IC cost which is essential to increase the product yield. In mixed signal ICs majority of circuits are digital and testing them is vital to improve yield. To ensure fault-free integrated circuits, a prototype is developed and tested vigorously before high-volume production [1]. In chips with high density of complex circuits, many internal sub-circuits are not accessible through the external input-output pins of IC. Such circuits can be tested by built-in self-test (BIST) which is fast and does not need advanced expensive automatic test equipments.

OBIST method for analog circuits is discussed in [1]-[13]. Conversion of CMOS inverter into oscillator is discussed in [1]. In this paper it is used for testing CMOS complex digital VLSI circuits. The method proposes change in oscillation frequency to detect catastrophic as well as parametric faults present in the circuit. Analog as well as digital circuits are manufactured on the same wafer in case of mixed signal IC. To test mixed signal circuits is a costly and challenging process [1]. The method reduces area overhead and cost if it is used to test both analog as well as digital parts in a mixed signal chip.

Quiescent current (I_{DDQ}) testing approach and traditional approach of applying different input test vectors are used for testing digital circuits. These methods are used for easily detecting faults in simple digital circuits. These faults include, the catastrophic faults like stuck-at-faults due to short circuit of input or output pin to V_{DD} or ground and open or short faults. However, for complex circuits containing more number of MOSFETs the I_{DDQ} method cannot give satisfactory results and the traditional approach is a tedious and delayed process due to increased test vector length.

In some cases, integral current sensor for ΔI_{DDQ} testing was used. The quiescent current was figured out by measuring number of clock pulses till the voltage at the disconnected node drops below reference value. Hence, the accuracy is enhanced by adjusting reference number and clock signal frequency [12]. In some instances, per chip current-threshold have been adaptively determined for I_{DDQ} testing to enhance test accuracy. Primarily the process condition of chip and sensitization vectors have been estimated based on Bayesian inference which successfully detected a very small leakage fault down to 16% of nominal I_{DDQ} current with the test escape ratio of 3.1% [13] [14]. In [15] OBIST method was used to detect faults in operational amplifier of R-2R ladder D/A converter and I_{DDQ} method for testing of R-2R resistor network. A fault coverage of 100% and 96% respectively for 10% and 5% deviation in resistors value from its $\pm 20\%$ tolerance range was obtained. The I_{DDQ} testing method used required 8 test vectors for R-2R resistor network.

OBIST technique to test faults in CCDCs is presented in this paper. Discrepancy in the number of pulses is used to find circuits with catastrophic faults as well as parametric gate delays beyond the threshold limit set by designer. Imperfection in length of channel (L), width (W), threshold voltage (V_T) and transconductance (μ) of MOSFETs are responsible for gate delays. The advantage of this method is it does not need external test vector input or complex response analyzer. Universal gates and CCDCs simulated using 50nm technology are used to assess and substantiate the usefulness of proposed method

The layout of the paper can be given as: The conversion of digital circuit to an oscillator is described in section 2. Section 3 explains the procedure for testing. Simulation results are discussed in section 4. Section 5 contains comments on the results obtained. Section 6 concludes the paper.

II. BASIC PRINCIPLE OF OBIST FOR CCDC

The OBIST methodology for CMOS circuits is illustrated by considering an example of basic gate inverter. The channel mobility of electrons is approximately twice that of the holes. Due to this, the conductivity of NMOS devices is doubled and it is twofold faster than that of identical PMOS device. To compensate for the lower mobility of holes and balance the switching speed, the width of PMOS device is doubled. This gives both propagation delay times identical. The oscillator action is obtained by connecting resistor R, capacitor C and inverter INV_2 as shown in Fig. 1. The channel width of INV_2 MOSFETs is taken large to make its propagation delay negligible as compared to that of inverter INV_1 under test. Due to this the number of pulses provided by oscillator circuit will not get affected by minor parasitic variations in INV_2 . The INV_1 input signal, its output signal and INV_2 output signals are shown in Fig. 2.

When input of INV_1 is low, its output is high and final output of INV_2 is low. The voltage across capacitor C is zero and it charges towards V_{DD} by the current flowing through the ON P channel MOSFET. As soon as input voltage becomes half of V_{DD} the inverter INV_1 output changes to low level, the output of INV_2 becomes high and the capacitor voltage jumps to $[(V_{DD}/2) + V_{DD}]$. As output of INV_1 is low the capacitor discharges to ground level voltage through resistor R and N channel MOSFET. When input voltage drops below $V_{DD}/2$, the INV_1 changes state from ON to OFF. The output of INV_2 changes state to low level, the capacitor voltage becomes $-(V_{DD}/2)$ and it charges through R and pull up device to $V_{DD}/2$, the INV_1 turns ON. If channel ON resistance of pull up and pull down devices is same then $T_1 = T_2$ and period T is (T_1+T_2) .

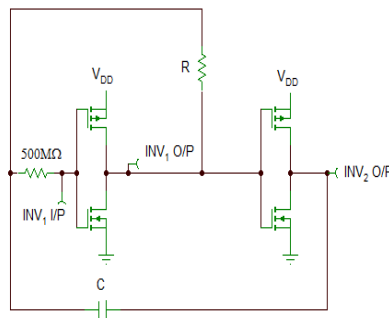


Fig. 1. CMOS inverter converted to an oscillator.

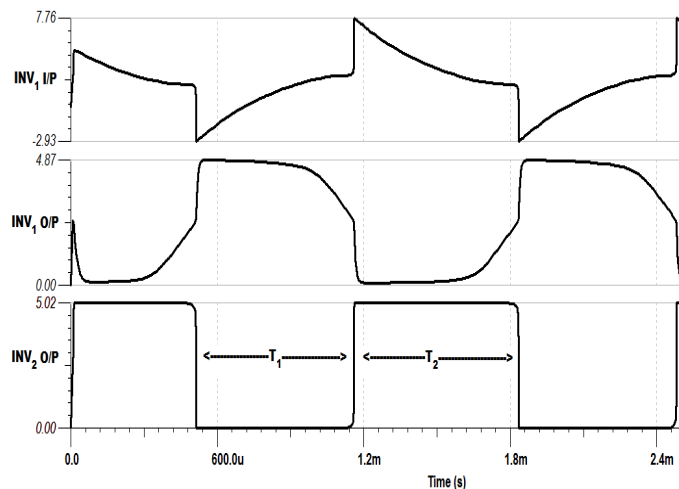


Fig. 2. Waveforms showing inverter 1 input, output signals and inverter 2 output pulses

$$T_1 = R_T C_T I_n \left[\frac{V_{DD} - \left(-\frac{V_{DD}}{2}\right)}{V_{DD} - \left(\frac{V_{DD}}{2}\right)} \right] \quad \text{---Where } V_{DD} : \text{Aim Voltage, } -V_{DD}/2 : \text{Starting Voltage}$$

and $V_{DD}/2$: Stop Voltage

$$= R_T C_T I_n (3)$$

$$= 1.1 R_T C_T$$

$$T_2 = R_T C_T I_n \left[\frac{0 - \left(\frac{3V_{DD}}{2}\right)}{0 - \left(\frac{V_{DD}}{2}\right)} \right] \quad \text{---Where } 0 : \text{Aim Voltage, } 3V_{DD}/2 : \text{Starting Voltage}$$

and $V_{DD}/2$: Stop Voltage

$$= R_T C_T I_n (3)$$

$$= 1.1 R_T C_T$$

$$T = T_1 + T_2 = 2.2 R_T C_T$$

The frequency of oscillator f_{OSC} is given by following equation;

$$f_{OSC} = [1 / (2.2 R_T C_T)] \quad (1)$$

Minimum geometry MOSFETs are used for experimental work. Aspect ratio W/L of N channel MOSFET is adjusted to 1 and as mobility of holes is half as that of electrons, the P channel device with aspect ratio 2 is considered to have identical rise and fall times. Hence, the inverter 1 has an aspect ratio of 2. When output of INV_1 is low, the N channel MOSFET operates in linear region. The selection of proper value of resistor R is important to have oscillatory output. The value of R is taken as 50 times of the ON resistance of N MOSFET to have strong low level output of INV_1 . Table I shows dependence of low level output and f_{OSC} on R and for aspect ratio of N channel MOSFETs 1 and 10. It observed that when R value is equal to channel resistance of N type MOSFET when it just enters into saturation mode, the INV_1 goes to metastable state and circuit ceases to oscillate.

The oscillation frequency of simulated circuit when $R = 400 \text{ k}\Omega$ is 750 Hz which matches with theoretical value of 757 Hz when channel resistance and parasitic capacitance are also taken into consideration. In equation 1, R_T is R plus equivalent ON resistance of selected MOSFET and C_T is C plus parasitic capacitance of devices in the circuit. The small variation in theoretical and practical frequency is result of added negligible propagation delay of INV_2 . The results are verified for circuits having different aspect ratios of MOSFETs, and it is observed that the f_{OSC} is directly proportional to aspect ratio. For increase in aspect ratio by 10 times, required R is $40 \text{ k}\Omega$ and the f_{OSC} becomes 7423 Hz. When this circuit is simulated for 10 ms, 74 pulses are produced.

TABLE I. Effect of R on low level output and number of pulses of inverter 1

Sr. No.	Inverter 1 with aspect ratio of N channel MOSFET 1			Inverter 1 with aspect ratio of N channel MOSFET 10		
	R in $\text{k}\Omega$	Frequency in Hz	O/P low level of INV_1 in mV	R in $\text{k}\Omega$	Frequency in Hz	O/P low level of INV_1 in mV
1	100	2115	375	10	20882	382
2	200	1290	180	20	12774	184
3	300	946	117	30	9324	120
4	400	750	87	40	7423	87
5	500	634	71	50	6265	71

III. STRATEGY FOR CHECKING CMOS CIRCUITS

A. Testing Procedure

The block diagram of testing procedure using OBIST is shown in Fig. 3. The CCDCUT and FCCDC are converted to oscillators and the output pulses of both are measured using digital counters. The counter outputs are compared by comparator circuit. Identical circuits have equal number of pulses and test outcome is **Pass**. In case of any fault in the CCDCUT, the number of pulses differs and test outcome is **Fail** which rejects the chip. Fig. 4 shows the schematic diagrams for two CCDCs. Usefulness of proposed method is studied for these circuits.

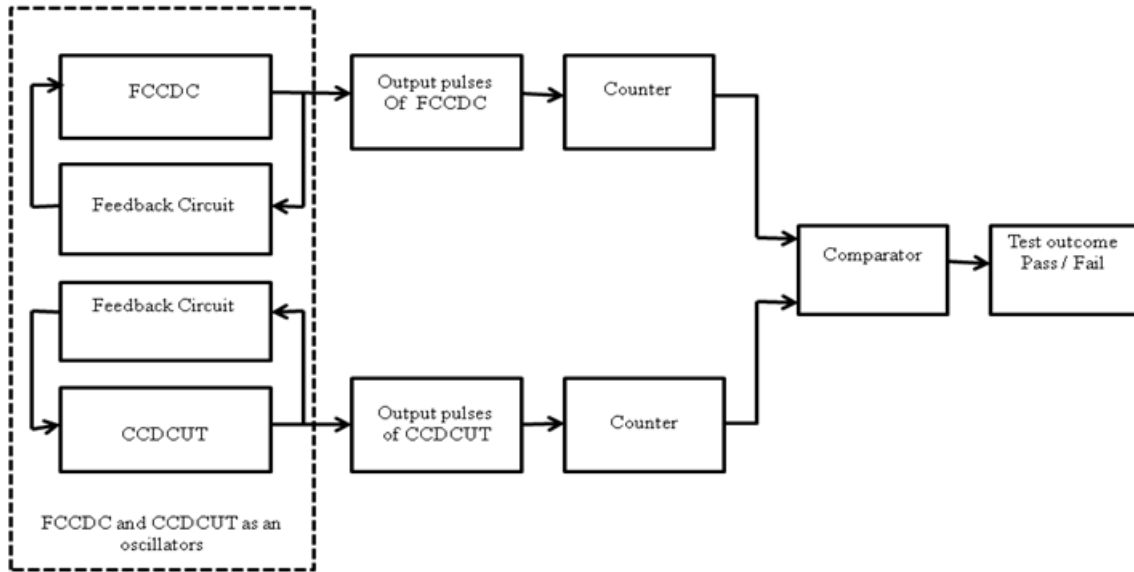


Fig. 3. Strategy for comparing number of pulses provided by complex CMOS digital circuit under test (CCDCUT) and Fault-free complex CMOS digital circuit (FCCDC) using OBIST method

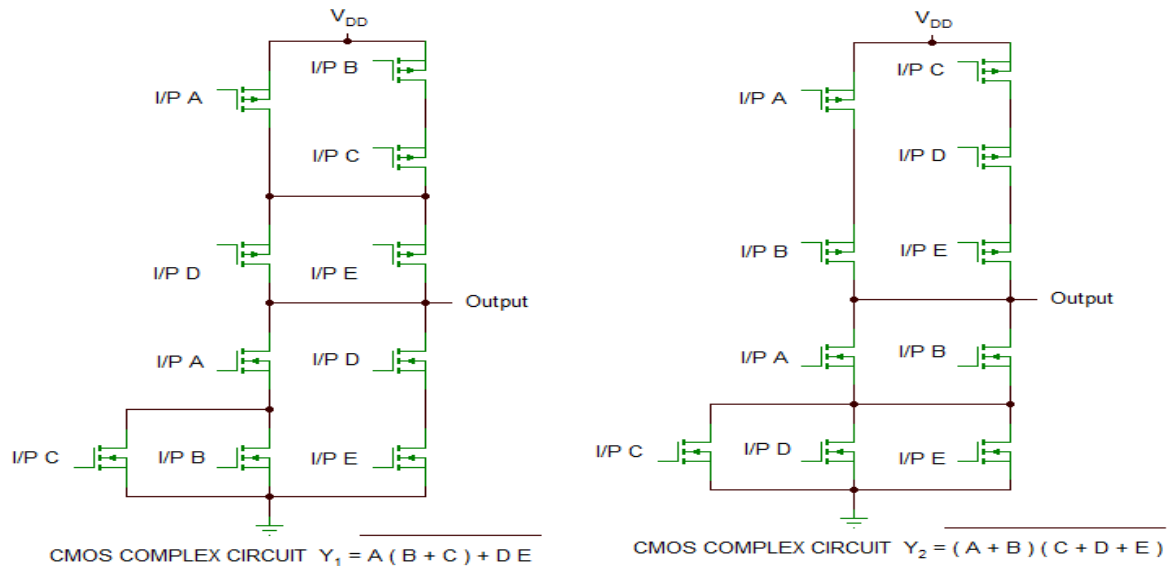


Fig. 4. Two CMOS complex digital circuits

B. Fault Models of MOSFETs

The fault models of N, P channel MOSFETs are shown in Fig. 5. Stuck-open fault for open Source or drain terminal of MOSFET is emulated by connecting high value resistor of 10 to 100MΩ in series with it. The short circuit between source, drain is emulated by small value resistor of 5 to 10Ω parallel to it.

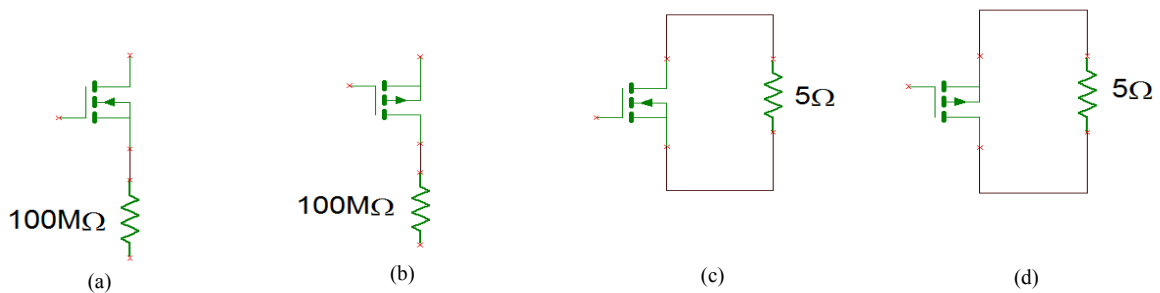


Fig. 5. Fault models for MOSFETs (a) N Channel source or drain open (b) P Channel source or drain open (c) N Channel source, drain short (d) P Channel source, drain short

C. Flow chart representation to detect faults in CCDC using OBIST method

The testing procedure mainly consists of converting CCDCUT and FCCDC into an oscillator. Range of faults are injected in the CCDCUT which is followed by verification of faults in it by comparing pulses generated by both circuits in a fix time slot. Fig. 6 shows a flow chart representation to detect faults in CCDC using OBIST method. Following list gives different steps for checking CCDC:

- (i) The FCCDC is transformed to an oscillator and the number of pulses provided in fix time interval are counted.
- (ii) Fault is introduced in the CCDCUT and simulation is done.
- (iii) Count number of pulses provided by CCDCUT in the fix time.
- (iv) Compare number of pulses provided by CCDCUT and FCCDC in the fix time interval.
- (v) The procedure is repeated until all faults are injected in CCDCUT.
- (vi) Nonappearance of fault in the chip will send it for further processing. For presence of fault it is rejected.

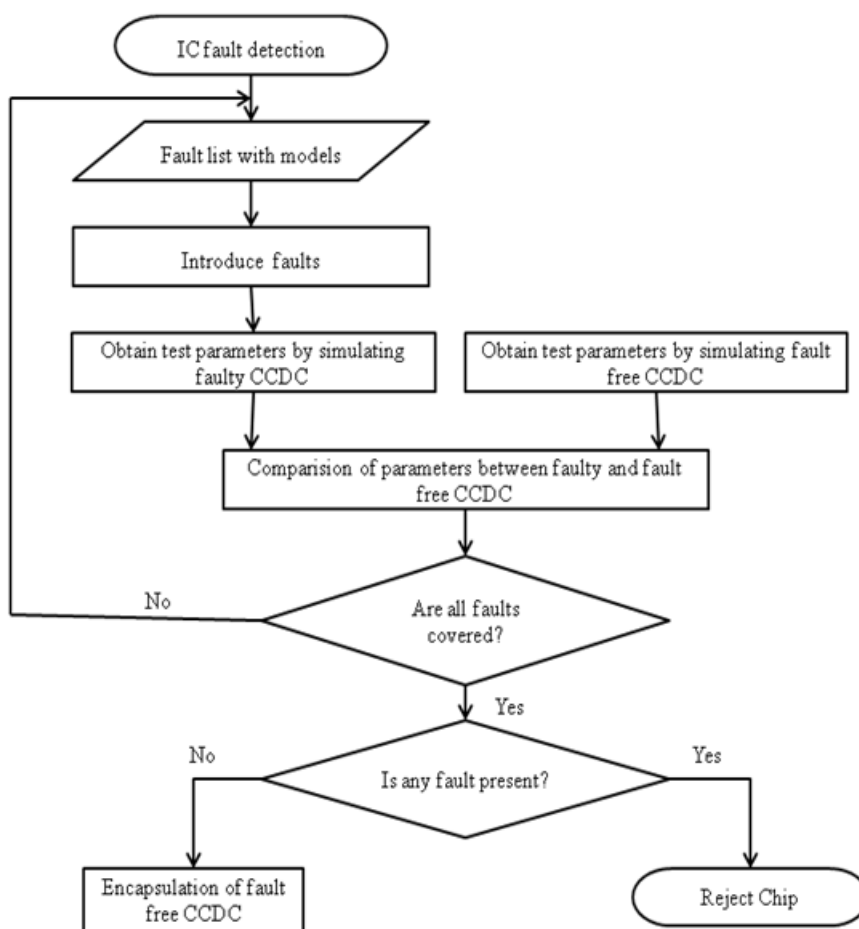


Fig. 6. Flow chart representation to detect faults in CCDC using OBIST method

IV. SIMULATION RESULTS AND ANALYSIS

OBIST methodology is used to detect stuck-at, open or short, gate delay faults in universal CMOS gates and CCDCs. The circuit is converted to an inverter by connecting all its inputs together. External resistor, capacitor and one extra inverter are used to have oscillatory behavior. To quantify the fault coverage, the circuit is induced with various faults and pulses provided in the fix time duration are measured.

A. Stuck at faults

Stuck at one fault is created at input or output if the corresponding pin is shorted with V_{DD} where as stuck at zero fault is created if the pin is shorted to ground. When stuck at fault is present, the circuit does not provide oscillations, number of pulses are zero, and this fault is very easily detected using proposed method.

B. Open and short faults

For open or short fault, all the outputs are not according to the truth-table of the circuit. In complex circuit 1, when source, drain of P channel MOSFET with input A is open, out of 32 input possibilities, for 9 possibilities the circuit provides false output. For short circuit between source and drain also for 9 possibilities this circuit could not give correct output. When the proposed OBIST method is used the fault-free complex circuit no1 provide 72 pulses in 100ms where as for open source or drain it provided 69 pulses and for shorted source and drain it provided 75 pulses. The number of pulses for fault-free and faulty circuit is different. Thus by counting pulses for fix time interval, whether the circuit has fault or not can be checked and there is no need to apply any test vector.

C. Simulation results of complex circuits

Universality for proposed method is shown by considering two complex digital circuits. Sixty six catastrophic faults and one hundred ninety two parametric faults are considered to check authenticity of proposed method. For presence of catastrophic fault, the circuit must be rejected. The number of pulses in 100 ms for different catastrophic faults are 69 or less and 75 or more. Hence, if pulse count is outside the range $< 70-74 >$, the chip is rejected

D. Gate delay faults

Due to process variation the threshold voltage, transconductance, channel length and width of P, N channel MOSFET, change; which manifests into change of propagation delay of circuits. The variation in propagation delay gives gate delay faults.

In integrated circuits, the worst case variation in these parameters is $\pm 20\%$. The channel resistance of MOSFETs is in direct proportion to L, V_T and is in inverse proportion to W, μ . The parameter variation which results in number of pulses outside 70 to 74 range will be rejected. For V_T the variation in number of pulses is more as the inverter threshold voltage of equivalent inverter changes which affects the charging-discharging voltage level. Hence when V_T is 15 to 20% even though the gate delay is within limit the chip gets rejected and there is yield loss. Table II shows number of pulses for variation of different parameters while yield loss for the circuits is tabulated in Table III. Monte Carlo analysis on each circuit is carried out for 50 runs to authenticate the results.

All catastrophic faults are detected by this method. The average yield loss of 12.5% is observed when change in threshold voltage of MOSFETs is 20%. There is no yield loss up to 10% tolerance band of gate delay faults. To reject circuits outside 10% tolerance band the number of pulses should be outside $< 71 - 73 >$ range.

In integrated circuits the maximum tolerance range of parameters is $\pm 20\%$. Possible parametric faults were simulated with varying L, W, μ, V_T values by $\pm 5\%$ and $\pm 10\%$ deviation from its maximum tolerance range. The simulation results in Table IV and V show that for $\pm 10\%$ deviation in parameters, 100% fault coverage with test escape 0% is obtained. For $\pm 5\%$ deviation the average fault coverage is 95.3% with test escape of 4.7%. The variation of different parameters and their effect on number of pulses for all these circuits is shown in Fig. 7.

TABLE II. No. of pulses in 100 ms simulation time for $\pm 5\%, \pm 10\%, \pm 15\%, \pm 20\%$ variation of different parameters

Variation in parameters	Complex circuit 1								Complex circuit 2							
	-20	-15	-10	-5	+5	+10	+15	+20	-20	-15	-10	-5	+5	+10	+15	+20
Fault free normal circuit	72								72							
ΔL_p	74	73	73	72	72	71	71	70	74	73	72	72	71	70	70	70
ΔL_n	74	73	73	72	72	71	71	70	73	72	72	72	72	71	71	71
ΔW_p	70	70	71	72	72	73	73	74	70	70	70	71	72	72	73	73
ΔW_n	70	70	71	72	72	73	73	74	71	71	71	72	72	72	72	73
$\Delta \mu_p$	70	71	72	72	72	72	73	73	70	70	70	71	72	72	73	73
$\Delta \mu_n$	70	71	72	72	72	72	73	74	70	70	71	71	72	73	73	74
ΔV_{TP}	76*	75*	74	73	71	70	69*	68*	76*	75*	74	73	71	70	68*	67*
ΔV_{Tn}	76*	75*	74	73	71	70	69*	68*	76*	75*	74	73	71	70	69*	68*

* Chip rejected (Yield loss)

TABLE III. Yield loss in percentage for four circuits at $\pm 15\%, \pm 20\%$ tolerance

Complex circuit 1		Complex circuit 2	
± 15	± 20	± 15	± 20
8.3	12.5	8.3	12.5

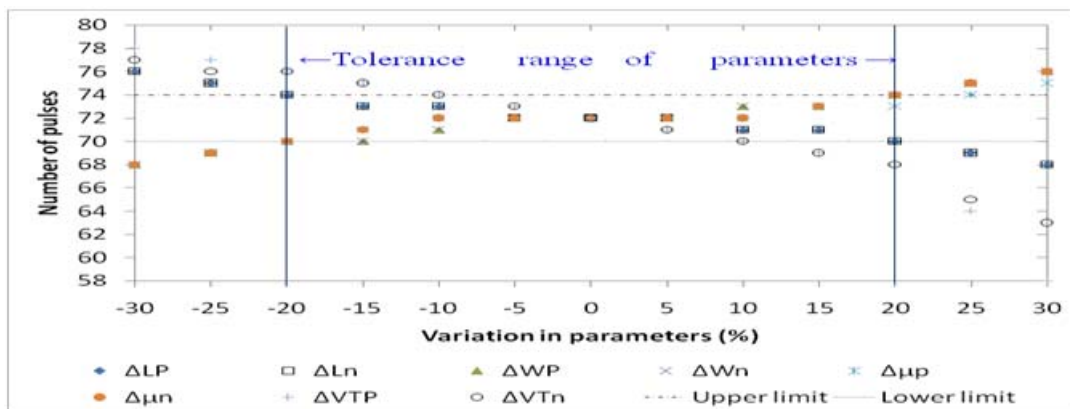
TABLE IV. No. of pulses in 100 ms simulation time considering parameter variation of $\pm 5\%$, $\pm 10\%$ outside $\pm 20\%$ tolerance range

Variation in parameters	Complex circuit 1				Complex circuit 2			
	-10	-5	+5	+10	-10	-5	+5	+10
ΔL_p	76	75	69	68	76	75	69	69
ΔL_n	76	75	69	68	76	75	69	69
ΔW_p	68	69	75	76	69	69	75	76
ΔW_n	68	69	75	76	69	69	75	76
$\Delta \mu_p$	68	69	74*	75	68	69	74*	75
$\Delta \mu_n$	68	69	75	76	68	69	75	76
ΔV_{TP}	78	77	64	58	78	77	62	58
ΔV_{Tn}	77	76	65	63	77	76	64	63

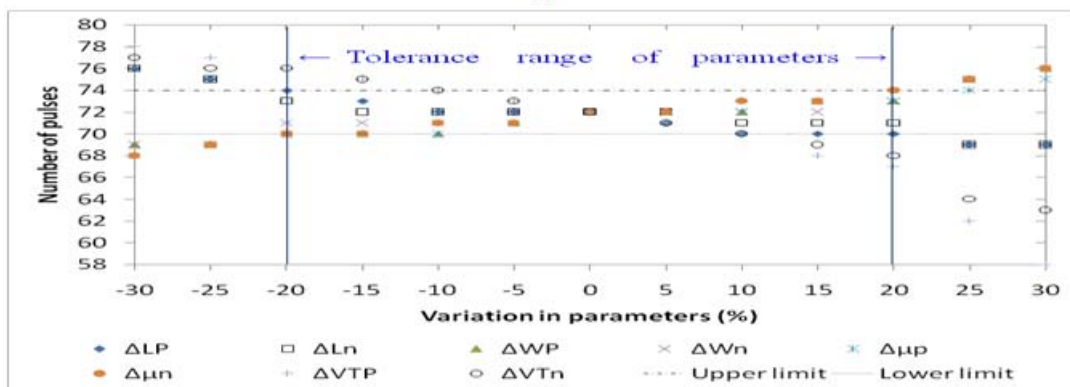
* Fault not detected (Test escape)

TABLE V. Fault coverage and test escape for $\pm 5\%$, $\pm 10\%$ parameter variation outside $\pm 20\%$ tolerance range

% variation \rightarrow	Complex circuit 1		Complex circuit 2	
	± 5	± 10	± 5	± 10
Fault coverage	93.75	100	93.75	100
Test escape	6.25	00	6.25	00



(a)



(b)

Fig. 7. Effect of parameter variation on number of pulses (a) Complex Circuit 1 (b) Complex Circuit 2

V. DISCUSSION

OBIST technique for finding faults in analog circuits is used in [1]-[13], but in this paper it is used for complex CMOS digital circuits. In integrated circuits the worst case process parameter variation for passive components is 20%. As the testing circuit for CCDCUT and FCCUT is built on same chip, the process parameter variation is identical for both. Due to this, change in number of pulses for both circuits will be identical. This effect is checked by changing R , C by $\pm 20\%$ in same direction as well as in opposite one. Even if component values of tester changes, the circuit provides authentic results. The N channel MOSFETs in inverter1 with aspect ratio 1 have ON resistance of 8 k Ω in linear mode. With change in technology the ON resistance of MOSFETs changes but external resistor R should be approximately 50 times ON resistance of MOSFET in linear mode. In experimental work for $R = 400$ k Ω and 500 k Ω the results are good. Hence 400 k Ω resistor is used to reduce area. The ratio W/L of pull up to pull down of equivalent inverter for all four circuits is adjusted 2 to have equal propagation delay time. Due to this all four normal circuits have provided 72 pulses in 100ms.

For higher W the equivalent ON resistance of MOSFETs reduces, the required R is less and more pulses are generated in stipulated time. This is verified for all four circuits. The used N channel MOSFETs in inverter1 with aspect ratio 10 have ON resistance of 800 Ω in linear mode and for $R = 40$ k Ω all normal circuits provided 72 pulses in 10ms.

The channel resistance is directly proportional to value of L , V_T and inversely proportional to value of W , μ . If all four parameters increase or decrease, the effect will counterbalance and variation in channel resistance is less. For 20% variation, the circuits will have gate delay within the threshold limit and the number of pulses are observed to be within the range of $< 70-74 >$. Hence, these circuits are not rejected; but if, there is a variation in L , V_T in one direction and W , μ in opposite direction it rejects even for 5% variation. This is because, the effect on channel resistance is maximum and the variation in gate delay is more, due to which the change in number of pulses is higher. All these effects are observed in the various circuits simulated in this work.

The designer has to adjust simulation time and evaluate the range of pulses so that all chips containing catastrophic faults are rejected. While doing experimental work, simulation time of 100 ms and number of pulses outside $< 70-74 >$ range are used to reject the circuits. This range depends on simulation time and the tolerance band required. Increase in simulation time provides better results.

VI. CONCLUSION

Detail analysis of OBIST method for CCDCs is presented in this paper. The obtained results clearly indicate that it has capability of testing faults in CCDCs. The merit of this method is that it can be used without an external vector or a complex response analyzer for detection of faults. A fault coverage of almost 100% is achieved for stuck-at faults, open or short faults. Time delay faults due to process variation are also detected. For 15% and more deviation in threshold voltage, the variation in number of pulses is higher which rejects even good chips, this gives yield loss of around 12.5%. For $\pm 10\%$ deviation in parameters outside tolerance range limit, 100% fault coverage is obtained with zero percent test escape. The simulation study demonstrates how the channel length, width of P channel N channel device can be adjusted to have circuits with equal propagation delays. Usage of an OBIST method to test both analog and digital parts in mixed signal IC, will eventually mitigate the area overhead and minimize the costs. This study further inspires in detail analysis for faults in different CMOS digital circuits.

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AUTHOR PROFILE



R. H. Khade Received BE degree in Electronics from Marathwada University, Aurangabad, India in 1987 and ME in Electronics from V.J.T.I. Mumbai, India in 1999. He is pursuing Ph.D. from NMU, Jalgaon, India. He is in teaching field from last 30 years.



Devendra S. Chaudhari obtained BE, ME from Marathwada University, Aurangabad, India and Ph.D. from Indian Institute of Technology Bombay, Mumbai, India. He has been engaged in teaching, research for period of about 30 years and worked on DST-SERC sponsored Fast Track Project for Young Scientists. He has worked as Head of Department Instrumentation, Electronics and Telecommunication in charge Dean (Academic), Dean (Quality Assurance) at Government College of Engineering, Amravati and Head of Department Electrical, Electronics and Telecommunication and Research, and incharge Principal at Government College of Engineering, Jalgaon. Dr. Chaudhari published several research papers including presentation in international conferences at Seattle, USA and Austria, Europe and Melbourne, Australia. He worked as Chairman /Expert Member on different committees of All India Council for Technical Education, New Delhi, Director of Technical Education, Mumbai for Approval, Graduation, Inspection, Variation of Intake of diploma and degree Engineering Institutions. As a university recognized Ph.D. research supervisor in Electronics and Computer Science Engineering he has been supervising research since 2001.