ISSN (Print) : 2319-8613
ISSN (Online) : 0975-4024

Study and Design of Standard PLL with Comparative Analysis between Current Starved VCO and Differential Pair VCO

Deepak Balodi[1], Arunima Verma[2] and P. A. Govidacharyulu[3] SMIEEE
[1]ANSAL Technical Campus, Lucknow, deepakbalodi@gmail.com
[2]Institute of Engineering and Technology (IET), Lucknow
[3]Vasavi College of Engineering, Hyderabad, India, pagovindacharyulu@yahoo.com

***Abstract*— This paper aims for the design of a Radio frequency (1.8GHz) low power (2.75mw) Phase Lock Loops (PLL) with a 0.35-µm CMOS technology. The comparison of Current Starved VCO and Differential pair VCO has been done and analyzed for low power and high frequency analysis respectively. Each component of PLL is designed and simulated in the Eldonet environment of Design Architect IC Station by Mentor Graphics in 0.35-µm technology. Both the standard configurations have been simulated under the same environment and results are analyzed for two most important VLSI constraints, Speed (High frequency range) and Power consumption. The high speed and locking performance of the Differential VCO has been evaluated against the lower power consumption benefit of Current starved based VCO.**

Keyword- VCO, PLL, Current Starved VCO, Phase noise, Charge pump

I. INTRODUCTION

Closed-loop frequency control system's functioning is based on the phase sensitive detection of phase and /or Frequency difference between the reference and output signals of the transceiver block. Voltage Controlled Oscillator (VCO) incorporated in the phase-locked loops (PLL) is the integral part of the frequency synthesizers and clock recovery circuits. PLL circuits have been used to demodulate FM signals for the long time, making obsolete the Foster-Seeley and radio detectors of the early years. A Voltage Controlled Oscillator finds variety of applications and therefore results in different architectural designs such as LC oscillator, Resonator circuit (using Ring architecture), Relaxation Oscillator etc. Due to better speed and higher stability in output oscillations, the differential amplifier based ring oscillator is used with less number of stages which results in reduced power consumption [1]. This crucial aspect of the differential amplifier configuration has inspired this work to remain focused around it. Further lower power dissipation can be obtained using some other configurations such as Partial Positive Feedback system and Ring Oscillator architecture [2]. LC tuned circuit based oscillators have proved their supremacy for the high frequency (microwave band) applications, but the advantage costs in terms of circuit complexity due to designing of inductors [3]; whereas a ring architecture has an added advantage of smaller area as compared to the LC oscillator. Ring oscillator shows an added advantage of wide tuning range also [4].

Since past many researches and publications came in focus whose realization differ in their frequency of operation, tuning range, phase noise characteristics, power consumption, circuit architecture and level of integration. Plenty of researches have been conducted in realizing a high lock range PLL with lesser lock time and power. There were papers on Mixed Signal Analysis and Low power design using technologies ranging from 600-nm to 22nm.

In this work, the design specification for 350nm technology has been chosen for having lesser high order effects and achieving higher Signal-to-Noise (S/N) ratio. The paper describes the design of 1.8GHz 2.75mW PLL that has been simulated with 0.35-µm CMOS technology in IC-Station (Mentor Graphics) on Eldo-Net simulator. Evolving from single stage oscillator, the PLL employs various circuit techniques to achieve high tunable frequency range with low power dissipation.

The main aim of the paper is to design and perform the comparative analysis on two different VCO design's aspect that are Current Starved VCO (CSVCO) and Differential Pair VCO (DAVCO) on the basis of tunable frequency range (speed), Power dissipation, tracking range and performance.

II. SCOPE FOR VARIOUS STRATEGIES' FORMATION

The standard architecture of PLL (shown in fig. 1), is a fairly standard topology. It consists of Phase Detector (PD), that generates an output signal which is proportional to the difference between the reference signal and the divided down signal, Charge Pump and Loop Filter to receive digital pulses and convert them into an analog control voltage Vcontrol, and a voltage-controlled oscillator (VCO) with the purpose of either speed up or speed down the feedback signal according to the error generated by PFD.

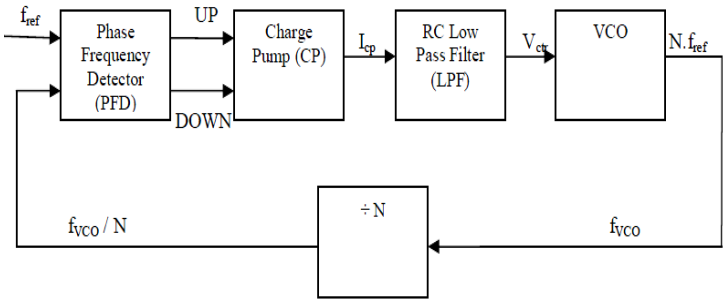

Fig 1: Phase-Locked Loop architecture

Instead of using the most basic phase detector which is simply an exclusive-OR gate, Phase Frequency Detector (PFD) has been employed here. It has been designed from D flip-flop which in turn is designed by using 2I/P and 3I/P NAND gates to eliminate the problem of locking onto harmonics of reference signal. Charge Pump with bootstrap buffer is incorporated in the design to overcome the issues of Charge Sharing, Mismatch between Drain Currents and Delay differences.

The design of PLL has evolved from a one-stage ring oscillator, and is described in a progression starting from the VCO circuit. This paper compares the design methodology, schematic complexities and performance of the two prescribed VCO's, CSVCO and Differential Pair VCO. The selection of the VCO depends upon the requirement of high tunable frequency range or low power design. The range of frequency of the PLL is concentrated by properly choosing the circuit architecture and parameters.

III. VCO ARCHITECTURE

A Voltage-controlled oscillator (VCO) is an electronic oscillator designed to be controlled in oscillation frequency by a voltage input. The most commonly used architecture for VCO in CMOS technology is voltage controlled ring type oscillator. It consists of several delay cells forming a closed loop. The study of previous researches post some challenges in the VCO design that is achieving high frequency to get wide tuning range, getting constant output swing (linearity) and stability of the design. The paper proposes the following two VCO designs are proposed that can be used according to the requirement:

A. Current Starved Voltage Controlled Oscillator (CSVCO)

The schematic view of the CSVCO has been shown in fig. 2. Its operation is very much similar to Ring oscillator. MOSFETs M2 and M3 are implemented to work as an Inverter and the current sourcing feature have been obtained from MOSFETs Ml and M4. The current sources Ml and M4 control and limit the current going to the inverter M2 and M3; in other words, the inverter is starved for current. The same drain currents of MOSFETs M5 and M6 are controlled by the input control voltage. The currents in M5 and M6 are mirrored in each inverter/current source stage.

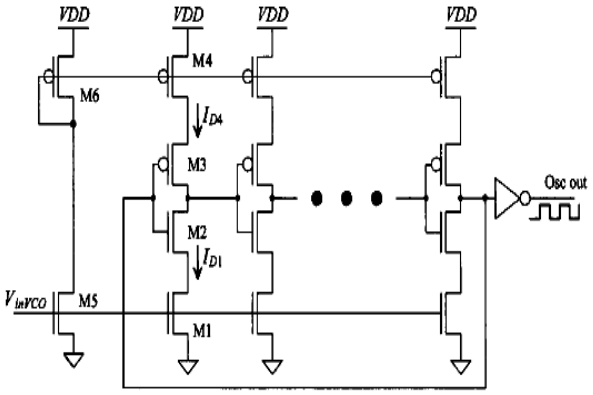

Fig 2: Current Starved VCO

B. Differential pair VCO

Ring oscillators have been widely used as VCO's in phase locked systems [5]–[7]. Providing a wide tuning range with relatively constant voltage swings, these oscillators also lend themselves to low-voltage operation. Differential VCO is also a ring type oscillator as shown in the basic block diagram in Figure 3.

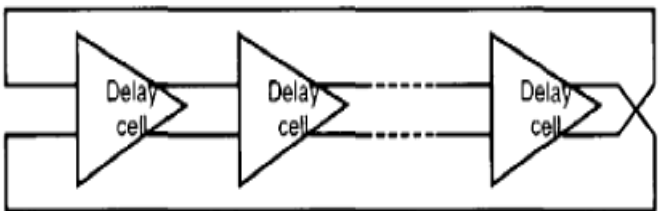

Fig 3: Ring type oscillator

The Differential VCO is designed to achieve high frequency range. The first step in designing the VCO was to design a delay cell. A delay cell consists of a basic differential operational amplifier. The two PMOS transistors in this delay cell were aimed to work in the linear region so as to act as variable resistors. This is necessary to monitor the output frequency by varying the resistance. This is because the frequency depends on the time constant of each delay cell, which is varied by changing the resistance. The remaining PMOS transistors were sized to operate in the saturation region. Here PMOS is driving circuit so we are using NMOS as active load. Figure 4 shows the schematic of a delay cell.

This type of delay cell has a major drawback as it cannot maintain a constant output swing. This occurs because as Vcontrol changes, Vout+ and Vout- will also change. This occurs because as Vcontrol changes, the resistance across the PMOS transistors always changes. A change in those points causes the output swing to vary, and thus introduces nonlinearity. The solution to this drawback was to create a control circuit. The main aim is to provide biasing current from internal circuitry rather than different biasing circuit for each stage. This makes design simpler. Vb1 and Vb2 from the control circuit control the current in each stage of the differential oscillator. Hence it controls the delay of each stage and therefore the oscillation frequency increases or decreases according to the variation in the delay of each stage.

The Vcontrol is given at the lower part of the control stage circuit and to the active load of each ring differential stage. More number of stage result in lowering frequency range as frequency is inversely proportional to two times delay of all stages and the low number in stage is unstable. From the view point of speed-power trade-off, it is desirable to decrease the number of stages in a ring to the extent possible, so in these design seven stages of ring differential pair is used. Figure 5 shows the schematic of Differential VCO where the control voltage can be seen before the differential stage which is used for biasing all the seven stages.

The output clock frequency is determined by the delay of each delay cell which in turn is controlled by control voltage. A wide frequency range of oscillator means a wide tuning range of each delay cell. The delay cell is usually a differential pair with a tail current and some active loading. The delay of each cell is controlled by the tail current.

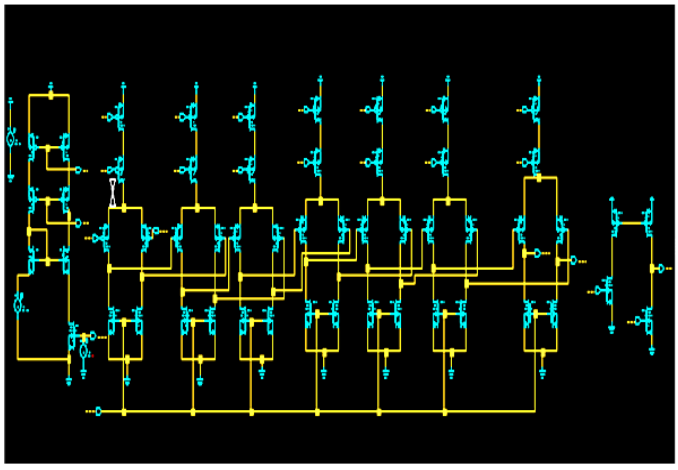

Fig 4: Proposed schematic design of differential pair ring VCO.

There are some difficulties associated with this architecture in order to achieve the wide tuning range. By using a single tail current, the tuning range is limited by the control voltage range. The control voltage is usually constraint by the power supply voltage, i.e. $0 \leq$ Vcontrol $\leq$ Vdd, where Vdd is the supply voltage, a constraint associated with the design technology. If we choose the small tail current, the tail current is still not large enough even that the control voltage reach the up limit so that the high end frequency range of VCO is small. On the other hand, if we choose the large tail current, the tail current is still large even that the control voltage reached the lower limit so that the lower end frequency range of VCO is large [8].

IV. EXPERIMENTAL RESULTS

The design of PLL that was chosen here was Digital PLL which incorporated both analog and digital counterparts. The digital part was PFD and divider network. The PFD was analyzed to detect both phase and frequency and using 2 and 3 input NAND gates; the problem of locking onto harmonics was eliminated. With the improved Charge Pump design, the work has been successful in obtaining stable and high frequency outputs with a very low phase noise. Also the power was significantly reduced by proper sizing of Divider network transistors and employing it in Master Slave pattern. Both the VCO's that were discussed in previous section were designed separately and employed in the design of PLL at the place of oscillator block. For the VCO's, performance characteristics and comparison of PLL is drawn.

With lesser complexity and lesser number of stages in the oscillator design the Current Starved VCO results into the low power consumption design whereas with total 7 stages in the differential pair VCO along with the control stage employed for internal biasing results in complex and comparatively high power consuming design, although both the designs succeeded in achieving wide tunable frequency range. Differential pair VCO operates at higher range of frequency whereas Current Starved VCO operates at comparatively lower frequency range. From the simulations, the Differential pair VCO shows high frequency gains near to 900MHz/V whereas the Current Starved VCO is limited in mid-50's MHz/V. The proposed design has succeeded in achieving small settling time and locking time, this show that the proposed PLL design acquires locking stage very fast in comparison to other PLLs thus can be called as fast acquisition Digital PLL.

Both the proposed designs have been implemented and simulated under the common simulation platform. The comparative results have been discussed under following major concerns:

a) High speed (frequency of Operation)
b) Low power dissipation
c) Linear response (frequency Vs Vcontrol)
d) Locking time

A. Output frequency and Linearity

One of the most important aspects of VCO design that is the output oscillation's linearity with respect to the input tuning Voltage (Vcontrol) has been plotted in fig. 5 and fig. 6.

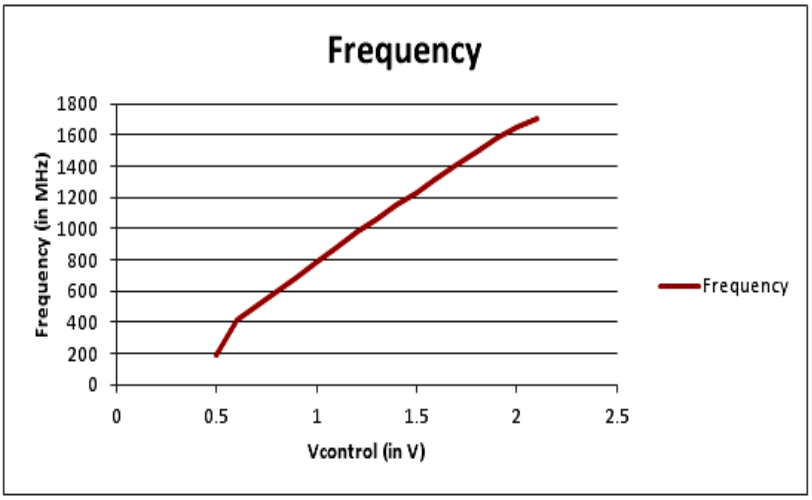

Fig 5: Differential VCO characteristic curve

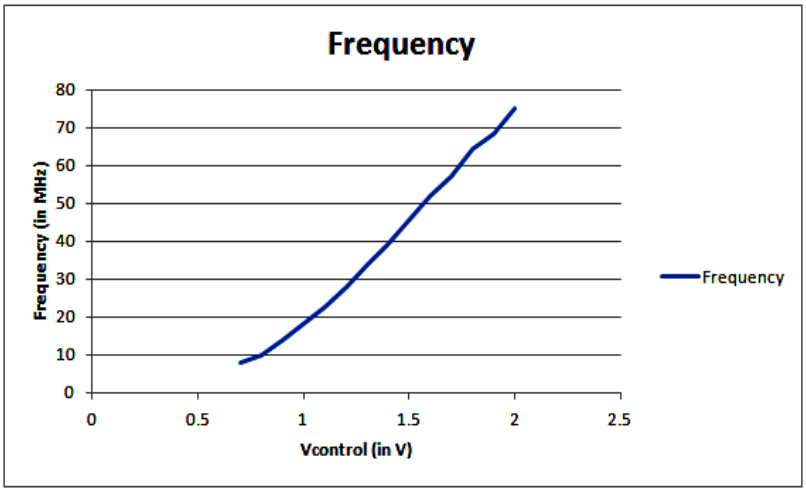

Fig. 6: Current Starved VCO characteristic curve

Here one can observe for the Differential VCO PLL that the linear range is far more extended in GHz than the Current Starved structure. A significant difference in highest frequency operation and fairly larger linear range of differential amplifier must be appreciated.

B. PLL Power Consumption

Table: 1 shows the amount of power consumed by various component of Differential VCO PLL (DA-VCO) fig. 7 explains the same in pie-chart diagram format, for the Current Starved VCO PLL (CS-VCO).

Table 1 Power Consumed in Differential VCO PLL

Component	Power Consumed (mW)
VCO	49.21
PFD	0.3
CHARGE PUMP	4.2
FREQUENCY DIVIDER	0.25

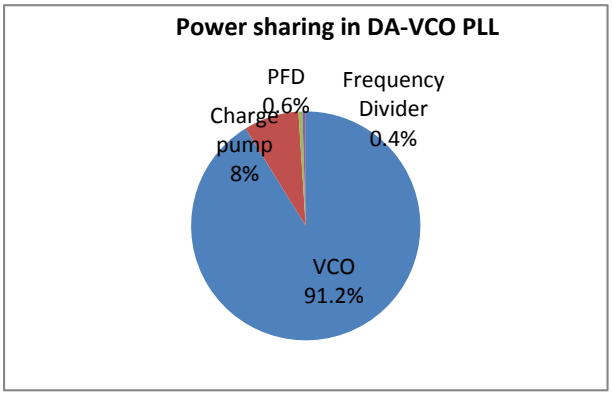

Fig. 7: Power Consumed in Differential VCO PLL

For DA-VCO PLL, VCO itself consumes the maximum power of 91% of the total PLL design. The lowest power is consumed by Frequency divider. It only consumes about 0.4% of total power. Charge pump consume 8% power while PFD consume 0.6% of the total power (Fig. 7).

Table 2 shows the amount of power consumed by various component of Current Starved PLL, where VCO consumes maximum power of 58%. The lowest power is consumed by Frequency divider again which is about 9% of total power. Charge pump consume 22% power while PFD consume 11% power.

Table 2 Power Consumed in Current Starved VCO PLL

Component	Power Consumed (mW)
VCO	1.54
PFD	0.3
CHARGE PUMP	0.58
FREQUENCY DIVIDER	0.25

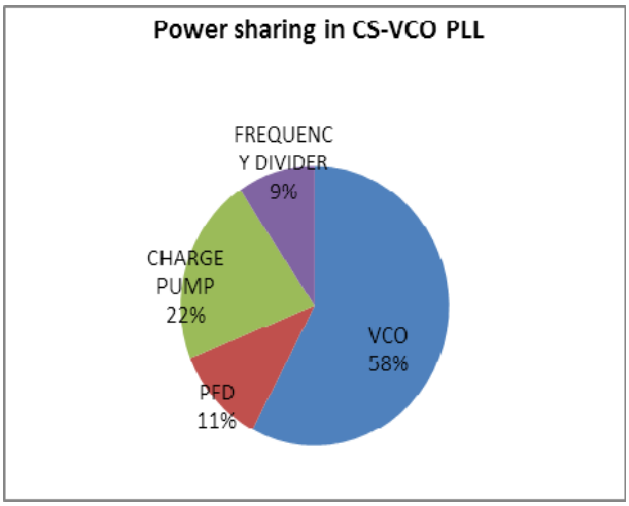

Fig. 8: Power Consumed in Differential VCO PLL

The Power consumption of Differential pair VCO and PLL is much higher than PLL using Current starved VCO due to large number of transistor used. In this design VCO consume about 91% of total power while power consumed by frequency divider is almost negligible. Charge Pump consume 8% of total power while PFD 1% as shown in fig. 8.

Thus total power consumption of Differential Amplifier PLL is about 54.91 mW, whereas only 2.67 mW by Current Starved PLL. This result clearly appreciates the lowest power consumption property of CMOS inverter design for Current Starved VCO.

V. CONCLUSION

The paper discusses the comparison and implementation of two designs of VCOs. Current starved ring comes out with the superior performance in form of its low power consumption and wide tunable frequency range whereas the differential pair VCO is considered for its high frequency and wide tunable frequency. It has been analyzed that the designed PLL using current starved VCO consumes 2.75 mW power from 1.3 V supply and have a smaller lock time. PLL using differential VCO consume 54.91 mw. The curve of differential VCO is linear in range of 400 MHz and 1.72MHz. So the centre Frequency is about 1 GHz, and wide tunable range is achieved using it.

Therefore for the speed and linearity concern, Differential architecture for VCO proves to be a better choice, especially for the fast communication devices, whereas the demanding need of lower power consumption for the remote wireless circuits still finds the Current starved VCO as a more prominent configuration. With the improved Charge Pump design, one is able to obtain stable and high frequency outputs with a very low phase noise. Also the power could be significantly reduced by proper sizing of Divider network transistors and employing it in Master Slave pattern.

REFERENCES

[1] Y. A. Eken and J.P. Uyemura, “A 5.9 Ghz Voltage Controlled ring oscillator in 0.18 µm CMOS” IEEE J. Solid State Circcuits, Volume 39, pp 230-233, Jaan. 2004.
[2] Narasi Reddy, Manisha Pattanaik and S. S. Rajput, “0.4 V CMOS based Low Power Voltage Controlled Ring Oscillator for Medical Applications” IEEE Tencon 2008, Volume 1, pp. 1-5, Jan. 2009.
[3] B. Razavi, “A study of phase noise in CMOS oscillators,” IEEE J. Solid State Circuits, Volume 31, pp. 331-343, Mar. 1996.
[4] S. Docking, M. Sachdev, “An Anlytical Equation for the oscillation frequency of High frequency Ring Oscillators,” IEEE Journal of Solid State Circuits, Volume 39, 2004, pp. 533-537.
[5] Ms. Ujwala A. Belorkar and Dr. S.A.Ladhake,“Area efficient 3.3ghz phase locked loopwith four multiple output using 45nm vlsi technology”, International Journal of VLSI design & Communication Systems (VLSICS) Vol.2, No.1, March 2011.
[6] Miljan Nikolić, Milan Savić, Predrag Petković, “The Self-Bias PLL in Standard CMOS”, electronics’ 2007 19 – 21 September, Sozopol, BULGARIA.
[7] Dean Bannerjee, PLL Performance, Simulation & Design, Edition 5, Reprint 2010.

[8] B. K. Mishra, Sandhya Save, Swapna Patil, "Design and Analysis of Second and Third Order PLL at 450MHz", International Journal of VLSI design & Communication Systems (VLSICS) Vol.2, No.1, March 2011
[9] Behzad Razavi, "Design of Analog CMOS Integrated Circuits." McGraw-Hall, 2010.A. Karnik, "Performance of TCP congestion control with rate feedback: TCP/ABR and rate adaptive TCP/IP," M. Eng. thesis, Indian Institute of Science, Bangalore, India, Jan. 1999.
[10] Po-Yao Ke and Jon Guerber, "A 1.3V Low Power Divide by 4 PLL Design with Output Range 0.5GHz-1.5 GHz", ECE 599, Fall 2009.
[11] Sean M. Garrison, "A Voltage Controlled Oscillator for a Phase-Locked Loop Frequency Synthesizer in a Silicon-on-Sapphire Process", March 2009.
[12] Prof. H. Jackel, "Design of a 5 GHz PLL in CMOS", Institute for Electronics, Sommersester 2002.
[13] D. J. Young, S. J. Mallin, and M. Cross, "2 GHz CMOS Voltage-Controlled Oscillator with Optimal Design of Phase Noise and Power Dissipation", Department of Electrical Engineering and Computer Science, Case Western Reserve University.
[14] Chih-Ming Hung, Brian A. Floyd and Kenneth K., "A Fully Integrated 5.35-GHz CMOS VCO and a Prescalar", Department of Electrical and Computer Engineering, Silicon Microwave Integrated Circuits and Systems Research Group.
[15] Sijie Zheng and Lili He, "The Mixed-Signal Design of PLL with CMOS Technology", Department of Electrical Engineering, San Jose State University
[16] Yalcin Alper Eken, Student Member, IEEE, and John P. Uyemura, Senior Member, IEEE, "A 5.9-GHz Voltage-Controlled Ring Oscillator in 0.18-_m CMOS", IEEE journal of solid-state circuits, vol. 39, no. 1, January 2004
[17] Behzad Razavi, "Design of High-Speed, Low-Power Frequency Dividers and PLLs in Deep Submicron CMOS", IEEE Journal of Solid-State Circuits, Vol. 30.Year 1995.

AUTHOR PROFILE

Deepak Balodi: An assistant professor at ANSAL Technical Campus-Lucknow (affiliated to AKTU-Lucknow) possesses a rich experience of teaching and research of more than 10 years in Analog and mixed signal circuit design and implementation. He has more than 10 publications including two books in the field of Electronics and communication.

Arunima Verma: An assistant professor at IET-Lucknow (affiliated to AKTU-Lucknow) possesses a vast experience of teaching and research of more than 17 years in Electrical and control system design. She has more than 25 publications of International repute in her credit.