

A Fastest RISC Processor using Convolution Method

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Abstract— The guideline set comprises of Logical, Numerous calculations have been configuration with a specific end goal to fulfill an enhanced the execution of the channels by utilizing the convolution outline. The engineering of the proposed RISC CPU is a uniform 32-bit guideline organize, single cycle non-pipelined processor. It has stack/store engineering, where the operations might be performed on registers, and not on memory areas. It takes after the traditional von-Neumann design with only one regular memory transport for both directions and information. An aggregate of 27 guidelines are composed in beginning advancement venture of the processor. Immediate, Jump, Load, store and HALT kind of direction. The joined points of interest RISC processor, for example, rapid, low power, region proficient and operation-particular outline conceivable outcomes have been dissected.

In this paper we have actualized 32 bit RISC processor to perform round convolution at various modules of RISC processor like execute unit alongside ALU, Instruction get alongside guideline memory, decipher unit, resistor unit, information memory has been executed.

The execution time to perform 4 bit round convolution is observed to be 270 ns. The execution time to execute the direction is observed to be 5 ns. In our paper, 3200 LUTs and 320 rationale components are utilized to execute 32 bit RISC processor which is observed to be territory effective when contrasted with different plans.

Keywords- Area Efficient Circular Convolution, RISC Processor.

INTRODUCTION:

I. TODAY

RISC Cpus (and microcontrollers) speak to most by far of all Cpus being used. The RISC outline procedure offers control in even little sizes, and in this manner has come to totally overwhelm the market for low-control "implanted" Cpus. Installed Cpus are by a long shot the biggest market for processors. RISC had likewise totally assumed control over the market for bigger workstations for a great part of the 90s. After the arrival of the Sun SPARC station alternate sellers raced to contend with RISC based arrangements of their own. Indeed, even the centralized computer world is currently totally RISC based. The reasons have been the preferences, for example, its basic, adaptable and settled guideline organize and hardwired control rationale, which clears for higher clock speed, by taking out the requirement for microprogramming. The consolidated focal points of rapid, low power, zone effective and operation particular plan conceivable outcomes have made the RISC processor general [9]

1. LITERATURE REVIEW

Reference [1] proposed a plan system of a solitary clock cycle MIPS RISC Processor utilizing VHDL to facilitate the depiction, confirmation, reproduction and equipment acknowledgment. The RISC processor has settled length of 32-bit directions in light of three diverse arrangement R-organize, I-configuration and J-design, and 32-bit broadly useful registers with memory expression of 32-bit. The MIPS processor is isolated into five phases: guideline get, direction unravel, execution, information memory and compose back. The control unit controls the operations performed in these stages. Every one of the modules in the outline are coded in VHDL, as it is exceptionally helpful device with its idea of simultaneousness to adapt to the parallelism of computerized equipment. The top-level module associates every one of the phases into a more elevated amount. When identifying the specific methodologies for information, yield, principle piece and diverse modules, the VHDL portrayals are go through a VHDL test system, trailed by the planning examination for the approval, usefulness and execution of the assigned outline that show the adequacy of the outline

Reference [2] proposed processor which has Harvard design and comprises of 24-bit address, 5-organize pipeline direction execution, and inside troubleshoot rationale. ADPCM vocoder and SOLA calculation are effectively completed on the processor made with FPGA. variety), MP3 disentangling. At last it was executed in 0.5 μ m CMOS process and it did effectively those calculations.

Reference [4] has proposed a 32 bit RISC Processor for implanted application is introduced. Regarding impediment of force and range in installed framework, RISC Processor is purposely designed. Dual-issue innovation is embraced to enhance the execution; the mind boggling rationale of the dynamic booking calculation is allotted into various pipeline stage to enhance the recurrence.

Reference [3] deals with outline and check of a 32-bit broadly useful chip which is good with ARM7 RISC Core, is portrayed. In the design perspective, the processor has 3-arrange pipeline, 6 enlist banks, 32-bit ALU, and 4-cycle MAC. The center portrayed here was outlined by hook base for low power and low unpredictability. Bring down power outline strategy is utilized to diminish the entire power. The processor is actualized by SMIC 0.18 um CMOS innovation. It contains very nearly 5 million transistors; the center recurrence is 266 MHz and the power is around 1.3 w under it. The installed VxWorks OS can keep running on it steadily. The execution investigation of the RISC processor is likewise given. As indicated by the implanted benchmark program, the normal IPC of the RISC processor is almost 1.5.

Reference [5] has depicted the engineering and plan of the pipelined execution unit of a 32-bit RISC processor. Association of the pieces in various phases of pipeline is done in a manner that pipeline can be timed at high recurrence. Control and forward of 'data stream' among the stages are taken care by committed equipment rationale. Distinctive squares of the execution unit and reliance among themselves are clarified in subtle elements with the assistance of applicable piece outlines. The plan has been demonstrated in verilog HDL and utilitarian confirmation strategies received for it have been portrayed altogether. Combination of the outline is completed at 0.13-micron standard cell innovation and for moderate planning library the reported recurrence of operation is 714 MHz at blend level.

Reference [6] has proposed the design and actualize programmable video flag processor committed as building square of a different direction various data(MIMD) based transport associated multiprocessor framework is exhibited. The framework can either be developed from a few single processor chips, or it can be incorporated on vast territory coordinated circuit containing a few processors. The Processor permits a proficient execution of various video coding principles like H.261, H.263 and MPEG-1& MPEG-2. It comprises of RISC Processor supplement by a coprocessor for calculation serious convolution like undertakings, which gives a pinnacle execution of more than 1 giga-number juggling operations every second (GOPS).The extensive territory coordinated circuit incorporating 9 processor elements(PE's) on a zone of 16.6 cm/sups² has been planned. Because of yield contemplations repetition ideas have been actualized that even within the sight of generation imperfections bring about working chips using a lower number of PE's. Every PE has worked in individual test (BIST) capacities, which take into account a free trial of itself under the control of its incorporated blame tolerant BIST controller.

Flawed PE's are turned off. Just the PE's passing the BIST is utilized for video handling undertakings. Models have been manufactured in a 0.8/splmu/m reciprocal metal-oxide semiconductor (CMOS) handle organized by covers utilizing wafer venturing with covering exposures. Utilizing excess, up to 6 PE's for each chip were utilitarian at 66 MHz, along these lines giving a pinnacle number juggling execution of up to 6 GOPS.

Reference [7] has display a parallel MAC (duplicate gathering) engineering is intended for DSP applications on a 200 MHz, 1.6-GOPS Multimedia RISC Processor. The information way engineering of the processor is intended to acknowledge parallel execution of an information exchange and SIMD parallel number-crunching operations. SIMD parallel 16-bit MAC guidelines are presented with a symmetric adjusting plan which expands the precision of the 18-bit gathering. This parallel 16-bit MAC direction on a 64-bit information way is appeared to be productively used for DSP applications, for example, convolution in the mixed media RISC processor. By utilizing the parallel MAC guideline with the symmetric adjusting plan, the two-dimensional backwards discrete cosine change (2D-IDCT) which fulfills IEEE 1180 can be executed in 202 cycles.

Reference [8] examines a VLSI based multiprocessor engineering for constant handling of video coding applications. The design comprises of numerous indistinguishable handling components and is portrayed as MIMD (different direction various information). The engineering of a preparing component depends on a standard processor center, e.g., a RISC processor, and a low-level coprocessor. The low-level coprocessor is adjusted to parallel preparing of convolution like operations. The execution of the design is talked about regarding the preparing time for half breed coding calculations and in addition to the required silicon range.

Reference [9] has been introduced 16-Bit non-pipelined RISC Processor for its application towards convolution application. Novel viper and multiplier structures have been utilized in the RISC design. This paper has developed the utility of the processor towards convolution application. The recreations portray the aggregate dispersed power by the processor to be roughly 329.3 μ W with the aggregate zone of 65012 nm².

Reference [11] has talks about 64 bit RISC Processor on FPGA with implicit individual test (BIST) highlight executed utilizing VHDL .The creator exhibit the engineering, information way and direction set (IS) of the RISC processor. The 64-bit processors, then again, can address tremendous measures of memory up to 16Exabyte s. The proposed configuration can discover its applications in high arranged automated work-stations, for example, convenient pong gaming units, advanced cells, ATMs.

In this work we are actualized rapid, range proficient 32 bit RISC processor to perform round convolution on a FPGA Implementation of processor that comprises of a few squares, for example, execute unit alongside ALU, direction bring alongside guideline memory, translating rationale, control unit, information memory and program memory. Our goal is to outlined processor engineering for RISC sort of direction set with one cycle operation which is adjusted for convolution operation.

Whatever is left of the paper is sorted out as takes after. Segment III Present plan of the RISC CPU. Segment IV show outline RISC Processor For roundabout convolution. Area V gives Simulation consequence of outline RISC Processor for roundabout convolution. Segment VI gives examination result with different references segment. Segments VII finish up

II. DESIGN OF 32 BIT RISC CPU

A.Architecture

The engineering of the proposed RISC CPU is a uniform 16-bit direction design, single cycle non-pipelined processor appeared in figure 1. It has a heap/store engineering, where the operations may be performed on registers, and not on memory areas. It takes after the established von-Neumann design with only one basic memory transport for both guidelines and information. A sum of 27 guidelines are planned as an initial phase during the time spent advancement of the processor. The direction set comprises of Logical, Immediate, Jump, Load, store and HALT sort of guidelines [9].

B. Detail of Logical Blocks

Figure 1 shows the square outline of the 32-bit RISC CPU. The proposed RISC CPU comprises of five pieces, to be specific, Arithmetic and Logical Unit (ALU), Program Counter (PC), Register document (REG), Instruction Decoder Unit (IDU) and Clock Control Unit (CCU). The information way of the proposed CPU in Fig. 1 is clarified as takes after [9].

1)Program Counter: The Program Counter (PC) is a 32-bit lock that holds the memory address of area, from which the following machine dialect guideline will be brought by the processor. It is a 6-bit pointer to demonstrate the guideline memory. It also utilizes a 6-bit pointer to indicate the information memory, which will be utilized just when a Load/Store guideline is experienced for execution..

2) Arithmetic and Logic unit:

The number-crunching and rationale unit (ALU) performs math and rationale operations. It additionally plays out the bit operations, for example, pivot and move by a characterized number of bit positions. The proposed ALU contains three sub-modules, viz. number juggling, rationale and move modules. The math unit includes the execution of expansion and duplication operations and produces Sign banner and Zero banner. The move module is utilized for executing guidelines, for example, turn and move operations [9]

3) Register File:

The enlist record comprises of 8 broadly useful registers of 32-bits limit each. These enlist documents are used amid the execution of math and information driven directions. The heap guideline is utilized to stack the qualities into the registers and store direction is utilized to recover the qualities back to the memory to acquire the handled yields once more from the processor.

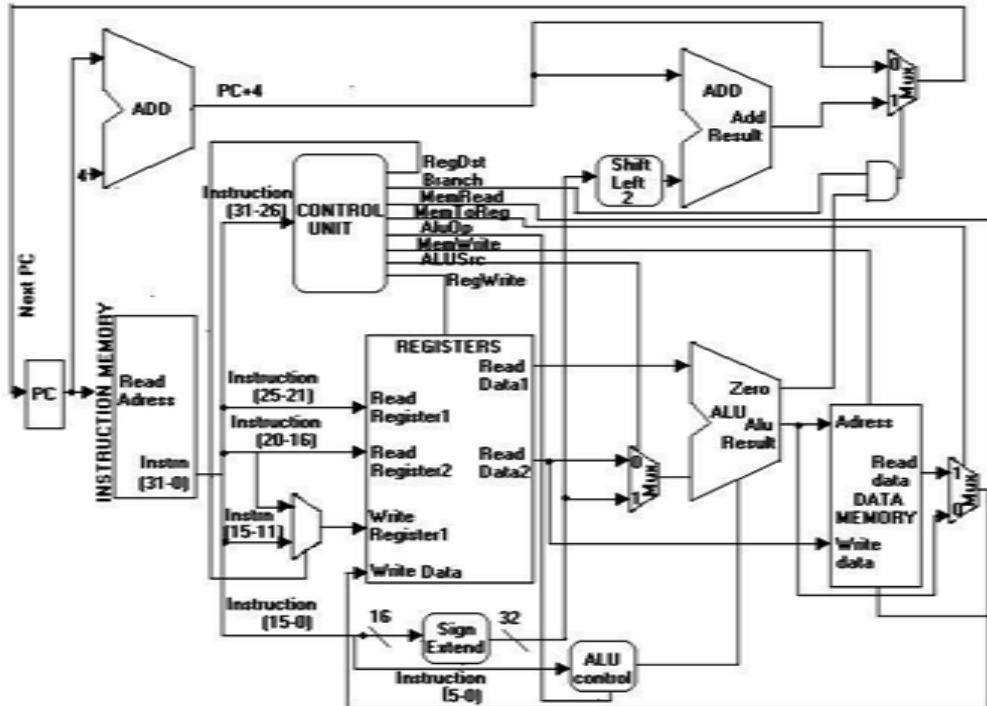


Fig. 1: Processor Architecture

4) *Instruction fetch unit*

The capacity of the direction get unit is to get a guideline from the guideline memory utilizing the present estimation of the PC and augmentation the PC esteem for the following direction as appeared in Figure 1.1 Since this outline utilizes a 8-bit information width we needed to execute byte tending to get to the registers and word deliver to get to the guideline memory of the MIPS single cycle processor[10].

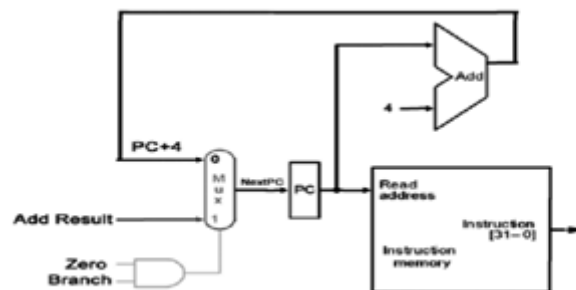


Fig 1.1 MIPS Instruction Fetch Unit (Source [10])

5) *Instruction decode unit*

The fundamental capacity of the direction unravel unit is to utilize the 32-bit guideline gave from the past direction get unit to list the enlist record and get the enroll information values as found in Figure 1.2 This unit likewise sign stretches out direction bits [15-0] to 32-bit. However with our outline of 8-bit information width, our execution utilizes the guideline bits [7-0] bits rather than sign augmenting the esteem. The rationale components to be actualized in VHDL incorporate a few multiplexors and the enroll document [10].

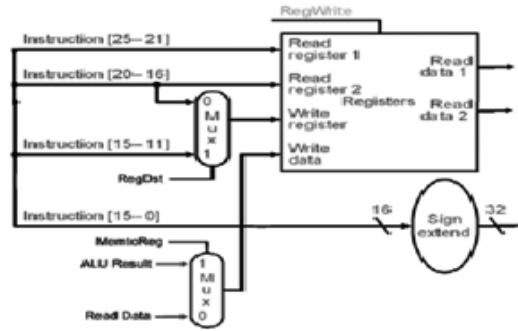


Fig 1.2 MIPS Instruction Decode Unit (Source [10])

6) *The control unit*

The control unit of the MIPS single-cycle processor looks at the direction opcode bits [31–26] and interprets the guideline to produce nine control signs to be utilized as a part of the extra modules as appeared in Figure 1.3. The RegDst control flag figures out which enlist is composed to the enroll document. The Jump control flag chooses the bounce deliver to be sent to the PC.

The Branch control flag is utilized to choose the branch deliver to be sent to the PC. The Mem Read control flag is affirmed amid a heap direction when the information memory is perused to stack an enroll with its memory substance. The Mem toReg control flag figures out whether the ALU result or the information memory yield is composed to the enroll document. The ALUOp control signals decide the capacity the ALU performs. (e.g. furthermore, or, include, sbu,slt) The MemWrite control flag is stated while amid a store direction when a registers esteem is put away in the information memory. The ALUSrc control flag figures out whether the ALU second operand originates from the enlist document or the sign augment [10].

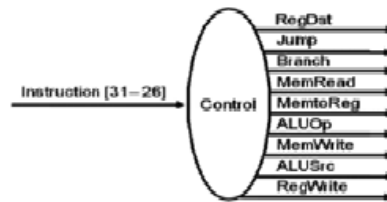


Fig. 1.3: MIPS Control Unit

7) *Execution unit*

The execution unit of the MIPS processor contains the math rationale unit (ALU) which plays out the operation dictated by the ALUop flag. The branch address is ascertained by adding the PC+4 to the sign developed quick field moved left 2 bits by a different snake. The rationale components to be actualized in VHDL incorporate a multiplexor, a viper, the ALU and the ALU control as appeared in Figure 1.4[10].

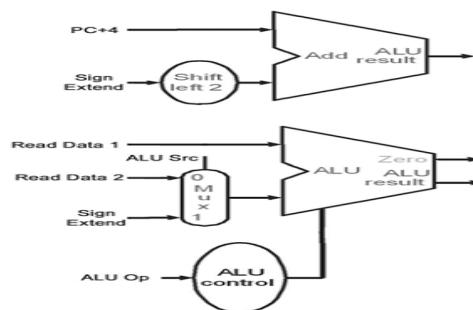


Fig 1.4: MIPS execution unit (Source [10])

8) Data Memory Unit

The information memory unit is just gotten to by the heap and store directions. The heap direction affirms the MemRead flag and uses the ALU Result esteem as a deliverer to record the information memory. The read yield information is then along these lines composed into the enroll document. A store guideline declares the MemWrite flag and composes the information esteem already read from an enlist into the figure memory-address [10].

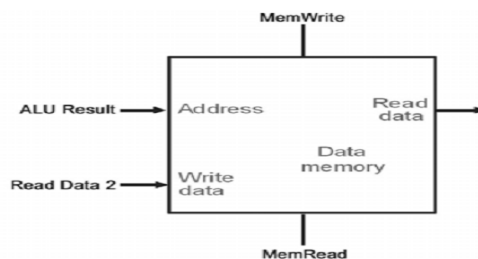


Fig 1.5 MIPS Data Memory unit

III. IMPLEMENTATION OF CIRCULAR CONVOLUTION

Dissimilar to the FPGA usage mind must be taken about the edge of an edge. Min and max operations are utilized to guarantee that a memory address doesn't surpass the edges of an edge thus leave the address go. Be that as it may one can execute diverse bits of the code contingent upon current. pixel areas, to lessen this overhead. The general structure is again like that for the FPGA. For genuine execution we have experienced after three procedures

1. Rotate and Shifting

In this procedure the information stream is moved by the move guideline from the processor. The information stream is moved from one digit as appeared in taking after grid

$$\begin{aligned} y(0) & 1 \ 1 \ 0 \ 2 \ 2 \\ y(1) & 2 \ 1 \ 1 \ 0 \ 3 \\ y(2) & 0 \ 2 \ 1 \ 1 \ 4 \\ y(3) & 1 \ 0 \ 2 \ 1 \ 5 \end{aligned}$$

Let $x_1(n) = \{2,3,4,5\}$ and $h_1(n) = \{1,2,0,1\}$

Then according to the formula of circular convolution

$$f(n) = \sum_{n=0}^{N-1} x_1(n) \cdot h_1(n-k)$$

2. Multiplying

In this procedure the information is increased by the duplicate guideline from the processor. The information is increased by every line to segment from the above network.

3. Adding

In this procedure the information is included a tiny bit at a time by the include direction from the processor. The information is including as appeared in the above lattice (1). Result is appeared from the reproduction of roundabout convolution handle

Simulation consequence of plan RISC processor for flow convolution.

The RISC processor design was reenacted on Altera Quartus-II Version 7.0. The reenactment results are found as taking after

I. *RTL views and simulation results of RISC PROCESSOR*

1) *Control unit*

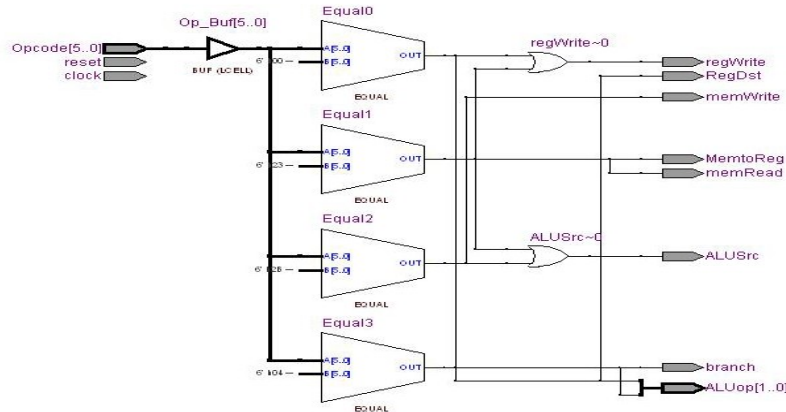


Fig 2.1 RTL view of control unit

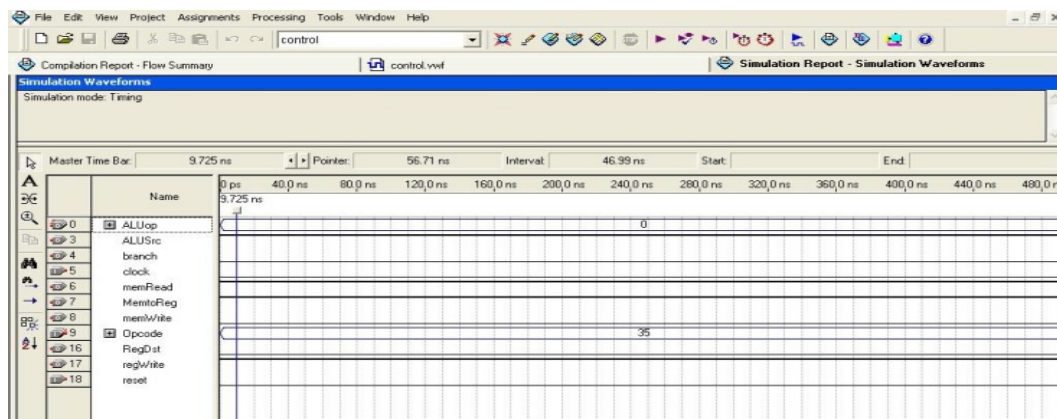


Fig 2.2 Simulation of control unit

2) *Data memory*

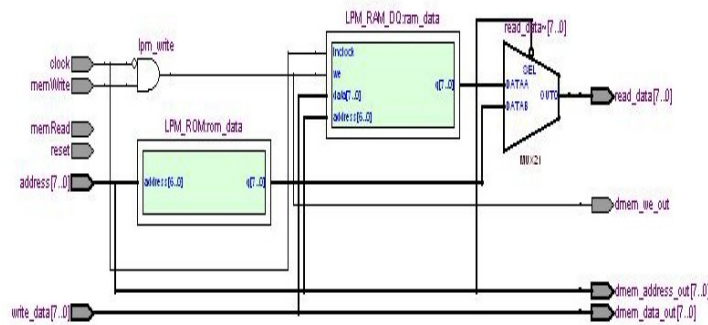


Fig 2.3RTL view data memory unit

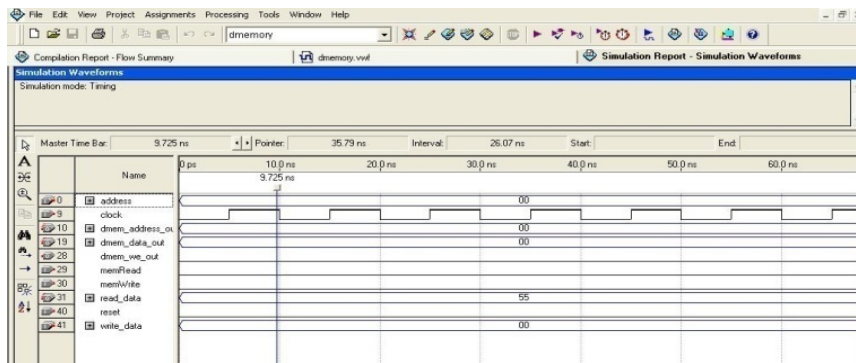


Fig 2.4 Simulation of data memory unit

3) *Instruction unit*

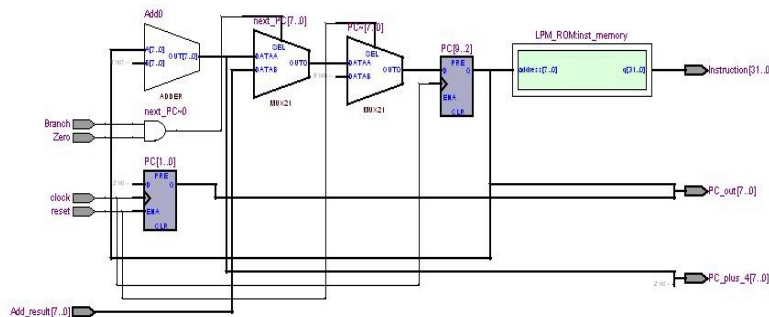


Fig 2.5 RTL view Instruction fetch unit

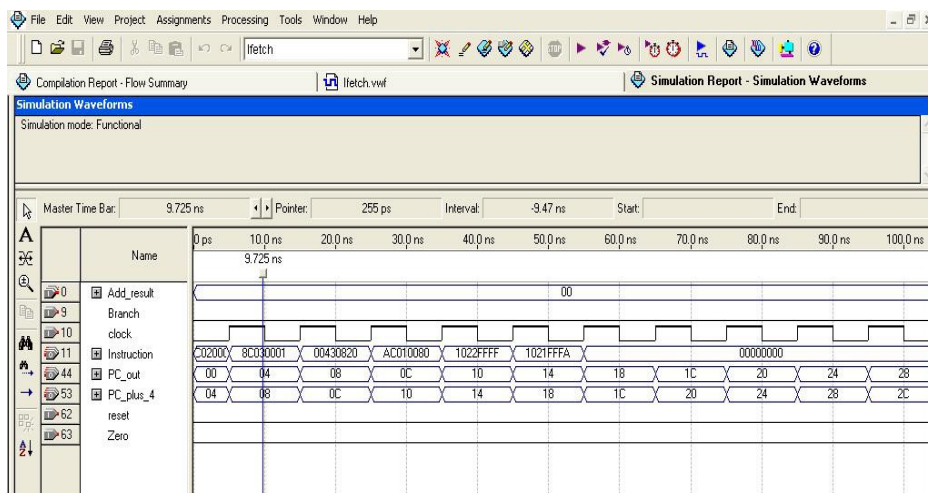


Fig 2.5 RTL view Instruction fetch unit

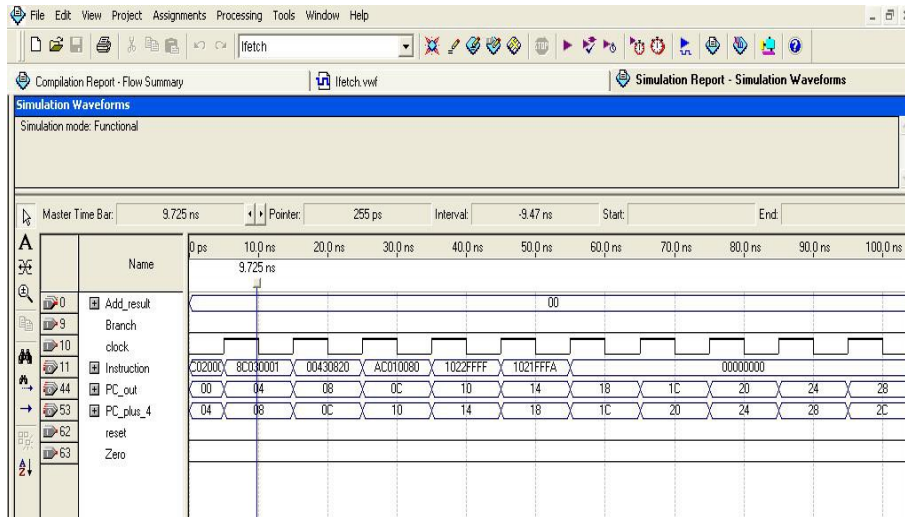


Fig 2.5 RTL view Instruction fetch unit

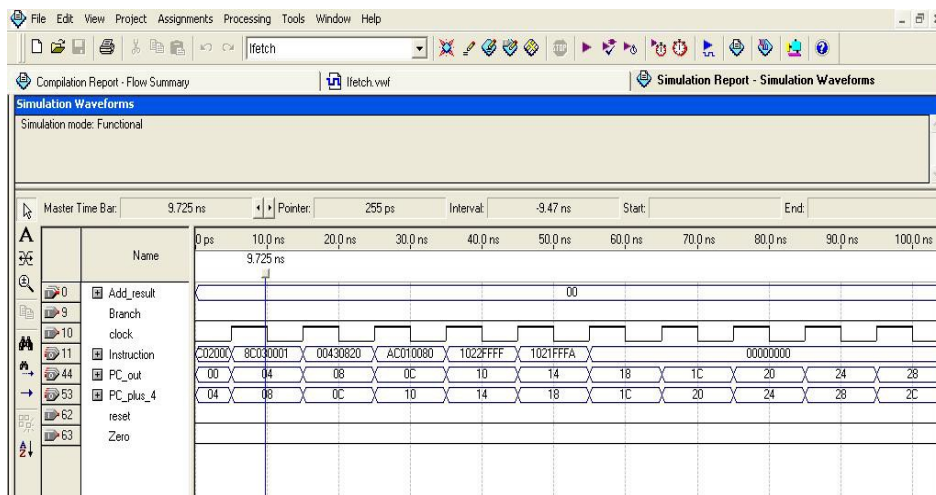
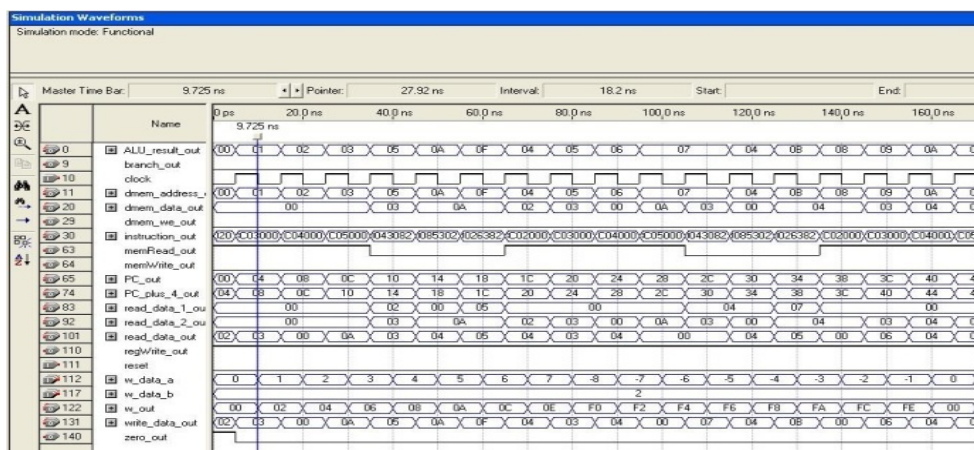


Fig 2.6 Simulation of Instruction Fetch unit

IV. SIMULATION RESULTS OF RISC PROCESSOR WITH CONVOLUTION



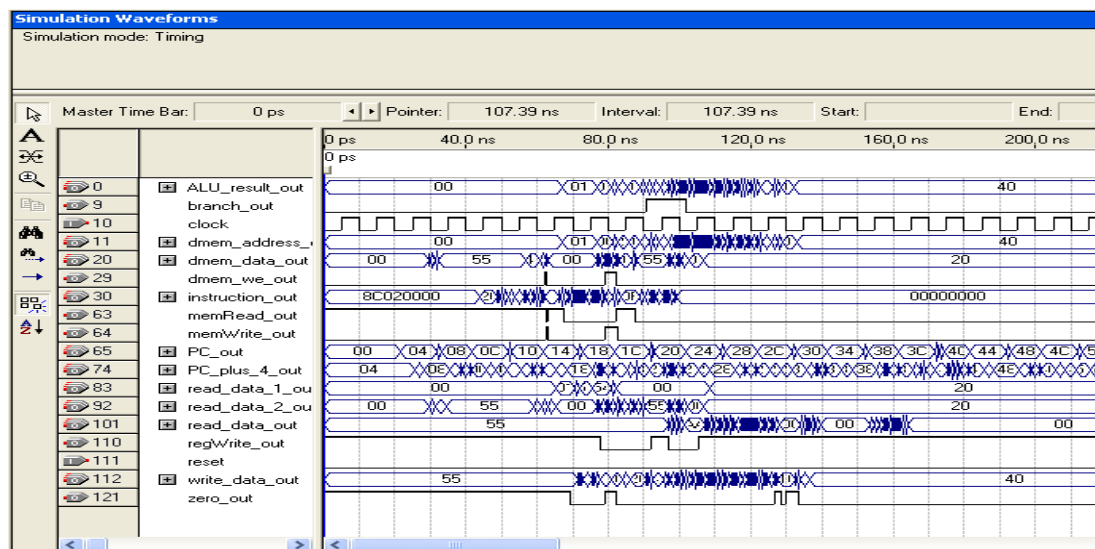


Fig 2.7 Simulation results of RISC PROCESSOR with Convolution

V. COMPARISON TABLE

Parameters	Ref. [1]	Ref. [2]	Ref. [3]	Ref. [4]	Ref. [5]	Our work
Implementation	FPGA	FPGA	FPGA	FPGA	VLSI	FPGA
Frequency	200 MHz	50 MHz	50 MHz	69 MHz	16 MHz	250 MHz
Area	-	-	78 CLBs And 6 DSP elements	2234 CLBs, 1164FlipFlops And 3829 LUTs	65012nm ²	3200LUTs, And 320Total Logic Elemen ts

VI. CONCLUSION

We have actualized 32 bit RISC processor to perform round convolution at various modules of RISC processor like execute unit alongside ALU, Instruction bring alongside guideline memory, decipher unit, resistor unit, information memory has been actualized.

In this paper we are attempting to demonstrate the plan that can be executed for Area Efficient plan in the RISC processor. We have mimicked the guidelines of 32 bit RISC processor. We have additionally mimicked the aftereffect of roundabout convolution on 32 bit RISC processor

The execution time to perform 4 bit round convolution is observed to be 270 ns. The execution time to execute the guideline is observed to be 5 ns.

In our work, 3200 LUTs and 320 rationale components are utilized to execute 32 bit RISC processor which is observed to be zone productive when contrasted with different plans given in the writing

VII. REFERENCES

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