Current Harmonics Reduction Technique in a BLDC motor Drive application

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Abstract: This paper describes the influence of different harmonics currents in the motor drive application. A variety of active and passive approaches can be adopted to reduce harmonics in systems that rely on precision motion control. For applications ranging from medical diagnostic to office automation equipment, the need to suppress conducted and radiated noise is critical, especially considering increasingly stringent electromagnetic compatibility (EMC) requirements. The challenges are to maintain system integrity and motor performance without adding significant cost or weight to a sub-assembly. This paper adopts active approach to reduce the effects of harmonics by introducing active line filter with PFC circuit at the input of power converter.

Keywords: Brushless DC motor, Buck-boost converter, Efficiency, Harmonics, Loss, Inverter,Power Factor Correction (PFC),Total Harmonic Distortion (THD).

I. Introduction

Brushless DC motors are widely used in consumer and industrial applications because of no brush and no commutator, wide speed range, and relatively high efficiency. When the motor is associated to a load system and input supplied from an inverter, there are several order of harmonics produced as per the non-linearity of motor parameters and dynamics of load.The harmonics consequences in various types of losses in the motor and inverter. These losses change according to the operating speed and the load conditions [1]. For example, when the motor speed becomes high, the iron loss increases, which reduces the motor performance. Hence, the analysis of harmonics and taking corrective actions are important. When primary source is ac mains, it is crucial to design and implement an effective line filter.

BLDC motors are frequently used along with low voltage electronics and control systems. Generally power source is common for both electronics and BLDC motor drives. So if harmonics produced during motor drive in action, are not neutralized or minimized, it will seriously affect the performance of electronics and controls. Mal-functioning of any control system in the industrial system will further degrade the quality of products being manufactured.

II. Harmonics analysis of electric drive

The standards such as CISPR 22 and IEC 61000 specify the limits on the current injection into the ground by power converter for commercial and domestic applications. NEMA MG-1, part 31 recommends the maximum allowable dv/dt that can be applied at the motor terminal for safe operation.

The IEEE 519 standard defines recommended current harmonics limits Iv at the point of common coupling for convertersystems containing non-linear loads (e.g. static power converters, arc discharge devices and saturatedmagnetic devices). The boundaries, which are defined for multiples of the fundamental frequency, are shown in Tab. 1.To meetthese regulations different solutions are adopted to mitigate the ill effects[9].

Application of the harmonic limits as defined in IEEE Std 519 to drive applications is a useful exercise but often a challenging one. Analysis canbe developed considering several harmonic attenuation methods whilecomparing hardware requirements, performance and cost.

It is significant to understand how the various system components interact with each other and with the power system [9]. It is essential that a harmonized solution be provided which meets THD levels, system performance demands and power system necessities. Fixing a harmonic distortion problem in the field after deployment can be problematic, time consuming and expensive.

Table 1:IEEE 519 standard

Low-Voltage System Classification and Distortion Limits			
	Special Applications	General System	Dedicated System
Notch Depth	10%	20%	50%
THD (voltage)	3%	5%	10%
Notch Area (AN)	16 400	22 800	36 500

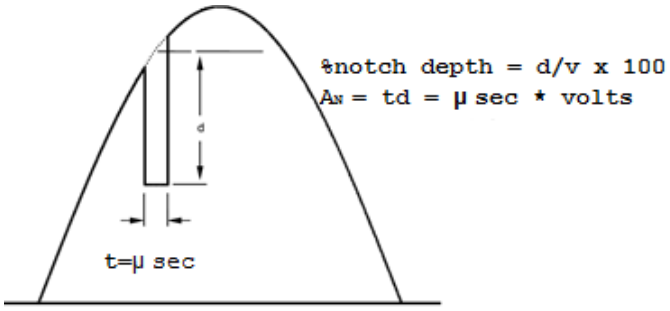

Figure 1: Definition of notch depth and notch area

Table 2: IEEE 519 standard for current distortion

Maximum harmonic current distortionIv in %					
	Individual harmonics orders				
Isc /I_L (A)	<11	11≤h≥17	17≤h≥23	23≤h≥35	35≤h
20	4	2	1.5	0.6	0.3
20-50	7	3.5	2.5	1	0.5
50-100	10	4.5	4	1.5	0.7
100-1000	12	5.5	5	2	1

III. Design objective of passive input filter

High rotational speeds for brushless motors is often limited only by the mechanical integrity of the rotor, speed related internal losses, and bearings. Speeds over 10,000 rpm are possible with appropriate design. Brushless DC motor's current can be obtained using below relation:

$$\omega = \frac{\left(\frac{T_l}{K_t} + I_o\right) \times R_t}{K_e} \times 1000$$

Where ω=motor speed, rpm, V= supply voltage, V: T_l = load torque, oz-in.; K_t= motor torque constant,oz-in./A; I_o=motor no load current, A; Rt=motor terminalresistance, Ohms; K_e= motor voltage constant, V/1000 rpm. When speed is known, one can solve this equetion for any of the unknown quantities, often voltage or current.

If motor's speed changed very frequently, it will generate too much harmonics due to change in switching frequency of inverter. An input LCL filter has to be designed to take care of such noises.Design steps are:

- The capacitor is sized to meet both of the hold-up time and the low frequency voltage ripple requirements. The capacitor value is selected to have the larger value among the two equations in below:

$C_o \geq \frac{2.P_o.t_{hold}}{V_o^2 - V_{o.min}^2}$ and

$$C_o \geq \frac{P_o}{2.\pi.f_{line}.\Delta V_o \ .V_o}$$

- check if Ton,min from the dV/dt value which is compatible with the application constraints; if not, higher dV/dt has to be accepted.
- Choose L1 such that π * L1*C ≤ Ton,min
- Choose R2 = Zc or slightly higher (R2 = n*Zc with 1<n <2)
- Set O/C protection such that O/Cth > Iphase,peak + Irecovery + Vdc/((n+1)*Zc).

- Find L2 with $f_{sw} = \frac{1}{2\pi}\sqrt{\frac{L_1+L_2}{L_1 L_2\, C}}$
- Normally, the resonant frequency is bigger than the 10 times the power frequency and smaller than 1/2 times the switching frequency.

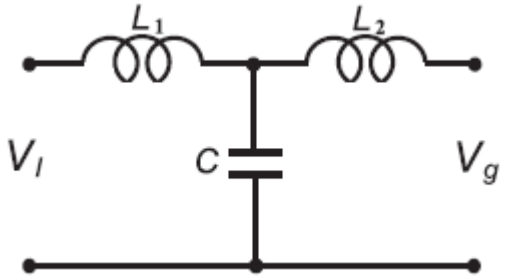

Figure 2: Schematic of LCL filter

IV. Design objective of PFC circuit

In order to meet the CISPR and IEC standards criteria for the power converter, PFC circuit has to be implementedand kept the THD within specified limits. Design steps for a buck-boost PFC are:

- Inductance Value Selection
- Output Capacitance Value Selection
- Current Error Amplifier Compensation
- Voltage Error Amplifier Compensation
- Feed-forward Voltage Divider
- PFC Controller (combined with main controller of motor inverter)
- Average Current Sensing Circuit
- Automatic Gain Control Circuit
- Protection Circuits (snubbers, fuse, TVSS diodes, GDT etc.)

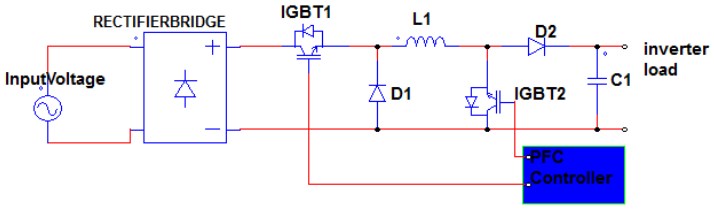

Figure 3: Buck-boost PFC circuit

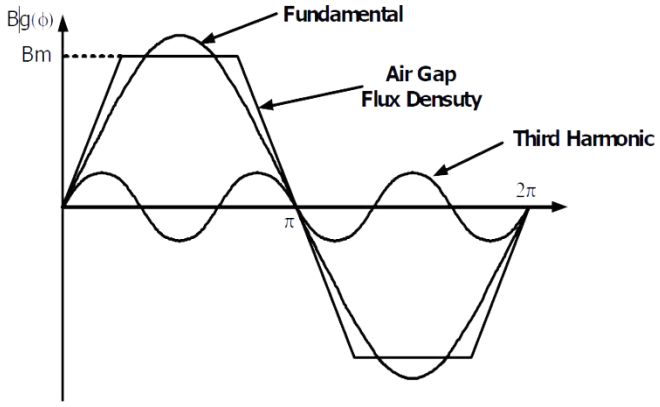

Figure 4: Representation of Harmonics

Total Harmonic Distortion of the voltage waveform is the ratio of the root-sum-square value of the harmonic content of the voltage to the root-mean-square value of the fundamental voltage.

$$V_{THD} = \frac{\sqrt{[V_2^2 + V_3^2 + V_4^2 + \cdots]}}{V_1} \times 100\%$$

Similarly, for current:

$$I_{THD} = \frac{\sqrt{[I_2^2 + I_3^2 + I_4^2 + \cdots]}}{I_1} \times 100\%$$

V. Experimental results

This study considers the BLDC motor applicationin the industrial hoists. When power is fed to the inverter through a passive filter and PFC circuit, harmonics currents are mitigated as compared to the case without filter circuit. Experiment has been conducted at rated load and speed as well as at no load conditions. During inching operations also harmonics contents in the input current have been controlled.Experimental setup consisting of electric hoist integrated with BLDC motor, power drive circuit, current and voltage probes, Yokogawa power quality analyzer, and variable frequency variable voltage power source.

Average current THD minimized to 0.63% with the use of filter and PFC circuit whereas same was at the 19% level when there was no filter and PFC circuit.

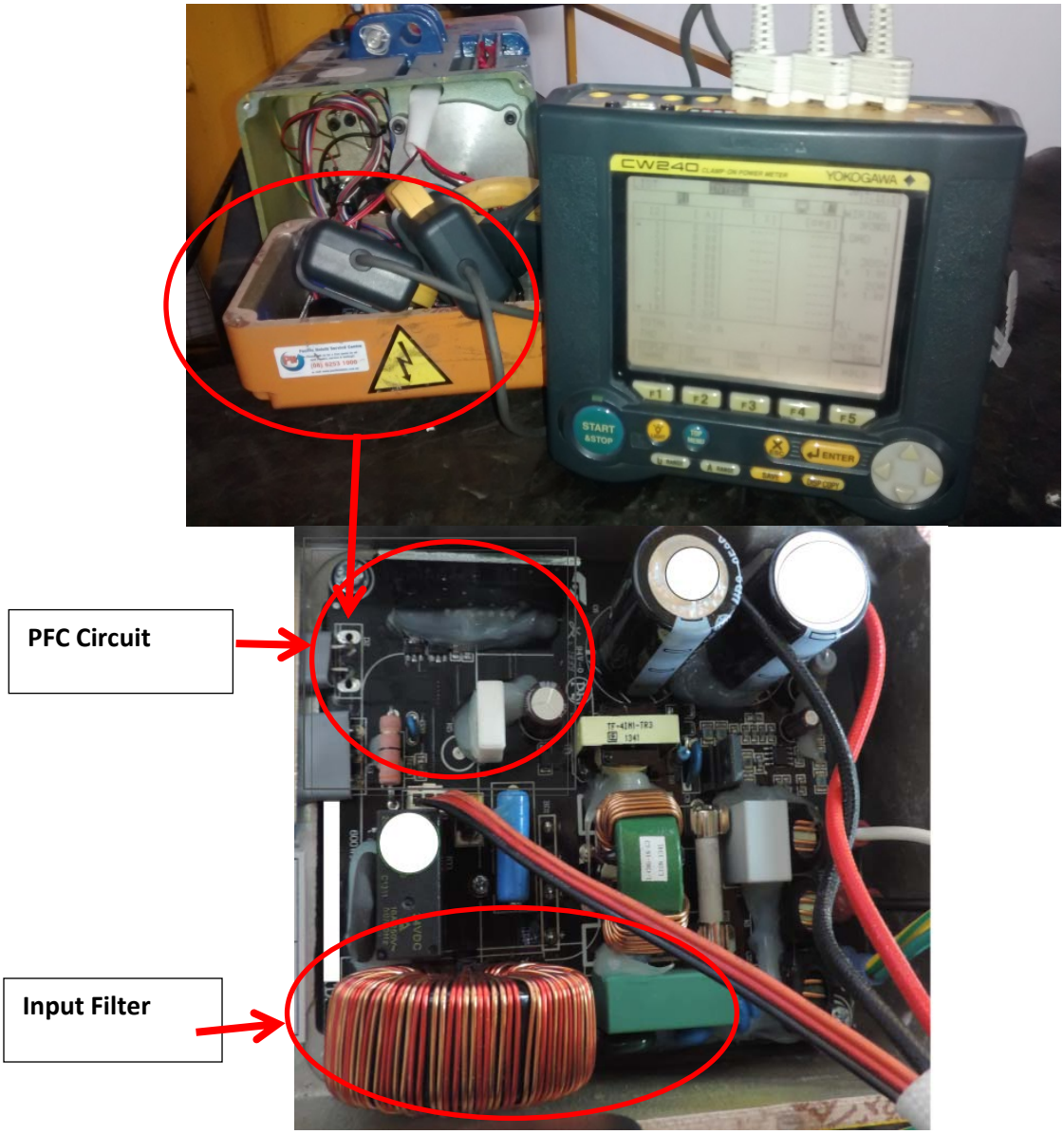

Figure 5:Test setup

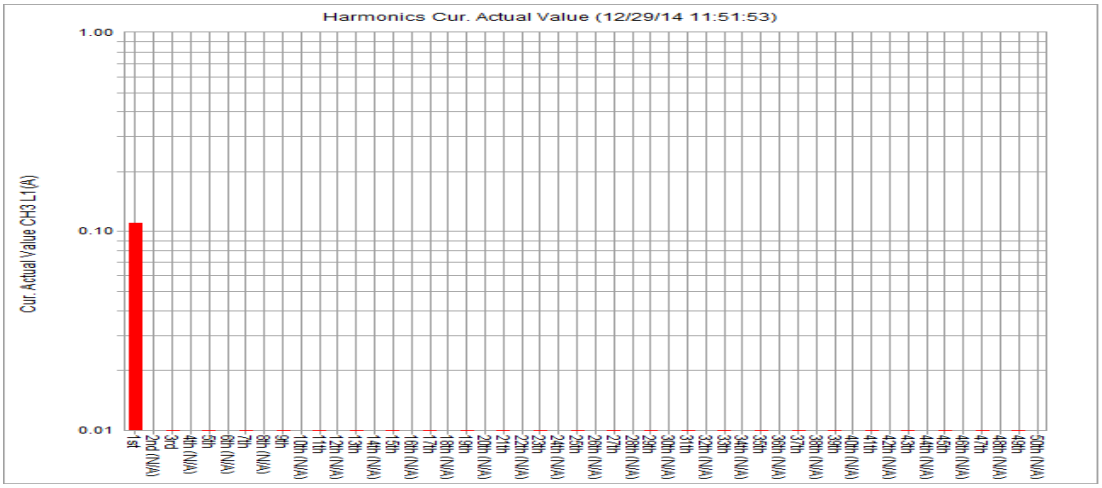

Figure 6: Input current when PFC and filter circuit implemented without load

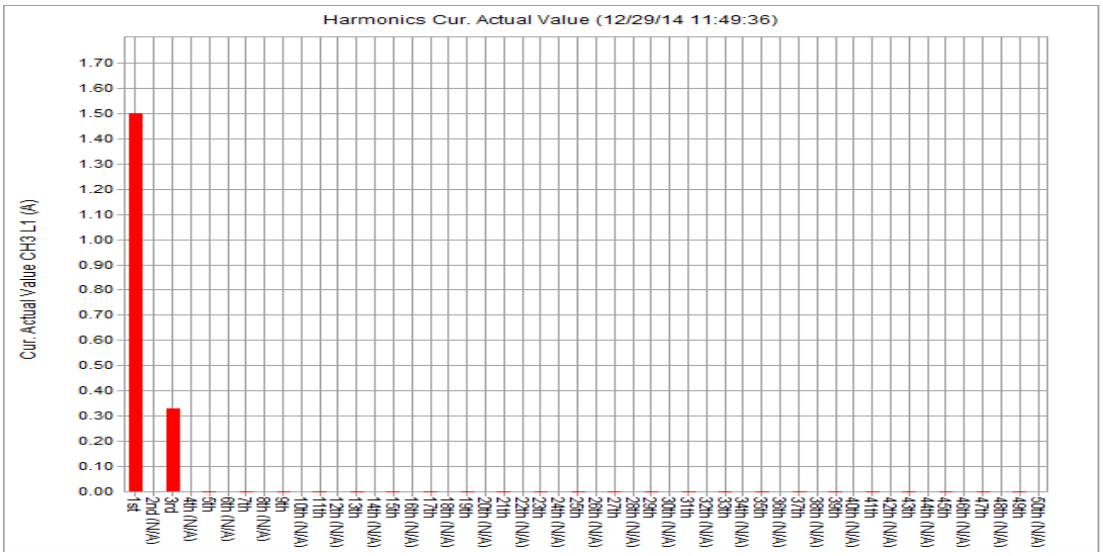

Figure 7: Input current when PFC and filter circuit implemented with load

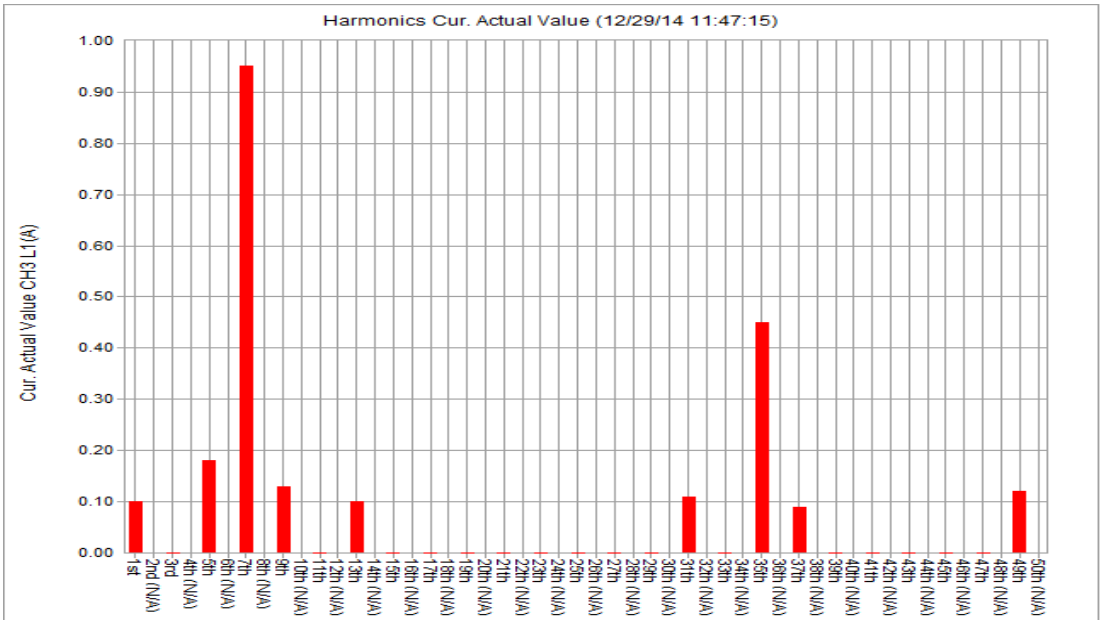

Figure 8: Harmonics current without filter and PFC

VI. Conclusion

In this paper, the harmonics current of a BLDC motor is analyzed. From the experimentalresults, it is evident that the harmonics components at the switching frequency and multiples of switching frequency are reduce by the filter.It is found that more than half of the harmonics components are reduced with filter. The current waveforms are smoothened by the filter during the operation and the commutation frequency harmonics minimized.

VII. References

[1] KayhanGulez, Ali Ahmed Adam, and HalitPastaci, "Torque Ripple and EMI Noise Minimization in PMSM Using Active Filter Topology and Field-Oriented Control," IEEE Trans. Industrial Electronics, Vol. 55, No. 1, pp. 251-256, Jan 2008.
[2] S. Morimoto, Y. Takeda, T. Hirasa, "Loss minimization control of permanent magnet Synchronous motor drives," IEEE Trans. Industry Electronics, vol. IE-41, no. 5, pp. 511- 517, 1994.
[3] S. Harrori, M. Ishida, and T. Hori, "Vibration suspension control method for PMSM using repetitive control with auto tuning function and Fourier transform." In Proc 27th Annu. Conf. IEEE IECON,2001, PP 1673-1679.
[4] J.S Kim, s. Doki and M.Ishida, "Improvement of IPMSM sensorless control performance using Fourier Transform and repetitive control," in proc.27th Annu. Conf. IEEE IECON, 2002. PP. 597-602.
[5] Yong Liu, Z. Q. Zhu, "Commutation-Torque-Ripple Minimization in Direct-Torque-Controlled PM Brushless DC Drives" IEEE trans. Industry Applications, Vol. 43, No. 4, August 2007. PP 1012- 1021.
[6] Roque Alfredo Osornio-Rios, Rene de Jesus Romero-Troncoso, Gilberto Herrera, and Rodrigo Castaneda-Miranda, "FPGA implementation of higher degree polynomial acceleration profiles for
[7] peak jerk reduction in servomotors.", Robotics and Computer- Integrated Manufacturing (2008) Science Direct, Jan 2008.
[8] Zhi Yang Pan, and Fang Lin Luo, "Novel resonant pole inverter for Brushless DC motor drive system", IEEE Trans on Power Electronics, Vol. 20, No. 1, Jan 2005. PP 173-181.
[9] Takeo Ishikawa, Takuma Tsuji, Seiji Hashimoto, and Nobuyuki Kurita, "A Simple Equivalent Circuit for Efficiency Calculation of Brushless DC Motors", Journal of International Conference on Electrical Machines and Systems Vol. 3, No. 1, pp. 54~60, 2014.
[10] IEEE Recommended Practice andRequirements for Harmonic Control inElectric Power Systems, Transmission and Distribution Committee of the IEEE Power and Energy Society, 2014.