

QCA Based Efficient Toffoli Gate Design and Implementation for Nanotechnology Applications

Bisma Bilal¹, Suhaib Ahmed², Vipin Kakkar³

Department of Electronics and Communication Engineering,
Shri Mata Vaishno Devi University, Katra, India

¹bismabilal21@gmail.com

²sabatt@outlook.com

³vipan.kakkar@smvdu.ac.in

Abstract—The construct of computing is the field of ever improving and advancing systems and architectures. One of the emerging archetype that has made its ground as a research area is the concept of reversible logic in computing. Reversible logic suggests the systems with zero heat dissipation since the computational models in this logic incorporate the concept of reversibility at a ground level thereby satisfying the work and heat relations according to the laws of physics. In this paper we have first of all presented a detailed insight about the reversible logic and the perspectives related to it. Further the design of reversible logic circuits using the new emerging nanotechnology called Quantum-dot Cellular Automata (QCA) has been envisaged. These two paradigms together hold the potential of realizing ultra-low power systems and architectures. In this paper, the most common and popular reversible gate called as the Toffoli Gate has been considered and designed using this new QCA technology. This paper presents the approach of using cell to cell interaction in designing the reversible circuits which result in efficient implementations. The necessary comparisons with the literature are drawn and it is explicitly shown that the proposed designs are highly optimized as compared to existing counterparts.

Keyword - Cellular Automata, Clocking, Invertibility, Nanotechnology, QCA, Reversibility

I. INTRODUCTION

The improvements in the computer architectures has been the primary goal of the researchers and designers ever since the paradigms of designing have made way. One of the primary design constraint that has limited the applicability of design conceptions is the work and heat relations of the computational systems. For the various systems a relationship between heat, power dissipated and the amount of work done suggests the information loss as the processing of bits takes place. The limitation of heat dissipation of the computing systems is the main driving force which draws the attention to reversibility. Reversibility not only calls for low power dissipation systems but also high speed and greater density of the circuits. In reversible logic we talk about conservation of information which can be considered as analogous to conservation of energy and momentum in physics. The concept of reversibility exists in all the physical systems even though it is not explicit due to the limitations of the computational models that exist. The inherent reversibility is exploited in the reversible architectures leading to a new framework that results in zero heat dissipation systems. In 1961 Landauer, suggested that the heat that is dissipated in the computing systems is not because of the processing of bits but due to the erasing of bits that occurs during the process. This suggests that the systems which are irreversible do not conserve information and thus are not information lossless. For every bit of information that is erased an energy equivalent to $KT\ln 2$ joules is dissipated [1]. Here T is the temperature at which the computation is performed and K is the Boltzmann's constant. Further to strengthen this theoretical concept Bennet derived some important analysis from the Turing machine example [2]. He suggested that this $KT\ln 2$ joules of dissipated energy in case of the irreversible systems can be avoided by using the systems which are reversible.

Reversibility is a notion which calls for the realization of bijective functions [10]. The concept of reversibility suggests that a backward and forward track, both are possible at any time for a system. The theory of reversibility finds its roots in the reversible nature of the physical laws which exhibit one to one functions. This suggests the possible reason for the irreversible nature of the conventional system which involve many to one or vice versa functions. While designing of reversible logic circuits this mapping is to be taken care of as fan out is not allowed in the case of reversible circuits. Inevitably even the conventional irreversible processes have the inherent reversibility but is hidden at the very low level, say in the physics of the basic gates. This however lies beyond the models of computation and hence appear irreversible due to the work-heat relations. As suggested by Toffoli, if the theoretical concept of achieving invertibility in systems is realized, a closer correspondence between the computing systems and the basic physical laws of nature can be achieved. He points out that the principles of micro level are not having an adequate representation in the theoretical constructs. So if somehow

the counterparts of the basic physical principles are achieved and incorporated in the theory a better match is possible between theoretical and application correspondent.

For any system to be reversible its building blocks need to be individually reversible. This means that at the basic level we can talk about a reversible gate. For reversible structures the number of inputs and outputs has to be always equal since without that the one to one mapping which is the second important consideration, cannot be achieved. Whenever achieving reversibility is a target some source and sink lines need to be added to construct an invertible function. These include some constant inputs, the inputs which have a sole function of achieving the invertible function and the garbage outputs, the outputs which are not used further in computation. The efficient systems aim for a reduction in the number of constant inputs and garbage outputs. The design optimization parameters in the reversible circuits include these constant inputs, garbage outputs and the quantum cost assessment. Quantum cost is defined as the number of primitives needed for the design of the particular circuit. In reversible logic optimizing the quantum cost is identified as the most important and most challenging task. This emerging concept of reversibility with its feature of low power dissipation forms the centre of attraction for the VLSI designers since CMOS VLSI is suffering the issue of power dissipation at the nano scale levels [3-5]. The quantum mechanical effects which lead to the failure of the CMOS devices in the deep sub-micron ranges can be countered by reversible logic since the quantum mechanical systems are inherently reversible in nature. This calls for extensive research in the areas like reversible design. The issue however remains of the designing of these circuits. A new design paradigm if successfully used in designing reversible circuits can lead to the ultra-low power systems which is the need of the hour to continue with the technology advancements. We discuss this new nanotechnology based cellular automata in the next section.

II. QCA ARCHITECTURE

Quantum-dot Cellular Automata (QCA) is identified as the new upcoming nanotechnology for the design of the digital circuits[6].The need for such a technology arises from the fact that as the scaling of conventional CMOS is taken down to the nano regime, the behavior of the device can no longer be classically governed. The effect of quantum mechanics cannot be neglected in this range and needs to be taken into consideration. The conventional technology models however fail to consider the quantum effects and thus are unable to explain the phenomenon occurring at the nano scale. This new technology called QCA uses the quantum effects to its advantage and thus is more suitable for the nanotechnology based applications. This technology calls for a departure from the conventional current and voltage paradigms and is governed by the laws of physics such as coulombic repulsions and the quantum mechanical tunneling. The basic concept of QCA architectures lies in two facts. Firstly, due to coulombic repulsions the electrons tend to take up the positions where they face minimum repulsion from each other and secondly the tunneling controls the alignment of these electrons. The structures in QCA are the cellular automata type designs where the basic component repetitions form all the circuitry. The fundamental element in QCA is the QCA cell which is a square structure as shown in the figure 1. This cell consists of four areas for the localization of the trapped electrons and there are two tunneling junctions due to which the electrons can change the alignment. The potential wells (areas of localization) can be created by quantum dots or metal islands. As is evident from the figure there are four places at which the electrons can reside. Due to coulombic repulsion between the trapped electrons they tend to take up the positions with minimum repulsion. For the shown structure of the cell this calls for two possible types of alignments called as the two polarizations of the cell. This is as shown in figure 1.

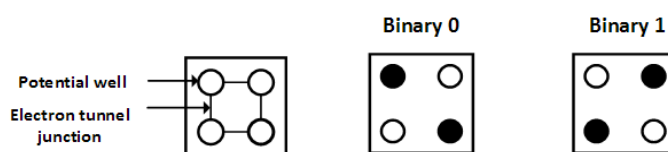


Fig. 1: Basic QCA cell

Since in QCA we deal with the digital designs the two polarizations represent the two possible digital states i.e. the binary zero and the binary one. This basic cell forms the building block for all the design architectures using the QCA nanotechnology [7,8]. When we talk about the conventional CMOS or any other technology the circuits and interconnections are two different class of elements but in QCA the basic cell forms both the circuits as well as the interconnections. The alignment of the cells adjacent to each other results in the formation of a binary wire which is used for the transmission of the information from one point to another. The inverter and the majority voter along with the binary wire form the basic blocks for designing any kind of complex architectures in the QCA. The three blocks are shown in the figure 2.

The working mechanism of the inverter is based on the opposite alignment of the cell at the right hand side due to which the alignment of electrons changes the polarization to achieve the stable state. Thus the output from such a structure is opposite as compared to the input. In the case of majority gate the central cell governs the output which in turn depends on the three inputs of the majority gate. The polarization of the central cell is

that of the majority of the inputs since that results in a stable state. Besides the basic blocks another very important consideration in the QCA design methodologies is the clocking mechanism involved in these circuits. The clocking in QCA governs the tunneling of the electrons between the potential wells which may be the quantum dots or islands as discussed earlier. In QCA one clock cycle consists of four clock phases. Each phase is characterized by either lowering or raising of the barrier.

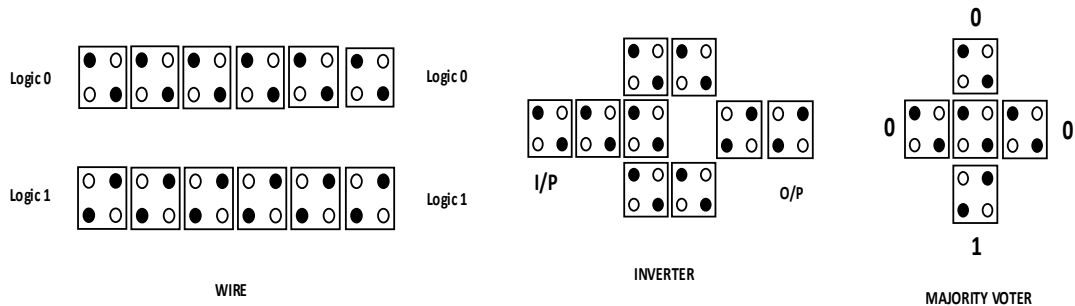


Fig. 2: Basic Building Blocks in QCA

The first phase is the switch phase in which the tunneling barriers are raised such that the cell attains a particular polarization. The next is the hold phase in which the barriers are maintained at a high level and the cell is in a position to effect the polarization of the adjacent cells. Further the other two phases are the release and the relax phase in which the barriers are lowered such that the cell again attains the null polarization. The clocking to the QCA circuits is provided by the underlining CMOS or carbon nanotube wiring to provide the necessary electric field for the alignment of electrons in particular polarization in a particular cell. Besides the clocking in QCA, another important criteria is the crossing over of the wires which result in the designing of efficient and optimized designs. A number of crossover schemes have been applied for the QCA designs. The most common are the coplanar and multilayer crossovers. Logical clock zone based crossovers have also been envisaged in the literature [14-17].

III. PROPOSED TOFFOLI GATE QCA DESIGN

When dealing with reversible logic which we have discussed in the first section of this paper, the basic concept is to achieve bijective functions. This is achieved in the case of reversible gates. A number of reversible gates have been proposed in literature and a number of applications of the designs are highlighted [9-12, 18, 19]. However design of reversible gates using the new QCA technology is still an emerging topic and researchers are working towards obtaining the optimized designs of the gates and circuits in the QCA technology. The need to do so is to achieve efficiency in all the aspects, be it the ultra-low power dissipation or the ultra-low size of the devices.

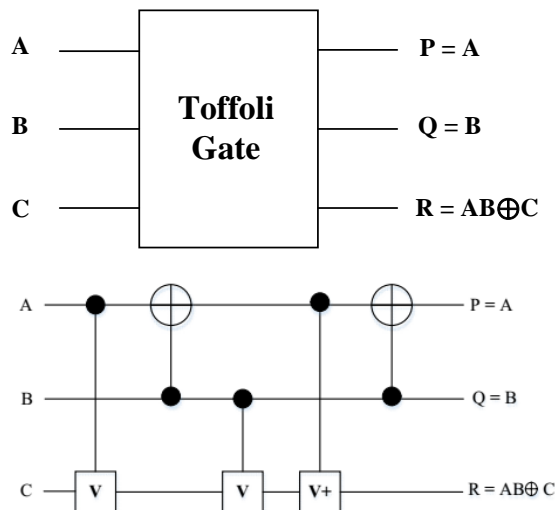


Fig. 3: Toffoli Gate and its Quantum Implementation

If the reversible gates find optimal realization in QCA the achievement of the above two targets can be changed from just a theoretical concept to the applicable paradigm. One of the most oldest and popular reversible gate is the Toffoli gate. This gate satisfies the conditions of reversibility which are the equal number of input and output, the one to one mapping between the input and output, no fan out and no feedback. The input

vector for the Toffoli gate is $I(A, B, C)$ and the output vector is defined as $O(P, Q, R)$. This is shown in figure 3. For designing the Toffoli gate in the QCA nanotechnology the tool called QCA Designer 2.0.3 [25] is used. The Toffoli gate is proved to be reversible from the truth table shown in table I which suggests that both inputs and outputs can be recovered uniquely.

A number of designs of Toffoli gate are implemented in QCA [20-24] but the designs involve a large cell count and area due to which they cannot be called as the optimized designs. In our proposed design we have shown a departure from the conventional majority logic approach which has been used in all designs in the literature as of now. We have used the explicit interaction of cells [13] to reduce the cell count and achieve efficient circuits.

TABLE I. Truth Table of Toffoli Gate

INPUT			OUTPUT		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

We have compared our designs with those present in the literature and have explicitly verified that our designs are highly optimized in terms of all the parameters such as the cell count, area, latency and complexity. Figure 4 shows the QCA implementation of the Toffoli gate along with the simulated results in QCA designer 2.0.3.

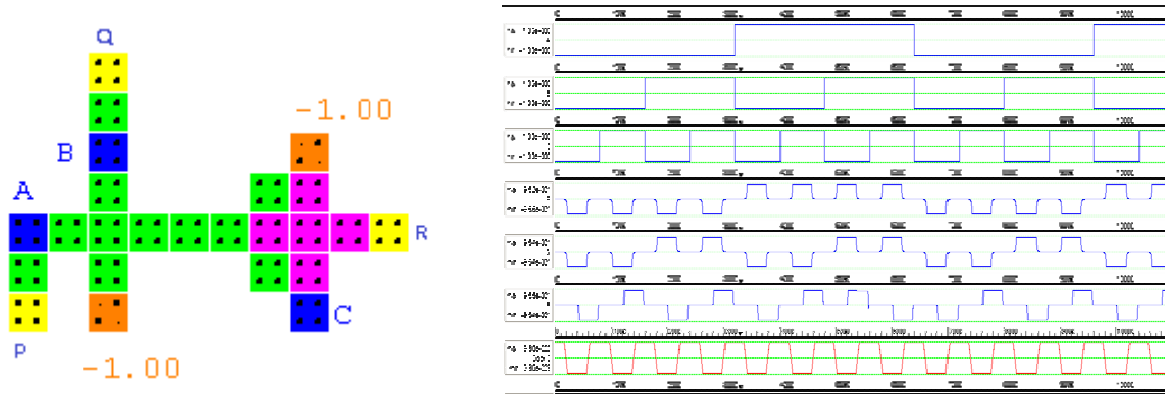


Fig. 4: Optimal QCA implementation of Toffoli Gate

One of the most important advantage of the Toffoli gate is that the gate is universal in nature and can be used for the implementation of all the seven basic functions. This is achieved by manipulating the inputs to the gate. This also results in the production of garbage outputs, the lines which have the functionality of just making the gate reversible. The manipulation of the inputs to achieve various functions is shown in table II.

TABLE III. Basic Gate Functions Obtained Using Toffoli Gate

S. No.	Circuit	Toffoli Gate Function
1	NOT Gate	Toffoli (A,1,1)
2	AND Gate	Toffoli (A,B,0)
3	NAND Gate	Toffoli (A,B,1)
4	OR Gate	Toffoli (A',B',1)
5	NOR Gate	Toffoli (A',B',0)
6	Ex-OR Gate	Toffoli (A,1,C)
7	Ex-NOR Gate	Toffoli (A,1,C')

The QCA implementation of the various logic gates designed with proposed Toffoli Gate are shown in Figures 5(a-g)

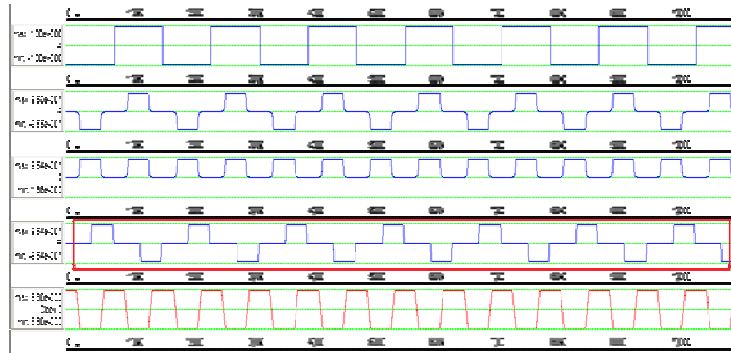
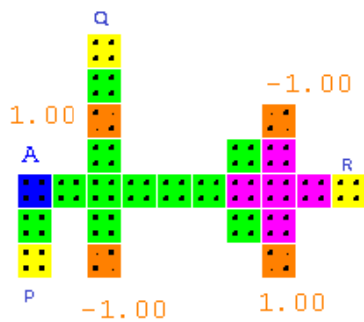


Fig. 5(a): QCA implementation and simulation waveform of NOT Gate using proposed Toffoli Gate

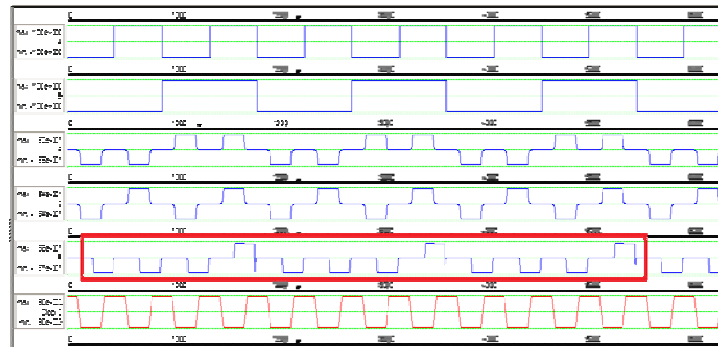
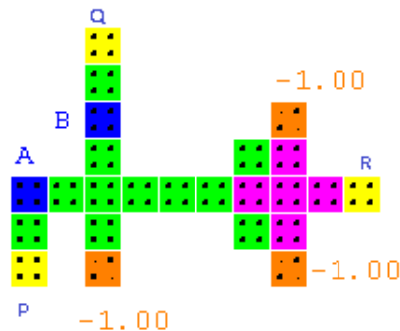


Fig. 5(b): QCA implementation and simulation waveform of AND Gate using proposed Toffoli Gate

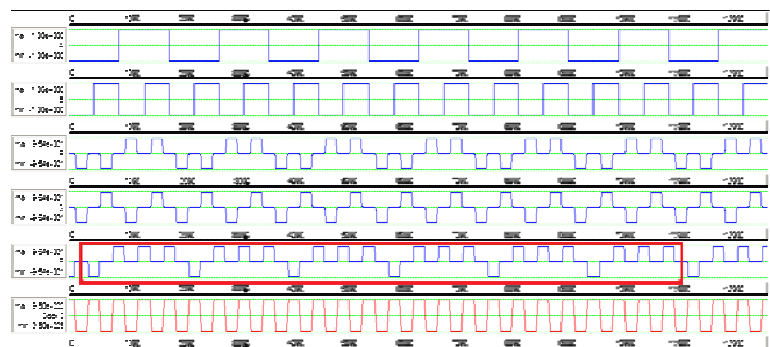
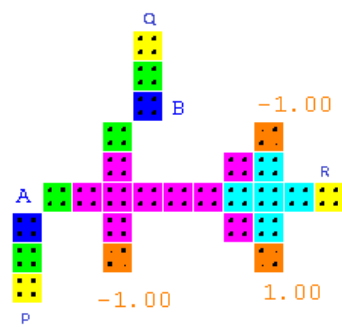


Fig. 5(c): QCA implementation and simulation waveform of OR Gate using proposed Toffoli Gate

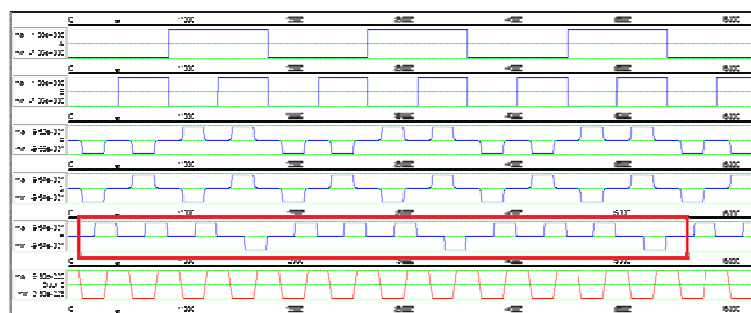
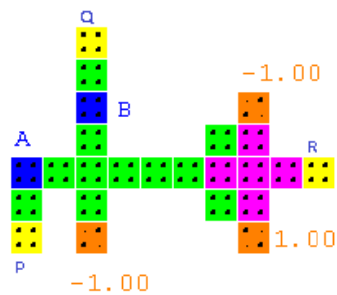


Fig. 5(d): QCA implementation and simulation waveform of NAND Gate using proposed Toffoli Gate

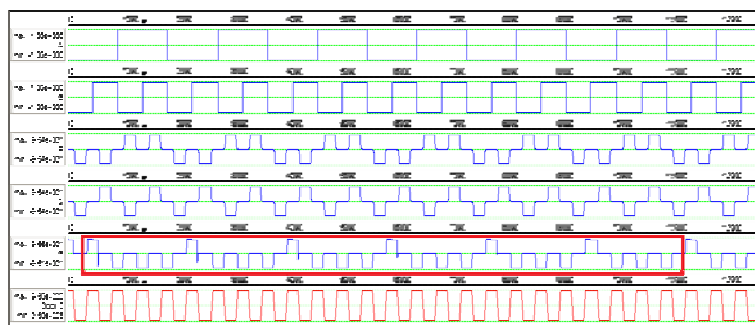
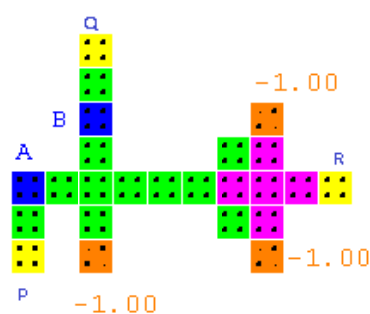


Fig. 5(e): QCA implementation and simulation waveform of NOR Gate using proposed Toffoli Gate

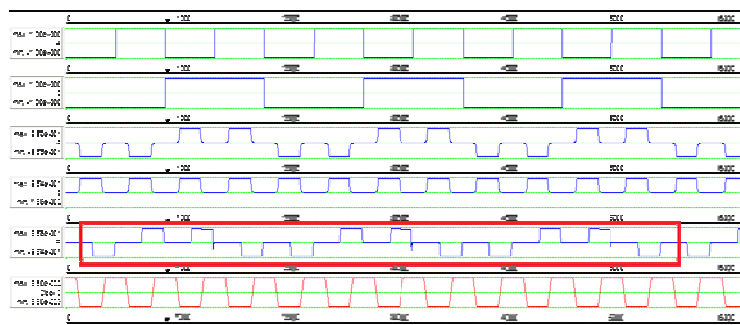
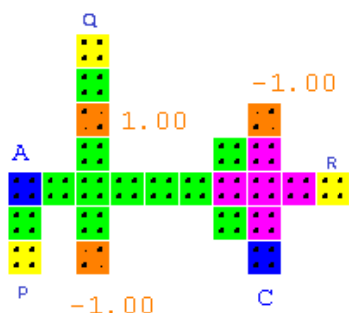


Fig. 5(f): QCA implementation and simulation waveform of Ex-OR Gate using proposed Toffoli Gate

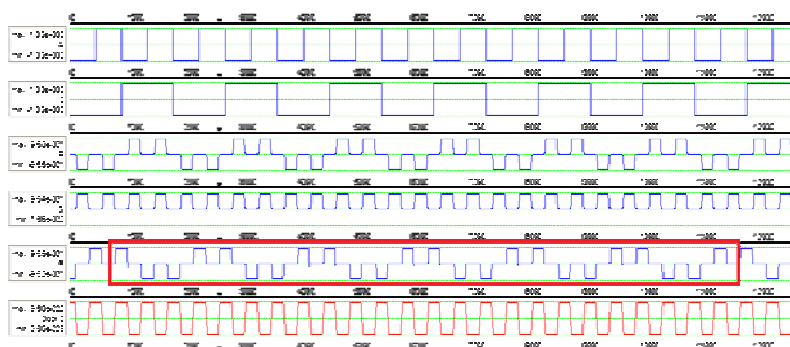
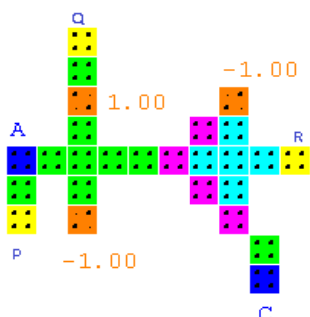


Fig. 5(g): QCA implementation and simulation waveform of Ex-NOR Gate using proposed Toffoli Gate

In the QCA Designer tool a number of engines are available for simulating the circuits. We have chosen the bistable approximation engine which does the time-independent simulation of the QCA design. This engine works on the principle of interaction of cells and suggests that the interaction strength decays between cells inversely with fifth power of distance between them. The parameters selected for simulation are

- Cell size = 18nm,
- Cell spacing = 2nm
- Number of Samples = 12800
- Radius of Effect = 65.000000nm
- Convergence Tolerance = 0.001000
- Relative Permittivity = 12.900000
- Clock High = 9.800000e-022
- Clock Low = 3.800000e-023
- Clock Shift = 0.000000e+000
- Clock Amplitude Factor = 2.000000
- Layer Separation = 11.500000

TABLE IIIII. Performance Comparison of various proposed Toffoli gates in QCA

Circuit	Cell Count	Cell Area (μm^2)	Total Area (μm^2)	Latency (in clock cycles)	Complexity
Toffoli [20]	169	0.0547	-	16	3 layers used
Toffoli [21]	101	0.0327	0.0829	5	Single layer design.
Toffoli [22]	75	0.0243	0.0952	4	Single layer
Toffoli [22]	48	0.0155	0.0498	4	Single layer
Toffoli [23]	57	0.0184	0.0700	3	Single layer
Toffoli [24]	45	0.0145	0.0427	4	Single layer
Proposed Toffoli Gate	24	0.0077	0.0226	0.5	Single layer

The graphical representation of the comparisons of proposed gate with the Toffoli Gate designs in literature are also shown in figures 6-9.

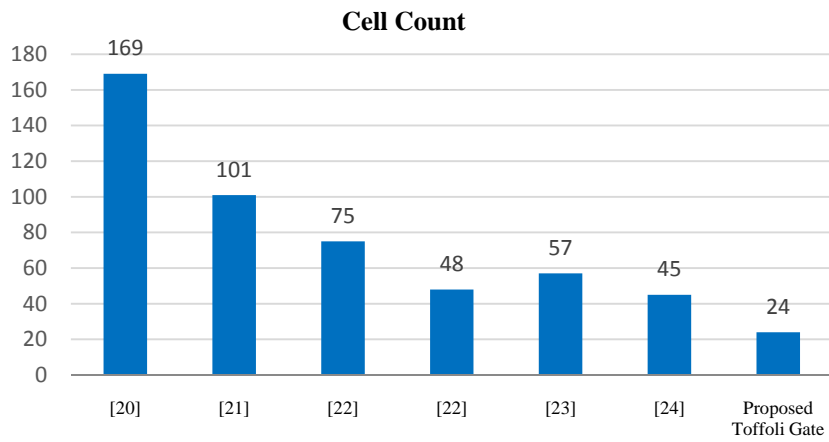


Fig. 6: Comparative Cell Count of various Toffoli Gate implementations

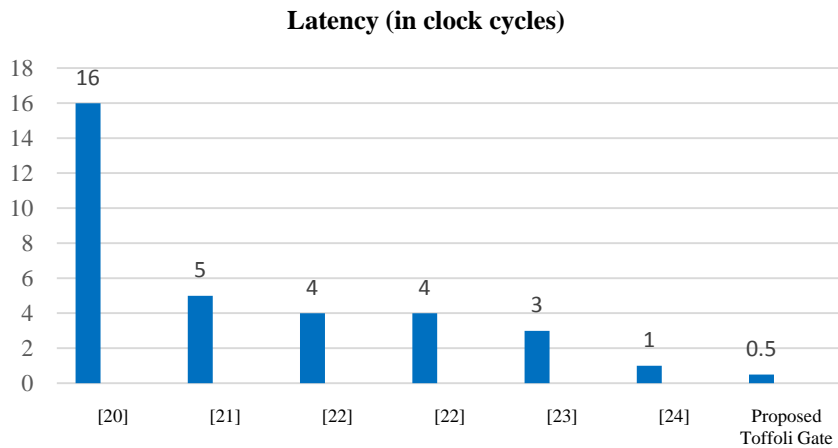


Fig. 7: Comparative Latency of various Toffoli Gate implementations.

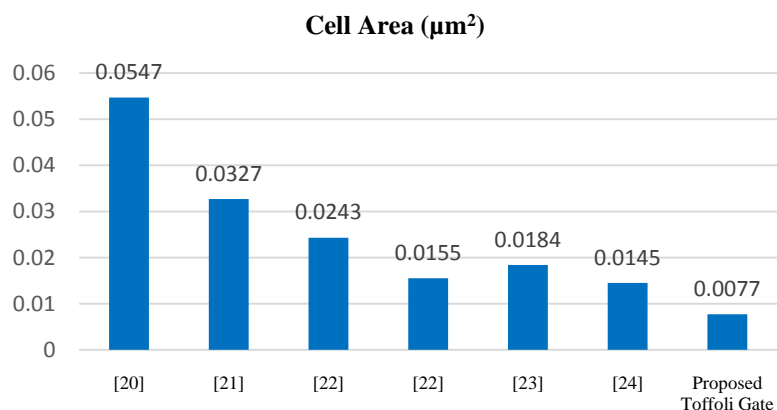


Fig. 8: Comparative Cell Area of various Toffoli Gate implementations.

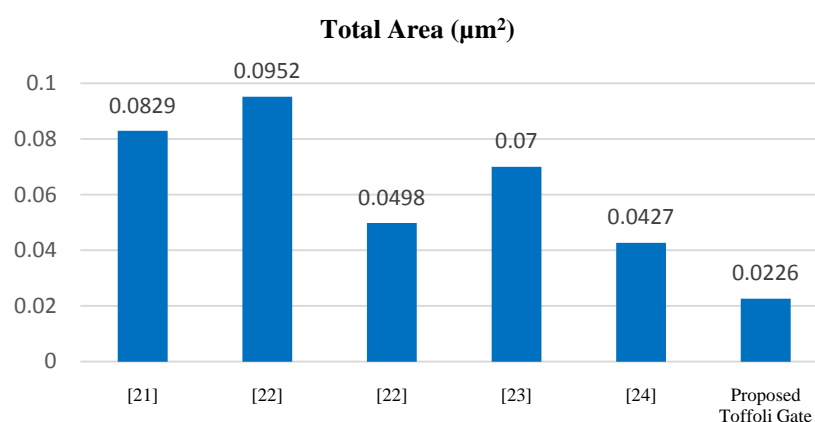


Fig. 9: Comparative Total Area of various Toffoli Gate implementations.

IV. CONCLUSION

This paper presents an overview of the concept of reversibility with focus on its utility and tendency to revolutionize the circuit designing paradigms. The combination of reversible logic and the Quantum-dot Cellular Automata Nanotechnology which has emerged as a hot area of research holds the potential to replace the conventional transistor based design architectures. A brief review of the QCA technology and the laws governing the QCA designing has been presented. Further the optimized Toffoli gate implementation in QCA has been proposed and comparisons are drawn with the existing implementations in the literature. It is shown both graphically and numerically that the proposed designs are highly efficient in terms of cost, area and delay as compared to existing counterparts.

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AUTHOR PROFILE

Bisma Bilal is currently pursuing M.Tech in Electronics and Communication Engineering at Shri Mata Vaishno Devi University, Katra, India. She received her B.Tech degree in Electronics and Communication Engineering from Islamic University of Science and Technology, Jammu And Kashmir, India. Her research interests include Nanotechnology, Quantum Cellular Automata, analog and digital VLSI design and biomedical VLSI

Suhaib Ahmed was born in Jammu, India, in 1991. He received the B.E. degree in electronics and communication engineering from University of Jammu, India, in 2012 and M.Tech. degree in electronics and communication engineering from Shri Mata Vaishno Devi University, India, in 2014. He is currently pursuing his Ph.D. degree in electronics and communication engineering from Shri Mata Vaishno Devi University, India. His research interests include data converters, quantum cellular automata, nanotechnology, application of wireless sensor networks in health and environment monitoring, biomedical signal processing and energy harvesting for biomedical implants. He is currently working on design and modeling of ultra low power mixed signal circuits for submicron devices. Mr. Ahmed is a member of IEEE, International Association of Engineers and Associate Member of Universal Association of Computer and Electronics Engineers.

Vipan Kakkar was born in Amritsar, India, in 1973. He received the B.E. degree in electronics and communication engineering from Nagpur University, India, in 1994 and M.S. degree from Bradford University, UK, in 1997. He received his Ph.D. degree in electronics and communication engineering from Delft University of Technology, Netherlands in 2002. He worked in Research & Development at Phillips, Netherlands as engineer and system architect from 2001 to 2009. Since 2009, he has been an Associate Professor with the Department of Electronics and Communication Engineering, Shri Mata Vaishno Devi University, Katra, India. His research interests include nanotechnology, ultra low power analog and mixed signal design, MEMS design, synthesis and optimization of digital circuits, biomedical system and implants design, audio and video processing. Dr. Kakkar is a Senior Member, IEEE and Life Member, IETE and has served as an Executive Member of IEEE, India and has published many research papers in peer reviewed journals and International Conferences. He has also authored a book on System on Chip Design and has served as an editorial board member of microelectronics and solid state electronics journal