Proportional Resonant controller based Inter Leaved Boost Converter fed Unified Power Quality Conditioner System

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***Abstract*- UPQC is an useful FACTS controller between sending end and receiving end for improvement of voltage quality. This work deals with identification of suitable controller for closed loop operation of ILBC based UPQC. The Analysis and comparison of responses with PI, FOPID & PR are presented in this article. The results of PI based ILBC-UPQC systems are compared with those of FOPID& PR controlled ILBC-UPQC system. The objective of this work is to improve the time domain response of ILBC-UPQC using suitable controller. The ILBC is proposed for UPQC since it gives better performance than HSUC and TIBC. The comparison is done in terms of rise time, peak time, settling time & steady state error. The MATLAB results indicate superior performance with PR based ILBC-UPQC system.**

Keywords: Rise time, Peak time, settling time, Steady State Error

I. INTRODUCTION

A.General

In present day control structures, allotment utilities arrange the related weights to satisfy the strict power quality rules. This is to improve the resolute nature of the scattering structure to address the issues of essential weights and tricky robotization systems.

The genuine necessities to keep up extraordinary quality power are: 1) essential responsive power requirements of the related burdens; 2) voltage records and swells at the reason for general coupling (PCC) due to affiliation and division of tremendous mechanical weights and open power compensating capacitors; and 3) voltage or conceivably current symphonious bowing on account of the closeness of nonlinear weights. Dynamic power channels (APFs) are the most reassuring and extensively used answers for upgrading the Power Quality (PQ) at the flow level [1]-[2]. These APFs can be appointed shunt APF, course of action APF, and blend APF. The blend of both course of action and shunt APFs, to decrease most of the voltage and current related PQ issues, is a bound together Unified Power Quality Conditioner (UPQC). Preferred execution and the utmost over abatement all major PQ issues make UPQC the most appealing system for PQ change despite its high cost, complex structure, and control [1]-[3]. The structure outline of an UPQC is showed up in Figure.1.

Current examples in the zone of UPQC are facilitated toward working the UPQC with least volt ampere (VA) stacking to lessen the general structure hardships [3]-[12]. In any case, most of the uncovered work rely on upon constraining the VA stacking in the midst of voltage rundown conditions [3],[4], [7]-[12]. The evaluating some portion of the UPQC system (tallying the shunt inverter, game plan inverter, and course of action transformer) considering particular shunt and game plan inverter VA stacking under different working conditions are inspected.

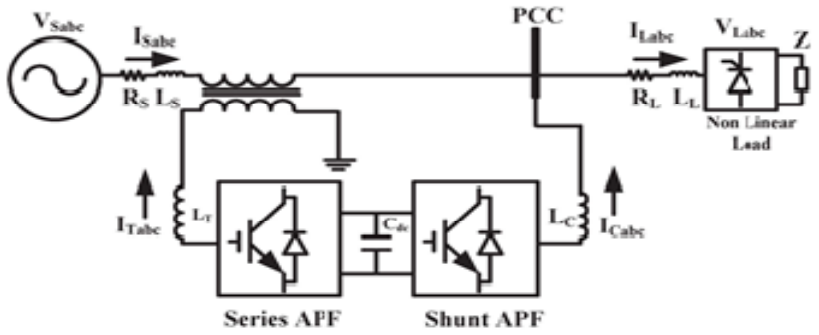

Fig.1: Schematic diagram of the Unified Power Quality Conditioner (UPQC)

In perspective of the control technique being used for voltage rundown or swell compensations, the UPQC structures can be appointed UPQC-P, UPQC-Q, and UPQC-S [2]. The UPQC-P is thought to be a consistent UPQC, where voltage fall and swell pay are performed by implanting/holding the dynamic influence (in eliminate or of stage voltage) through the course of action some portion of the UPQC while the shunt inverter supports the load responsive influence, dynamic influence required by the plan inverter, and the adversities in the structure. For a comparative estimation of voltage hang and swell compensation, the VA loadings of course of action and shunt inverters will be most outrageous in the midst of the UPQC-P, compensating for the best voltage list. Thus, UPQC-P should be sketched out in light of the best, voltage hang compensation. While in case of UPQC-Q the voltage imbued through a game plan transformer is in quadrature with the source current. As needs be, plan inverter does not require any unique influence for reimbursing the voltage hang except for the trading and filtering setbacks. The UPQC-Q approach is obliged to voltage list compensation since it can't compensate for the voltage swell [2], [4]. For a comparable measure of rundown pay, UPQC-Q requires greater course of action imbuement voltage degree appeared differently in relation to UPQC-P [2]-[4], [7], [8]. This assembles the VA rating of the plan transformer basically.

Generally, the voltage sags and swells are brief term PQ issues. In this way, in UPQC-P and UPQC_Q, course of action inverter VA stacking might be utilized for brief terms. On the other hand, the shunt inverter VA rating is totally utilized watchful out the operation, as a result of steady load open power support and current consonant pay. To enhance the utilization of course of action some bit of UPQC in the midst of persisting state, some bit of load open power is reinforced by the game plan inverter in UPQC – S [5], {6]. This piece of course of action inverter improves its utilization, and in addition reduces the shunt inverter VA stacking. As a result of the stack responsive power sharing component of the game plan part, the rating of the shunt inverter in UPQC-S may be not as much as that in the UPQC-P. In any case, this is to the burden of a fairly extended course of action transformer rating and diminishment in the rate of swell pay limit.

B. Research Gap

The Literature [1]-[12] does not deal with PR controlled ILBC-UPQC system. This work proposes ILBC to reduce current ripple. The Literature does not deal with PR to improve time response of closed loop controlled ILBC-UPQC system. The PR is proposed since it improves stability and reduces chaotics in output.

II. SYSTEM CONFIGURATION

The block diagram of proposed system is shown in Figure – 2. The capacitor of UPQC is charged by the Output of ILBC. The output voltage of PV is boosted using ILBC.The Battery is replaced by a PV system & ILBC to produce the voltage required to charge the capacitor. ILBC is preferred to single boost converter due to reduced input current ripple.

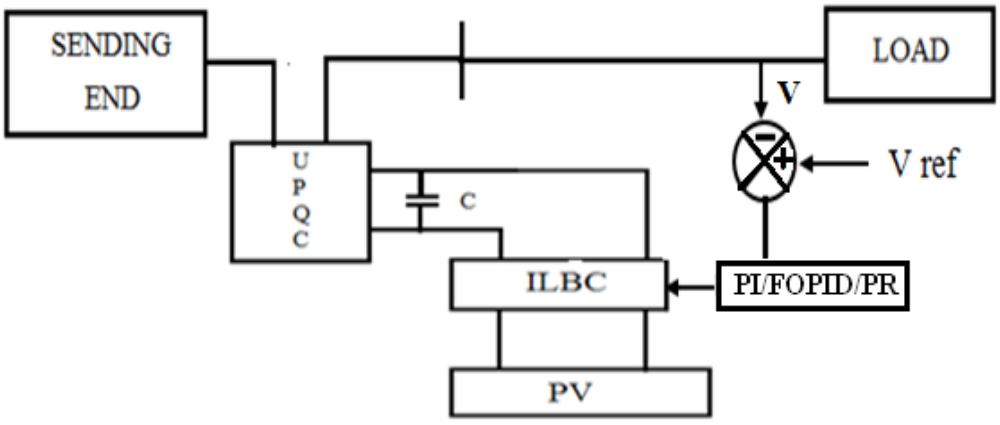

Fig.2: Block Diagram of Proposed ILBC-UPQC System

Load Voltage is sensed and it is compared with the reference voltage. The error is applied to the PI/FOPID/PR Controller. The PI/FOPID/PR updates the pulse width of ILBC to regulate the load voltage.

III. SYSTEM ANALYSIS

Design is done by obtaining the values of V_1, I_1 and frequency of MOSFET. Based on required capacitor voltage, the duty ratio is calculated using the following equation

$$V_0 = \frac{V_1}{(1-a)} \quad (1)$$

Efficiency of the converter to calculatethe output current is

$$\eta = \frac{V_a I_a}{V_1 I_a} \quad (2)$$

The values of L & C are calculated by assuming ΔI & ΔV

$$\Delta V = \frac{V_1 D}{f L} \quad (3)$$

$$\Delta I = \frac{I_a D}{fC} \quad (4)$$

Voltage to be injected is equal to IZ. The active filter is designed to supply fifth harmonic. The value of C_5 is assumed and L_5 is calculated with formula

$$f_5 = \frac{1}{2\pi (L_5 C_5)^{\frac{1}{2}}} \quad (5)$$

Pulse width for switches of DVR inverter is$\frac{T_O}{2}$. Pulse width for switches of AF inverter is $\frac{T_5}{2}$

Total Input current of ILBC is sum of the currents through L_1 and L_2.

$$I_T = I_{L1} + I_{L2} \quad (6)$$

The output of FOPID is as follows

$$V_O(S) = E(S)\left[K_1 + \frac{K_2}{S^m} + K_3 S^n\right] \quad (7)$$

Where m and n are fractions.

The output of PR based system is as follows.

$$V_O(S) = E(S)\left[K_4 + K_5 \frac{\omega}{s^2+\omega^2}\right] \quad (8)$$

K_4 & K_5 are the constants of PR controller

IV. SIMULATION RESULTS

Closed loop controlled UPQC Systems with PI, FOPID& PR Controllers are modeled, simulated and their results are presented in this section. The simulation parameters are as follows.

Table-1: Parameters used for Simulation

PARAMETER	VALUE
Source Parameters -R_1,L_1	0.1Ω, 3mH
R_2,L_2	0.5Ω, 30mH
R_3,L_3	0.8Ω, 40mH
C_{in}	50 µF
C_b	9000µF
K_1	0.2
K_2	0.5
K_3	0.009
K_4	0.9
K_5	0.3
Lt_1,Lt_2	0.1mH, 0.1mH
Load Parameters - R_O,L_O	200Ω, 100mH

A. Closed Loop PI controlled ILBC based UPQC System

Closed loop ILBC-UPQC system with PI controller is shown in Fig 3.1.Line impedance is split into two equal parts. Initial load and additional load are represented as series combination of R & L. Additional load is connected with the help of Breaker-1. Voltage of DVR is injected using Breaker -2. SAF part of UPQC is connected at the sending end of the system. The Output of DVR is injected into the line through a transformer. Load voltage is rectified to convert it to an analog signal. It is compared with the reference voltage. The error is applied to a PI controller. The output of PI controller is applied to pulse generator. The receiving end voltage

is shown in Fig.3.2 and its peak value is 10^4 Volts. The R.M.S receiving end voltage is shown in Fig.3.3 and its value is 6900 Volts. The Real power is shown in Fig 3.4 and its value is $4 * 10^5$ Watts. The Reactive power is shown in Figure 3.5 and its value is $6 * 10^4$ VAR.

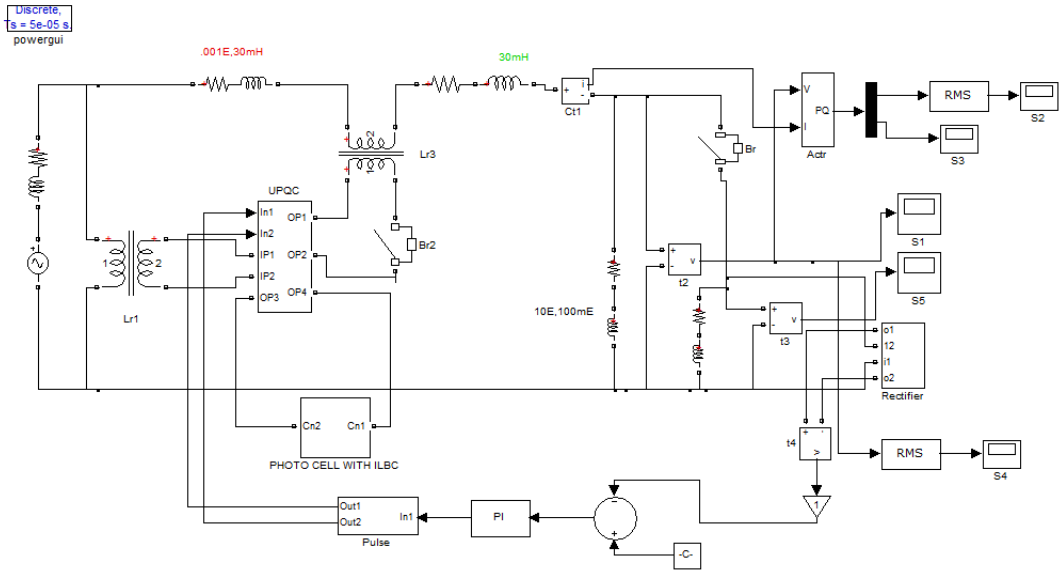

Fig.3.1: Closed loop ILBC-UPQC with PI Controller

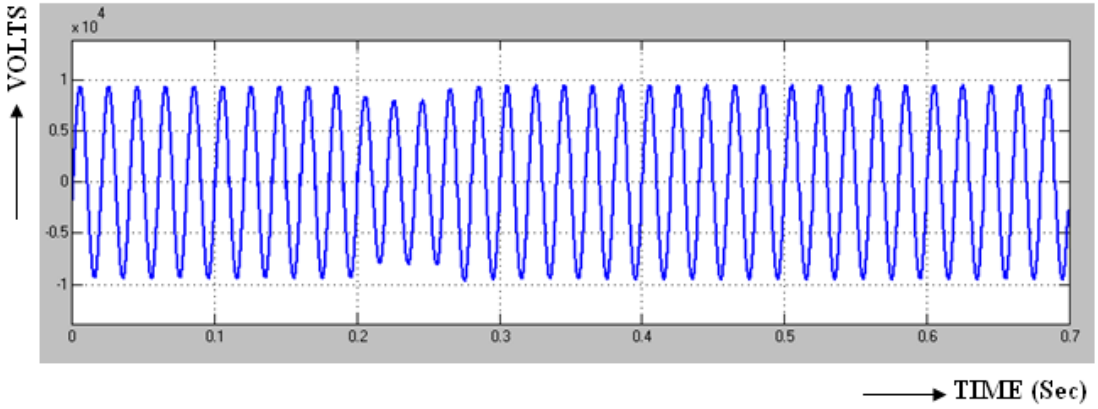

Fig.3.2: Receiving End Voltage

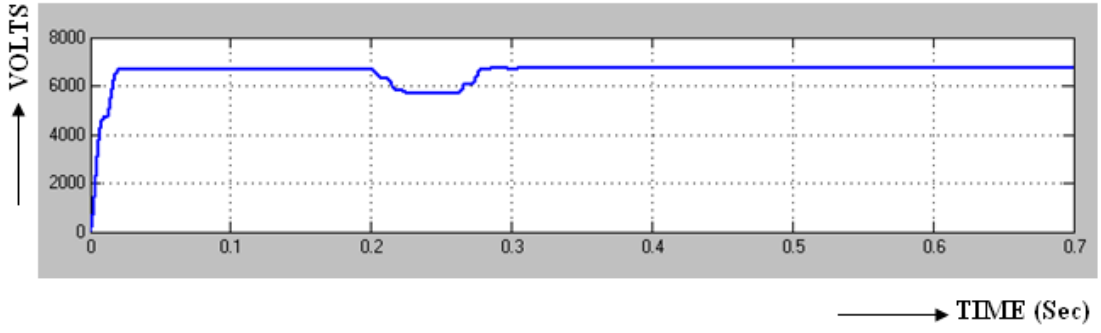

Fig.3.3: R.M.S Receiving End voltage

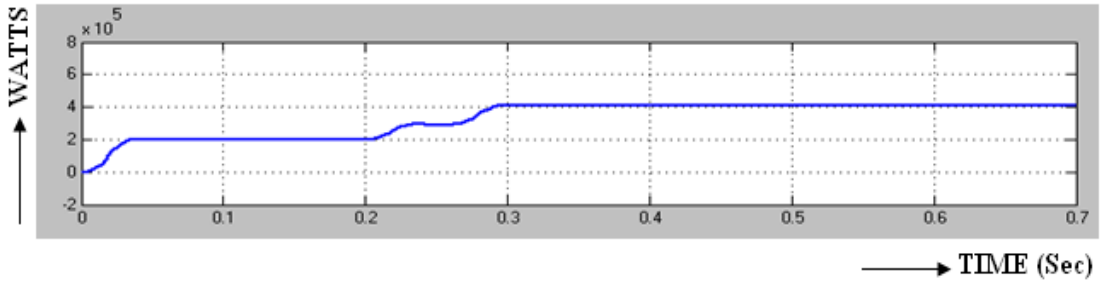

Fig.3.4: Real Power

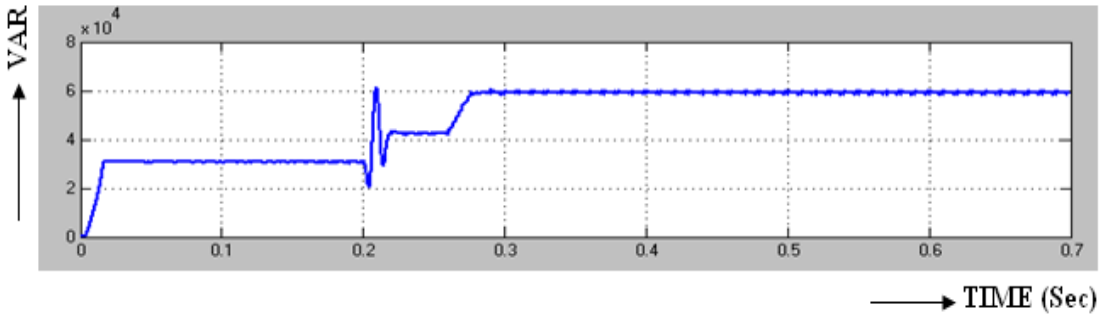

Fig.3.5: Reactive Power

B. Closed Loop ILBC-UPQC System with FOPID Controller

Closed Loop ILBC-UPQC system with FOPID controller is shown in Fig.4.1.The PI controller in Fig.3.1 is replaced by FOPID controller. The receiving end voltage is shown in Fig.4.2 and its peak value is 10^4 V. The R.M.S receiving end voltage is shown in Fig.4.3. and its value is 6100 Volts. The receiving end voltage resumes normal value due to the injection of voltage by UPQC. The Real power is shown in Fig.4.4 and its value is 2.4 * 10^5 Watts. The reactive power is shown in Fig 4.5 and its value is 4.4 * 10^4 VAR.

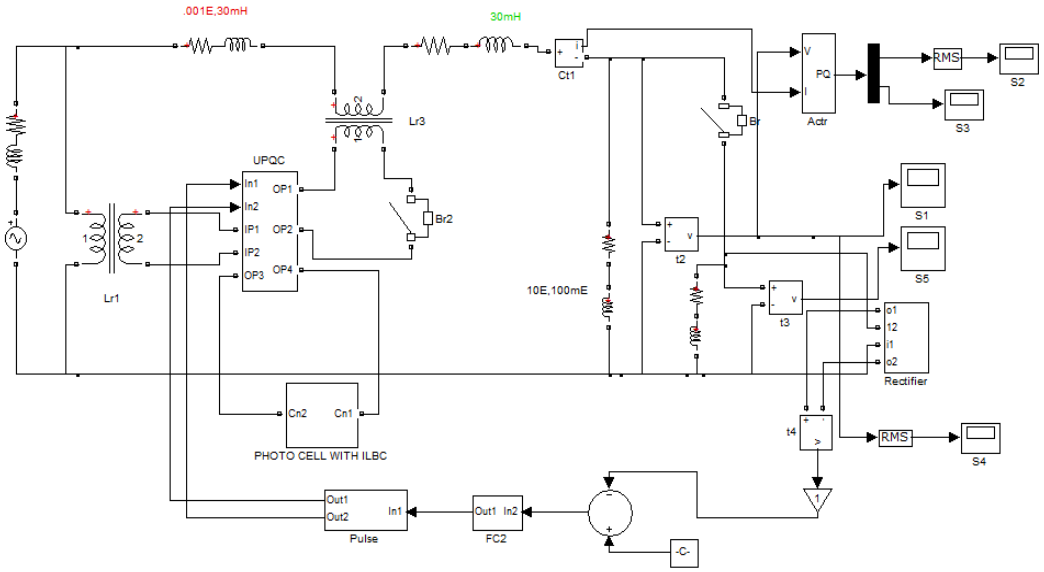

Fig. 4.1: Closed Loop ILBC-UPQC system with FOPID Controller

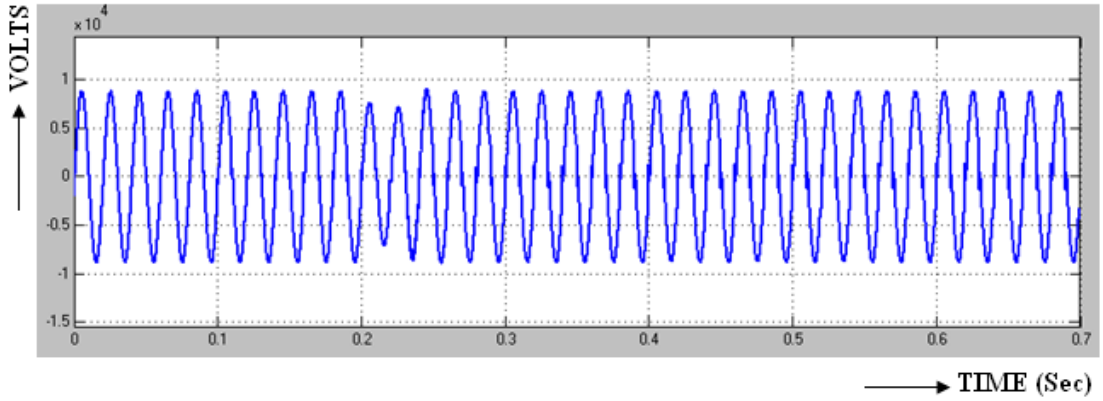

Fig.4.2: Receiving End voltage

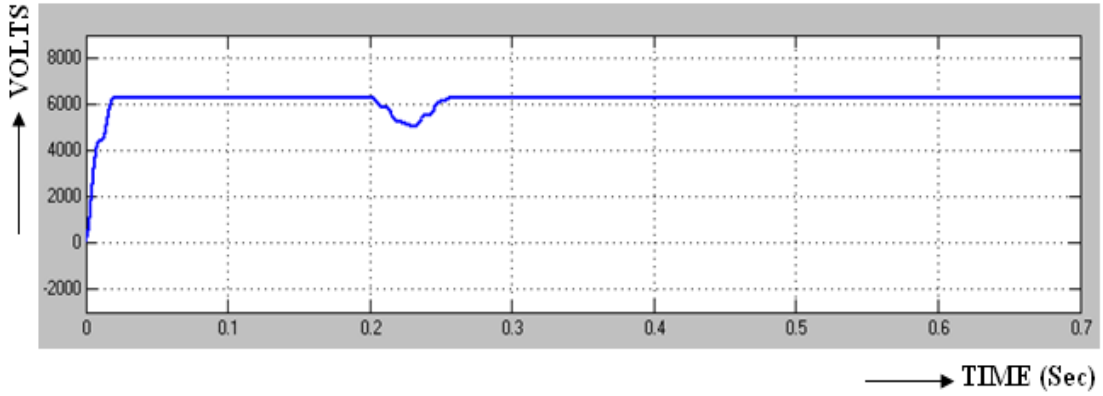

Fig.4.3: R.M.S. Receiving End Voltage

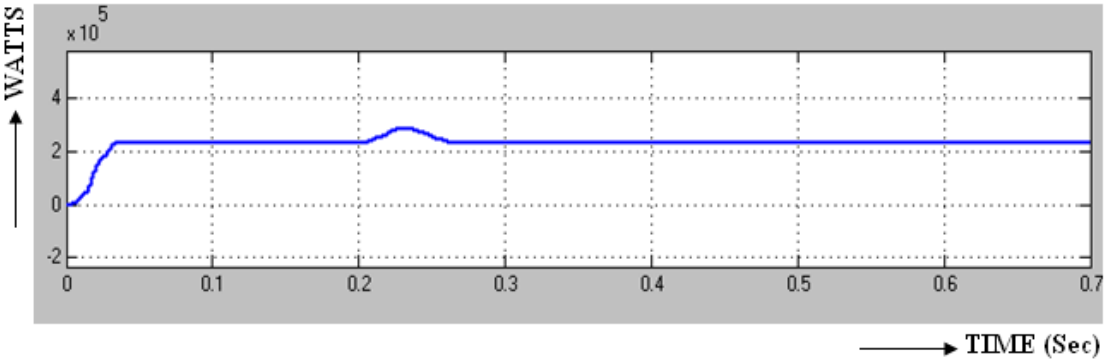

Fig.4.4: Real Power

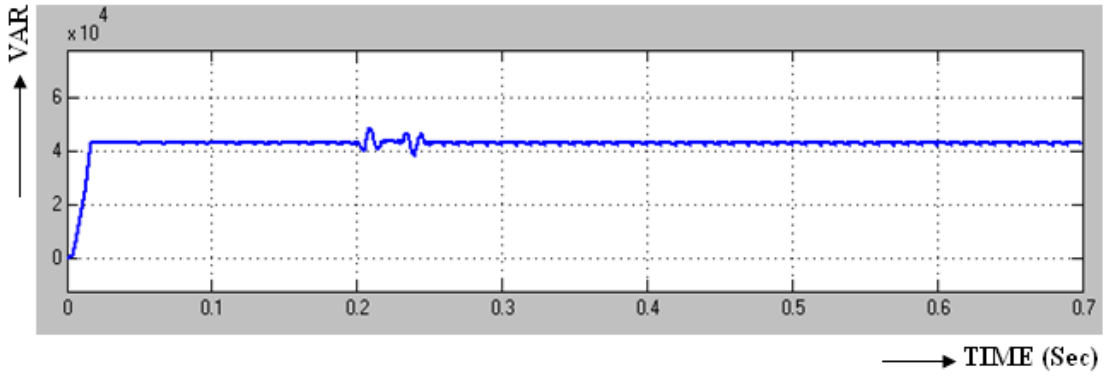

Fig.4.5: Reactive Power

C. Proposed Closed Loop ILBC-UPQC System with PR Controller

Closed Loop ILBC-UPQC system with PR controller is shown in Fig.5.1. The FOPID is now replaced by PR controller. The receiving end voltage is shown in Fig.5.2 and its peak value is 10^4 V. The R.M.S receiving end voltage is shown in Fig.5.3. and its value is 6100 Volts. The Real power is shown in Fig.5.4 and its value is 2.4 * 10^5 Watts. The reactive power is shown in Fig 5.5 and its value is 4.4 * 10^4 VAR.

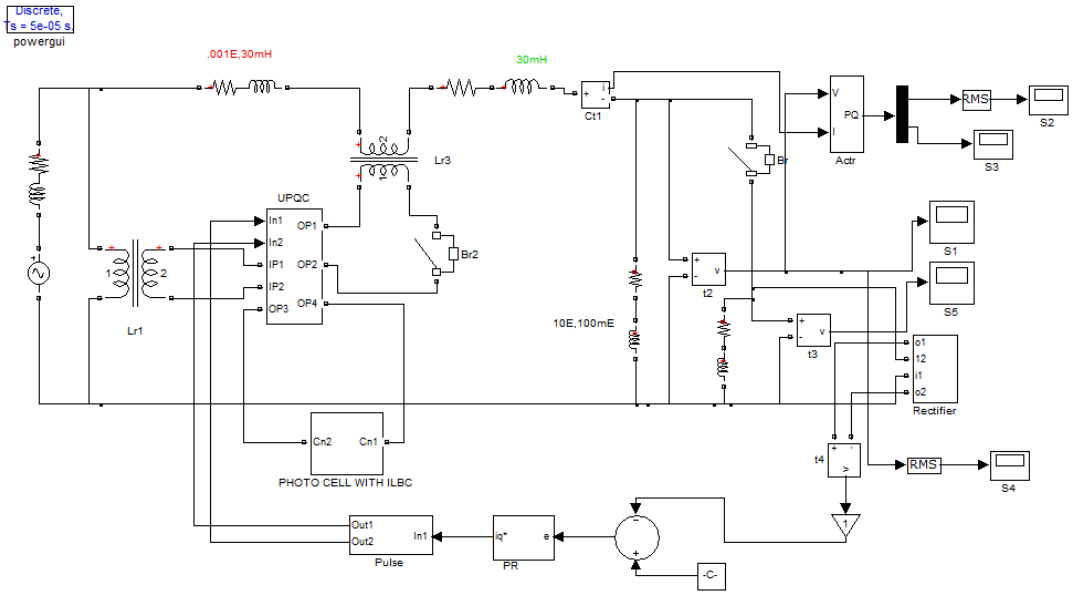

Fig. 5.1: Closed Loop ILBC-UPQC system with PR Controller

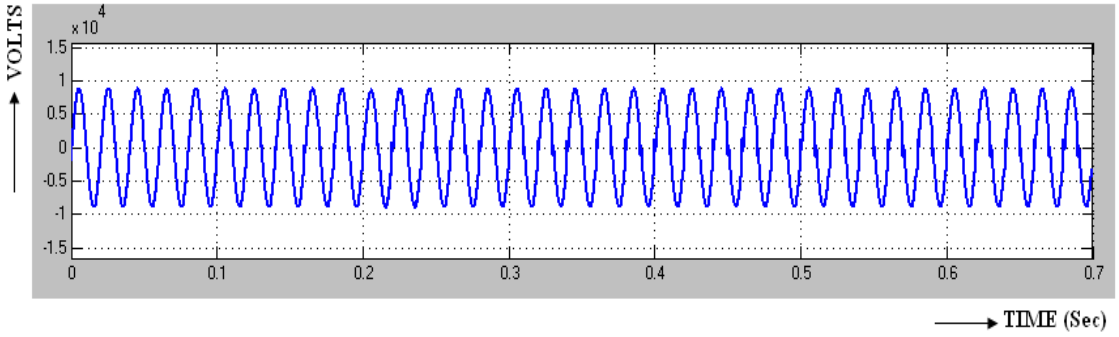

Fig.5.2: Receiving End voltage

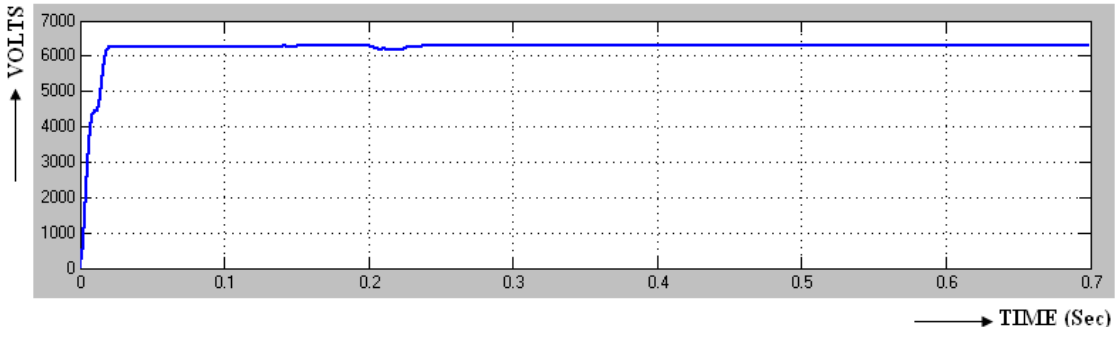

Fig.5.3: R.M.S. Output Voltage

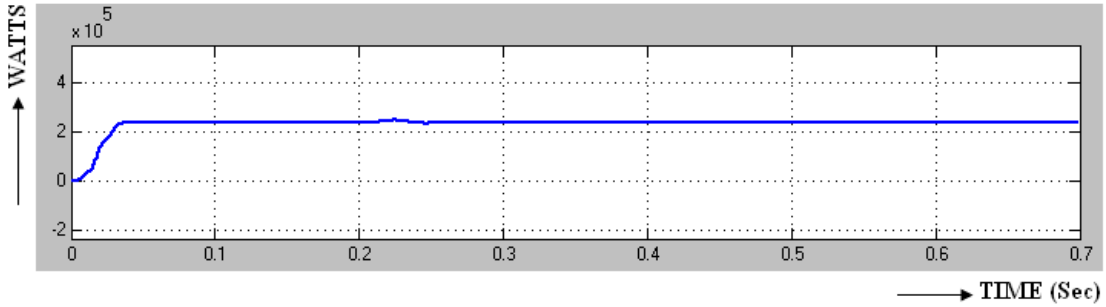

Fig.5.4: Real Power

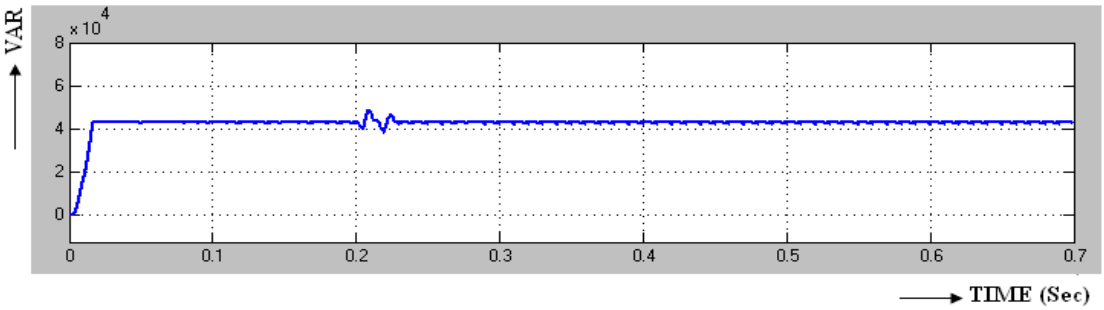

Fig.5.5: Reactive Power

From simulation results the observations of time domain parameters are as follows. The Rise time is 0.23 sec in PI controller, it is reducesto 0.21 sec with FOPID controller it turns to 0.207 sec with PR controller. The Peak time is 0.26 sec in PI controller, is reduced to 0.22 sec with FOPID controller and it turns to 0.21 sec with PR controller. The Settling time is 0.31 sec in PI controller, is reduces to 0.25 sec with FOPID controller and it turns to 0.23 sec in PR controller. The steady state error is reduced from 5.3 V in PI controller, reduces to 2.7 V with FOPID controller and it turns to 1.8 V with PR controller. The comparison of time domain parameters is shown in Table -2.

Table-2:Comparison of Time domain parameters with PI,FOPID & PR Controllers

Controllers	Rise time (s)	Peak time (s)	Settling time (s)	Steady state Error (V)
PI	0.23	0.26	0.31	5.3
FOPID	0.21	0.22	0.25	2.7
PR	0.207	0.21	0.23	1.8

V. CONCLUSIONS

PI, FOPID & PR based ILBC-UPQC systems are modeled and simulated using MATLAB and the results are analyzed. The results indicated that the response with PR is faster than that of PI& FOPID Controlled ILBC-UPQC systems. The settling time is reduced by 0.06 sec when compared with PI and reduced by 0.02 sec when compared with FOPID. The steady state error is reduced by 2.6 Volts by replacing PI with FOPID Controller and also reduced by 0.9V by replacing FOPID with PR controller. The contributions of the present work are as follows: ILBC based UPQC is proposed for power quality improvement. The PR is proposed to enhance time domain response characteristics of ILBC based UPQC system. The advantages of proposed ILBC-UPQC system are reduced ripple and improved time domain response characteristics.The disadvantage is that the hardware of ILBC becomes twice that of HSUC.

The present work deals with comparison of PI, FOPID controlled ILBC-UPQC systems with PR based ILBC-UPQC system. The comparison between PR & FUZZY controlled systems will be done at a later date.

ACKNOWLEDGEMENTS

The authors would like to thankProf. A. Lakshimi Devi, HOD – EEE, Prof. Dr. J. Karthikeyan Principal, M. Devarajulu,Registrar, Prof. Avula Damodaram, Vice – Chancellor, S.V. University, Tirupathi, A.P., India for providing the facilities to conduct Simulation studies in the Power Electronics Lab.

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