Power Efficient Dual Edge-Triggered Storage Design

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***Abstract*— In this work, four conventional most commonly referred master slave dual-edge-triggered storage designs are analyzed. The power efficient master slave dual-edge-triggered storage design is also proposed. A detailed comparison of the existing and proposed designs is presented in this work. All simulations are performed on TSpice using BSIM models in 130 nm process node. The simulation results show that the proposed design has the least power consumption for all data patterns, all supply voltages and all clock frequencies among all the discussed designs and has up to 97.41% lesser power consumption than existing designs. The proposed design has lesser PDP than all existing designs and has up to 97.63% improvement in PDP. The design has improvements in terms of power dissipation and PDP with reduced silicon area. The proposed design is suitable for low power applications of all data patterns and is also suitable for low area applications.**

Keyword - Edge triggered, Pass Transistor, Parasitic capacitance, propagation delay, clocked transistor

I. INTRODUCTION

The rapid scaling of silicon technology has enabled designers to integrate millions and even billions of transistors into a single chip. However, while the performance increases due to scaling, the power density increases substantially every generation due to higher integration density. So, the need for power-efficient design techniques has grown considerably [1]-[3]. The latest advances in mobile battery-powered devices have set new goals in digital VLSI design. These devices require high speed and low power consumption. So, the low power design is must for the applications operated by batteries such as pocket calculators, wrist watches, mobile phones, laptops etc. It is important to prolong the battery life as much as possible [4]-[8]. High power dissipation of a SoC will not only increase its system costs but also affect the product lifetime and reliability. Minimizing power dissipation increases lifetime and reliability of the circuit [9].

Voltage scaling is the most effective way to decrease power consumption, since power is proportional to the square of the supply voltage. However, voltage scaling is associated with threshold voltage scaling which can cause the leakage power to increase exponentially [10]. By using dual-edge triggered flip-flops (DETFFs), the clock frequency can be significantly reduced-ideally, cut in half-while preserving the rate of data processing [11]. In many digital VLSI designs, the clock system that includes clock distribution network and flip-flops is one of the highest power consuming components and accounts for 30% to 60% of the total system power, out of which 90% is consumed by the flip-flops and the last branches of the clock distribution network that are driving the flip-flops [12]. So using lower clock frequency may translate into considerable power savings.

Flip-flops thus contribute a significant portion of the chip area and power consumption to the overall system design. Therefore, it is imperative to carefully design flip-flops for minimum power, area, delay and maximum reliability. Several flip-flop designs have been proposed for power reduction in past. Some of these designs require a large number of transistors for implementation, resulting in a large area, not necessarily suitable for small, low-priced systems. In this work, the existing flip-flop architectures have been extensively studied and new low power and low transistor count double edge triggered flip-flop has been proposed.

This paper is organized into six sections. Section II reviews previous designs of DETFFs. The proposed power efficient DET flip-flop is discussed in Section III. Section IV shows the simulation conditions. Section V presents the results and comparison of existing and proposed flip-flops. The conclusion is given in the last section.

II. EXISTING DUAL EDGE TRIGGERED STORAGE DESIGNS

Several DET flip-flops have been described by replicating the latch elements of a SET flip-flop and multiplexing the output. The Double edge triggered flip-flop shown in figure 1 was proposed by R. Hossain [13]. The structure is based on master-slave pattern. It has two data paths, an upper data path and a lower data path. The upper data path consists of MN1, INV2 and MN3; the lower data path consists of MN2, INV4 and MN4. The input data is in connection with MN1 and MN2 and output is taken from INV5 whose input in turn connected with MN3 and MN4. Each data path have loop within itself for retaining charge levels functionally static. The feedback path in each loop includes an inverter and a PMOS which is switched by clock. The loops

are isolated from each other. When the clock pulse changes from low to high upper loop holds data and lower loop samples the data. But when clock pulse changes from high to low the upper loop switches to sample data and lower loops holds the data.

The Double edge triggered flip-flop shown in figure 2 was proposed by G.M. Blair [14]. The structure is based on master-slave pattern. It has two data paths, an upper data path and a lower data path. The upper data path consists of transmission gates TG1 and TG3 and inverter INV2; the lower data path consists of transmission gates TG2, TG4 and inverter INV4. The input data is in connection with transmission gates TG1 and TG2 and output is taken from inverter INV5 whose input in turn connected with the output of transmission gates TG3 and TG4. The Transmission gates used in both the data paths are clocked such that upper data path works as negative edge triggered flip-flop and lower data path works as positive edge triggered flip-flop. Each data path have loop within itself for retaining charge levels functionally static. The feedback path in each loop includes an inverter and transmission gate.

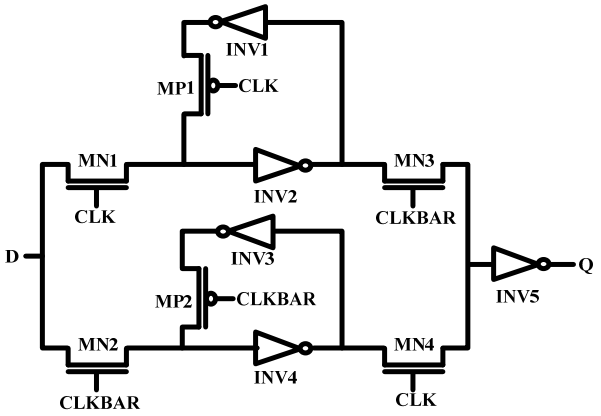

Figure 1: DET Flip-Flop proposed by R. Hossain ($DETFF_{Hossain}$)

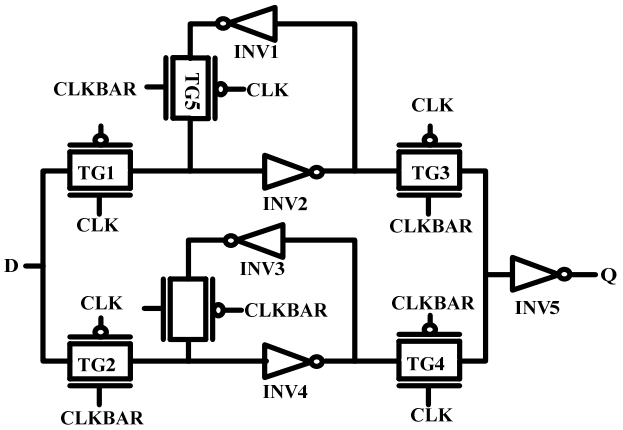

Figure 2: DET Flip-Flop proposed by G.M. Blair ($DETFF_{Blair}$)

The Double Edge-Triggered Flip-Flop, shown in figure 3, was proposed by Imran A. Khan [15]. The structure is based on master-slave pattern. It has two data paths, an upper data path and a lower data path. The upper data path consists of TG1, INV1 and TG2; the lower data path consists of TG3, INV3 and TG4. The input data is in connection with TG1 and TG3 and output is taken from INV5 whose input in turn connected with the output of TG2 and TG4. The Transmission gates used in both the data paths are clocked such that upper data path works as positive edge triggered flip-flop and lower data path works as negative edge triggered flip-flop. Each data path have loop within itself for retaining charge levels functionally static. The feedback path in each loop includes an inverter and pass transistor P1 in upper data path loop and P2 in lower data path loop. It is identical to double edge triggered flip-flop proposed by G.M. Blair (shown in figure 2) except feedback. The feedback transmission gates of this flip-flop are not on critical paths, so in the flip-flop feedback transmission gates are replaced with pass transistors. This improved the power efficiency of the flip flop.

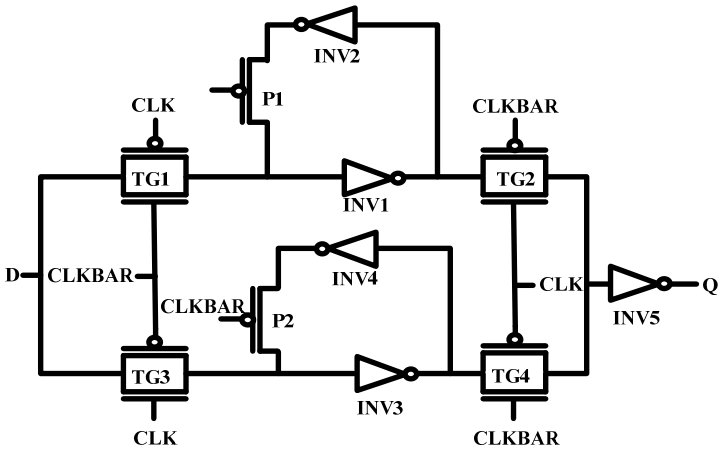

Figure 3: Double Edge-Triggered flip-flop proposed by Imran A. Khan ($DETFF_{Imran}$)

The DET flip-flop shown in figure 4 was proposed by M. Pedram [16]. In this flip-flop the input data controls the passing of the clock signals in the feedback path of both data paths used in the circuit. If clock = 1, TG1 turns on, when D = 0, Node X discharges to 0 and Node Y switches to 1 due to this MN1 turns on. As a result, TG1 and MN1 attempt to write 0 and 1(two different voltages) simultaneously onto Node X. This voltage conflict is present until the clock =0. So this structure allows large current to flow at the input. Similarly in other cases power consumption is increased. Another problem with this circuit is reduction of noise margin. The degraded voltage level at Node X also causes a direct path current in the following inverters. This increases power consumption.

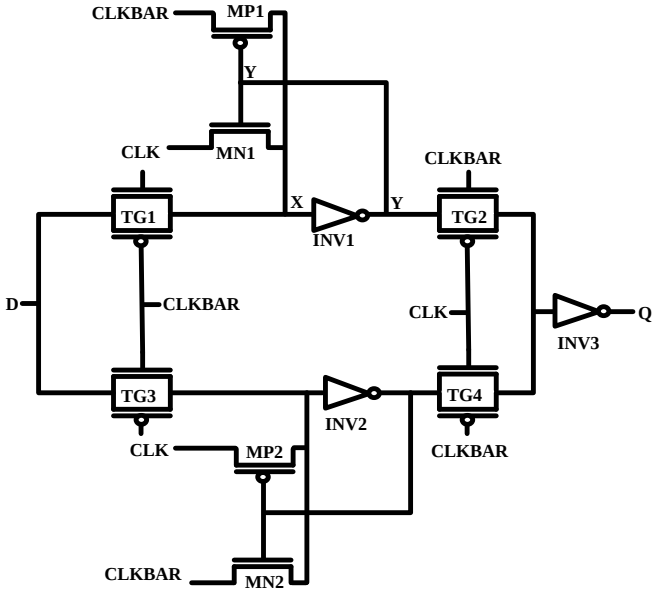

Figure 4: DET Flip-Flop proposed by M. Pedram ($DETFF_{Pedram}$)

III. PROPOSED DESIGN OF POWER EFFICIENT DUAL EDGE TRIGGERED FLIP-FLOP

A new master-slave Dual edge-triggered flip-flop is proposed in the paper. This design is shown in figure 5. Similar to the existing flip-flops, it has two data paths, an upper data path and a lower data path. The upper data path consists of transmission gate (TG1), an inverter (INV1) and another transmission gate (TG3); the lower data path consists of transmission gate (TG2), inverter (INV2) and another transmission gate (TG4). The input data is in connection with the transmission gates TG1 and TG2, the output is taken from inverter INV3 whose input in turn connected with the output of transmission gates TG3 and TG4. The transmission gates used in both the data paths are clocked such that upper data path works as negative edge triggered flip-flop and lower data path works as positive edge triggered flip-flop. The pass transistor P1 and inverter INV4 are used to provide feedback and to make this double edge-triggered flip-flop static in nature.

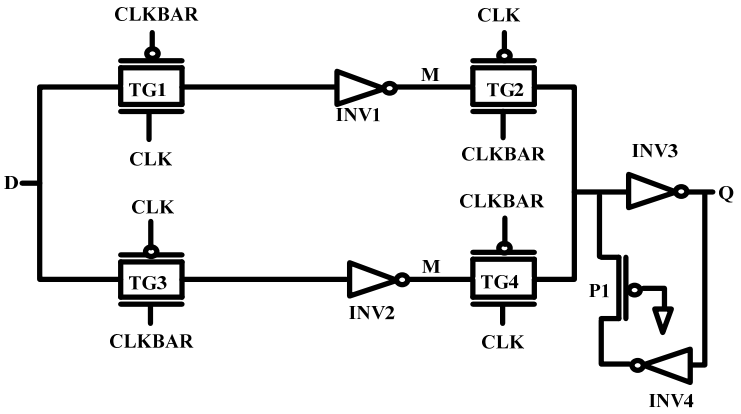

Figure 5: Proposed Power Efficient Double Edge-Triggered Flip-Flop (PEDETF)

The proposed Power Efficient Double Edge-Triggered Flip-Flop (PEDETFF) is identical to double edge triggered flip-flop proposed by G.M. Blair (shown in figure 2) except two things. First is feedback, the double edge triggered flip-flop proposed by G.M. Blair uses an inverter and the transmission gate to provide feedback, while in the proposed design, an inverter with a PMOS is used to provide feedback. This PMOS is grounded; so this transistor is permanently ON to reduce the switched capacitance. Thus there is no clocked transistor in feedback path of the proposed double edge triggered flip-flop. While in the double edge triggered flip-flop proposed by G.M. Blair, there are two transistors (a transmission gate) in feedback of each data path (total four clocked transistors). The power consumption is directly related to the number of clocked transistors. Generally clock has the highest switching activity, so the reduction in number of clocked transistors results in the reduction of power consumption. In the proposed flip-flop, there are only eight clocked transistors. While in the flip-flop proposed by G.M. Blair, there are twelve clocked transistors. Hence four clocked transistors are reduced in the proposed flip-flop to reduce the power consumption.

The second difference between the proposed flip-flop and $DETFF_{Blair}$ is that the feedback paths of upper data path and lower data path are combined in the proposed flip-flop. This decreases the total parasitic capacitance at the internal flip-flop nodes, leading to lower dynamic power dissipation and increased performance. This also results in total chip area reduction due to decreased transistor count. So, the proposed DETFF provides significant die area (wafer cost) savings. The main features of the proposed flip-flop are reduced device count and decreased parasitic capacitances which results in short latency, low power consumption and improved power-delay product.

IV. SIMULATION CONDITIONS

The simulations are performed on TSpice using BSIM 3v3 level 53 models in 130 nm process node. Table I shows the simulation parameters used for comparison. The supply voltage is varied from 1.2V to 2V. The clock frequency is varied from 100MHz to 1GHz. Under nominal condition, a 16-cycle sequence (1111010110010000) with an activity factor of 50% is supplied at the input. But the dynamic power depends on switching activities at various nodes of the circuit. It varies with different data rates and circuit topologies. Hence to obtain a fair idea of power dissipation for a circuit topology, different data patterns should be applied with different activity rates [16]-[18]. So in simulations, following six different data sequences have been adopted to compare the power consumption of flip-flop structures discussed in this paper:

i) 1111111111111111
ii) 0000000000000000
iii) 1111010110010000
iv) 1100110011001100
v) 1010101010101010
vi) 0100000000000000

Table I: CMOS Simulation parameter

Particulars	**Value**	**Particulars**	**Value**
CMOS Technology	130 nm	Temperature	25° C
Min. Gate Width	0.26 µm	Duty Cycle	50 %
Max. Gate Width	1.04 µm	Sequence Length	16 Data Cycles
MOSFET Model	BSIM 3v3 level 53	Nominal Clock Frequency	400MHz
Rise Time of Clock & Data	100 ps	Nominal Supply Voltage	1.6V
Fall Time of Clock & Data	100 ps	Nominal Data Sequence	1111010110010000

Power increases on optimizing a circuit for delay and vice versa. The designs have been simulated to attain minimum power consumption. For fair comparison all the flip-flops have same aspect ratios of transistors for both critical and non critical paths. The transistors of all flip-flops, that are not located on critical path, are implemented with minimum size to reduce area overhead and to minimize power dissipation.

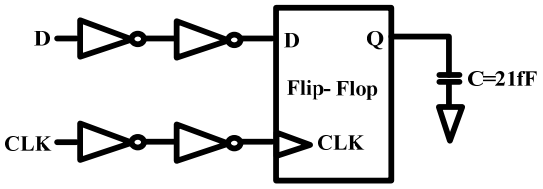

Figure 6: Simulation setup model

The simulation setup model is shown in figure 6. In practical conditions, the flip-flop is generally connected between two logic blocks such that the input to it comes from output of a block and the output of the flip-flop is connected to input of another block. To imitate the signal rise and fall time delays that is to provide realistic clock and data signals, input and clock signals are generated through buffers. To consider the loading effect of the flip-flop to clock network and the previous stage, the power consumptions of the clock and data buffers are also included. A fan-out of fourteen minimum sized inverters (FO14) is used as the capacitance load at node Q. This capacitance load is estimated to be 21fF [3]. So, the output of the flip-flop is loaded with a 21fF capacitor. All the needed inversions are made inside flip-flop. For example complementary clock signals are needed; these inverters are made in the flip-flop structures and are considered in power consumption measurements.

V. SIMULATION RESULTS AND DISCUSSION

Table II shows power consumption in µW as a function of data activity. The proposed PEDETFF has the least power consumption for all data patterns among all the discussed double edge triggered flip-flops. The existing $DETFF_{Pedram}$ consumes the highest power and the existing $DETFF_{Hossain}$ consumes the second highest power for all data patterns. For fair comparison, the average of power consumption at all data patterns is taken. The average results show that the proposed PEDETFF has 71.83%, 63.73%, 64.74% and 94.77% lesser power consumption than existing DET flip-flops respectively. The PEDETFF has up to 97.41% lesser power consumption than existing DET flip-flops.

Table II: Power consumption in µW as a function of data activity

Data Pattern	**000000 00000 00000**	**111111 11111 11111**	**111101 01100 10000**	**110011 00110 01100**	**101010 10101 01010**	**010000 00000 00000**	**Avg (µW)**
DETFF-Hossain	45.8	42.1	64.1	64.5	85.7	51.4	58.93
DETFF-Blair	38.4	38.6	49.0	48.1	59.5	41.0	45.77
DETFF-Imran	42.5	35.3	49.1	49.1	61.6	44.9	47.08
DETFF-Pedram	386.4	217.4	307.4	303.4	313.2	377.0	317.47
Proposed PEDETFF	12.89	13.64	18.03	17.62	23.35	14.04	16.60

Table III compares power consumption (microwatts) as a function of clock frequency. The proposed PEDETFF has the least power consumption among all the discussed double edge triggered flip-flops for all clock frequencies. The existing $DETFF_{Pedram}$ consumes the highest power for all clock frequencies. The existing $DETFF_{Hossain}$ consumes the second highest power for all clock frequencies except at 250MHz and 1GHz, at 1GHz this flip-flop failed and $DETFF_{Imran}$ consumes the second highest power at this frequency. For fair comparison, the average of power consumption at all clock frequencies is taken. $DETFF_{Hossain}$ failed at 1GHz clock frequency. So the average of $DETFF_{Hossain}$ is less because it fails at the highest clock frequency (when there is the highest power consumption). The average results show that the proposed PEDETFF has 59.17%, 64.80%, 63.86% and 94.26% lesser power consumption than existing DET flip-flops respectively. The proposed PEDETFF has up to 97.04% lesser power consumption than existing DET flip-flops respectively.

Table III: Power consumption in μW as a function of clock frequency

Clock Frequency	**100 MHz**	**200 MHz**	**250 MHz**	**400 MHz**	**1000 MHz**	**Avg (μW)**
DETFF-Hossain	34.7	45.4	27.7	64.1	Fail	42.98
DETFF-Blair	30.6	29.1	35.5	49.0	105.1	49.86
DETFF-Imran	20.9	29.5	37.8	49.1	105.5	48.56
DETFF-Pedram	279.04	287.91	294.59	307.4	360.4	305.87
Proposed PEDETFF	8.27	11.0	13.36	18.03	37.11	17.55

Table IV: Power consumption (microwatts) as a function of supply voltage

VDD	**1.2 (V)**	**1.3 (V)**	**1.4 (V)**	**1.6 (V)**	**1.8 (V)**	**2.0 (V)**	**Avg (μW)**
DETFF-Hossain	Fail	Fail	44.6	64.11	96.0	125.83	82.64
DETFF-Blair	28.3	33.8	37.7	49.0	61.7	75.6	56.00
DETFF-Imran	26.6	31.3	35.8	49.1	61.9	77.7	56.13
DETFF-Pedram	108.0	146.6	192.0	307.4	465.9	667.6	408.23
Proposed PEDETFF	11.26	12.30	14.42	18.03	23.45	29.07	21.24

Table IV shows power consumption (in microwatts) as a function of supply voltage. The existing $DETFF_{Pedram}$ consumes the highest power for all supply voltages. The proposed PEDETFF has the lowest power consumption among all the discussed double edge triggered flip-flops for all supply voltages and has 74.30%, 62.07%, 62.16% and 94.80% lesser power consumption than existing DET flip-flops respectively. The power performance of $DETFF_{Pedram}$ degrades with increase in supply voltages. The proposed PEDETFF has up to 95.65% improvement in power performance than existing DET flip-flops.

Table V: Delay (pS) with the variation in supply

VDD	**1.2 (V)**	**1.3 (V)**	**1.4 (V)**	**1.6 (V)**	**1.8 (V)**	**2.0 (V)**	**Avg (pS)**
DETFF-Hossain	Fail	Fail	529.71	250.44	199.91	166.41	286.62
DETFF-Blair	254.07	155.22	118.55	190.17	29.40	20.82	89.74
DETFF-Imran	388.23	315.44	249.14	46.35	25.16	19.05	84.93
DETFF-Pedram	292.81	237.32	288.15	191.17	133.48	110.84	180.91
Proposed PEDETFF	211.42	129.73	178.49	82.73	74.85	60.46	99.13

The table V presents the clock to output delay. $DETFF_{Hossain}$ fails at 1.2V and 1.3V supply voltages and at all remaining supply voltages it has the longest delay. $DETFF_{Pedram}$ has the longest delay at 1.2V and 1.3V supply voltages and at all remaining supply voltages it has the second longest delay. $DETFF_{Imran}$ has the second longest delay at 1.2V and 1.3V supply voltages. As the supply voltage is increased, the speed of $DETFF_{Imran}$ improves and at 1.6V, 1.8V and 2V supply voltages it has the shortest delay. As the supply voltage is reduced, the speed of the proposed PEDETFF improves. At 1.4V and 1.6V supply voltages the design has the second shortest delay and it has the shortest delay at 1.2V and 1.3V supply voltages. The proposed PEDETFF has shorter delay than the existing $DETFF_{Pedram}$ and $DETFF_{Hossain}$ at all supply voltages and comparable delay to $DETFF_{Blair}$ and $DETFF_{Imran}$. The average results reveal that PEDETFF has 65.41% and 45.20% improvement in delay than existing $DETFF_{Hossain}$ and $DETFF_{Pedram}$ respectively. However the flip-flop has 9.47% and 14.32% longer delay than $DETFF_{Blair}$ and $DETFF_{Imran}$ respectively. The proposed PEDETFF has up to 66.97% shorter delay than existing DET flip-flops.

Table VI: PDP (fJ) with the variation in supply voltage

VDD	1.2 (V)	1.3 (V)	1.4 (V)	1.6 (V)	1.8 (V)	2.0 (V)	Avg (fJ)
DETFF-Hossain	Fail	Fail	23625.07	16055.71	19191.36	20939.37	23686.07
DETFF-Blair	7190.18	5246.44	4469.34	9318.33	1813.98	1573.99	5025.16
DETFF-Imran	10326.92	9873.27	8919.21	2275.79	1557.40	1480.19	4766.84
DETFF-Pedram	31623.48	34791.11	55324.80	58765.66	62188.33	73996.78	52781.69
Proposed PEDETFF	2380.59	1595.68	2573.83	1491.62	1755.23	1757.57	2105.57

Table VII: Number of Transistors and Clocked Transistors

Flip-flop	Number of Transistors	Number of Clocked Transistors
DETFF-Hossain	16	6
DETFF-Blair	22	12
DETFF-Imran	20	10
DETFF-Pedram	18	12
Proposed PEDETFF	17	9

The table VI presents the clock to output PDP (in fJ). The existing $DETFF_{Pedram}$ has the highest PDP for all supply voltages. The existing $DETFF_{Hossain}$ failed at 1.2V and 1.3V and for all remaining supply voltages, this existing DET flip-flop has the second highest PDP. For all supply voltages, the proposed PEDETFF has the lowest PDP except 1.8V and 2V. At these two supply voltages $DETFF_{Imran}$ has the least PDP. The average results show that the proposed PEDETFF has 91.11%, 58.10%, 55.83% and 96.01% improvement in PDP than the existing flip-flops respectively. The simulation results show that the proposed PEDETFF has up to 97.63% lesser PDP than existing DET flip-flops. Table VII shows the number of transistors and clocked transistors of the proposed and existing flip-flops.

VI. CONCLUSION

In this paper, a detailed analysis on master slave low power and high-performance double edge triggered flip-flops are presented. It can be observed that the existing $DETFF_{Pedram}$ consumes the highest power for all data patterns, all clock frequencies and all supply voltages. The existing $DETFF_{Hossain}$ failed at 1.2V and 1.3V and for all other supply voltages the flip-flop consumes the second highest power and has the longest delay. The $DETFF_{Pedram}$ has the second longest delay for all supply voltages. $DETFF_{Pedram}$ has the highest PDP for all supply voltages among all the discussed DET flip-flops.

The proposed PEDETFF has the least power consumption for all data patterns, all supply voltages and all clock frequencies among all the discussed double edge triggered flip-flops. The simulation results show that the proposed PEDETFF has up to 97.41% lesser power consumption than existing DET flip-flops. The proposed PEDETFF has shorter delay than the existing $DETFF_{Pedram}$ and $DETFF_{Hossain}$ at all supply voltages and comparable delay to $DETFF_{Blair}$ and $DETFF_{Imran}$. As the supply voltage is reduced, the speed of the proposed PEDETFF improves. For all supply voltages, the proposed PEDETFF has lesser PDP than all existing DET flip-flops except few conditions; at 1.8V $DETFF_{Imran}$ and at 2V $DETFF_{Blair}$ and $DETFF_{Imran}$ have lesser PDP than PEDETFF. The simulation results show that the proposed PEDETFF has up to 66.97% shorter delay and up to 97.63% lesser PDP than existing DET flip-flops.

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