ISSN (Print) : 2319-8613
ISSN (Online) : 0975-4024 

# Scaling Effect on Parameters of $HfO_2$ Based CSDG MOSFET

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***Abstract* - To make obvious the advantages of Nanoelectronic circuits with addition of functionality and chip density compared to the simple switch, application of cylindrical surrounding double-gate (CSDG) MOSFET is suitable. In addition to the Silicon-dioxide, in this present work, a high dielectric material ($HfO_2$) has been added. Various parameters such as scaling of device, thermal effect, *ON*-resistance and capacitances, equivalent oxide thickness, capacitance equivalent thickness, and breakdown of a CSDG MOSFET has been discussed. This provides an improved MOSFET to drive the nanotechnology circuit with minimum signal propagation delay.**

***Keywords*** **-** High dielectric constant, $HfO_2$, Cylindrical surrounding double-gate MOSFET, Nanotechnology, VLSI.

## I. INTRODUCTION

The radio frequency micro-electro-mechanical switch (RF MEMS) have been considered as an alternative to the solid state switches due to fast switching, low loss, high isolation and linearity with less power consumption [1-3]. In addition to this, the electronic switch is also performing better with the application of high dielectric material as $HfO_2$, which has been analyzed in this present research work [4, 5]. *Padovani et. al.* [6] have proposed a model which describes the operations of $HfO_2$ based resistive RAM devices at microscopic level. The $HfO_2$ based resistive memory with TiN electrodes has been analyzed in ref. [7] and integrated with *0.18* $\mu m$ CMOS technology.

The nanowires, FinFET, gate all around (GAA) has been the focus of consideration for the application of Microelectronics / Nanoelectronic engineering due to their short channel effects (SCE) and enhanced current capability in devices [8-11]. In this work an extended version of GAA has been analyzed. It has the double-gate and cylindrical structure, hence the name cylindrical surrounding double-gate (CSDG) MOSFET [12]. Its effective resistance $R_{ON}$ is less as it is inversely proportional to the transconductance (which is higher for $HfO_2$ than $SiO_2$). So it is better to utilize the $HfO_2$ for CSDG MOSFET. The attenuation is proportional to *ON*-resistance, so it can be improved with the help of $HfO_2$. For the switching circuits, if no any dc current available, then the average dynamic power will be $P_{avg} = C_L.V_{DD}^2.f$ based on the band gap theory as in table I [13, 14]. The average dynamic power due to $V_{DD}$ for $HfO_2$ is less and better for the CSDG MOSFET.

To design a high frequency and radio frequency switches for telecommunication systems and devices, a high dielectric constant material ($HfO_2$) in this CSDG MOSFET has been introduced. This work has been organized as follows. The scaling process for the CSDG MOSFET with the $HfO_2$ has been discussed in the Section II. The detailed CSDG MOSFET design with $HfO_2$ and its brief fabrication techniques has been given in the Section III. The various parameters as thermal effect, resistance and capacitances, equivalent oxide thickness, capacitance equivalent thickness, and breakdown have been analyzed in the Section IV. Finally, the Section V concludes the work and recommends the future aspect.

## II. SCALING OF CSDG MOSFET

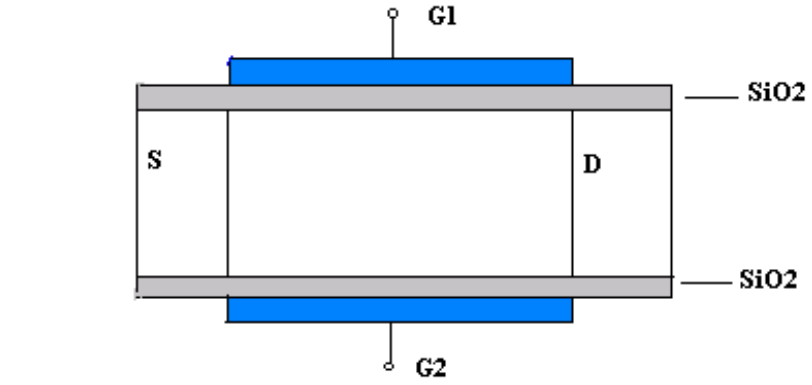
Moore's law is an observation about the component density and performance of the integrated circuits that these parameters are doubles every year, and later it has been revised to double in every two years [15]. The reduction in the thickness of silicon dioxide increases the device density in a particular area of the chip design and produces the higher performance and switching speed. Scaling of the device means to minimize the size of MOSFET with the help of gate length, channel length etc. The CSDG MOSFET has the same channel length as of the traditional MOSFET but resulting channel length doubles due to the internal channel and external channel as shown in fig. 1. If the scaling is beyond the limit, then drain voltage reduces the barrier height at source which lowers the source to channel barrier height. This phenomenon is known as drain-induced barrier lowering (DIBL) [16].

TABLE I. PROPERTIES OF $HfO_2$ AND $SiO_2$

| Properties | $HfO_2$ | $SiO_2$ |
|---|---|---|
| Crystal structure | Monoclinic Cubic | Amorphous |
| Dielectric constant | 20 to 25 | 3.9 |
| Solubility | Insoluble | Insoluble |
| Density ($g/cm^3$) | 9.68 | 2.2 |
| Transition temperature (°C) | 2100 | 867 |
| Melting point (°C) | 2812 | 1600 |
| Band Gap (eV) | 5.68 to 6.00 | 8.9 to 9.0 |
| Work function (eV) | 1.5 | 3.5 |
| Crystal size (nm) | 5 to 50 | -- |
| Stability with Silicon | Yes | Yes |
| Thickness (nm) | 3 to 5 | 2 |

In a MOSFET the tunneling of carriers from source to drain results in a leakage current [17]. So the use of $HfO_2$ above the $SiO_2$ layer is suitable to reduce this type of leakage as shown in fig. 2(b). Also, a control on the channel and source and drain doping profiles can be achieved by the CSDG MOSFET which provides high ON/OFF current ratio.

The scaling restriction is due to its parasitic resistance and capacitance as the distance between MOSFETs in the design / chip design becomes too small. The leakage current depends on barrier height and with the use of $HfO_2$, this height can be increased, so the leakage current can be reduced. It can also be achieved with the same equivalent oxide thickness (EOT) which has been discussed in the following sections. Due to high thickness in the design, the reliability of oxide layers can be enhanced [18]. Scaling of the solid state devices improves the performance and power of the system. The big challenge is that the end of planar CMOS transistor scaling is near as the transistor size approaches to nanometers [16]. As the scaling of traditional MOSFETs device is approaching its limit, new materials are needed to improve the device performances. *Yurchuk et. al.* [19] have analyzed the impact of scaling on memory performance of Ferroelectric field effect transistors (Fe-FET) devices employing Si:$HfO_2$ ferroelectric films. In this work $HfO_2$ has been used with the CSDG MOSFET.

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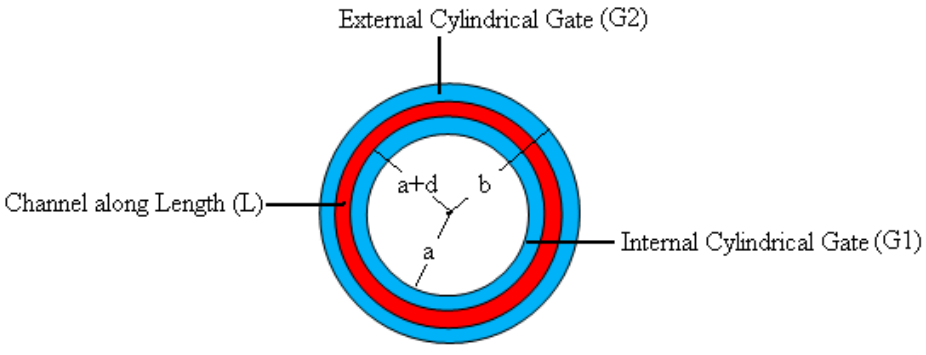



(b)

Fig. 1. Basic model of a) Double-gate MOSFET and b) side view of cylindrical surrounding double-gate MOSFET [12].

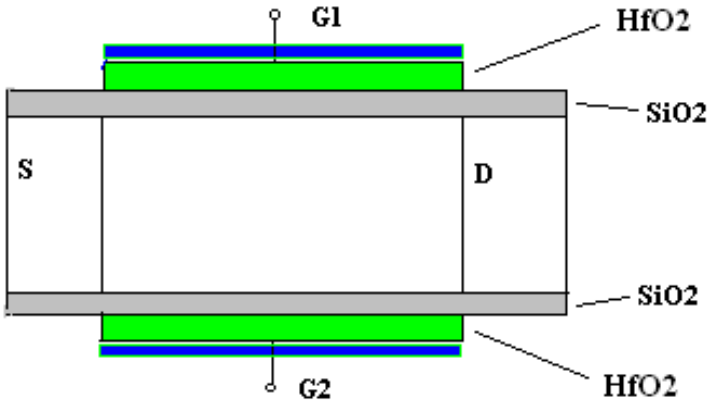
## III. $HfO_2$ Based CSDG MOSFET

For the device scaling beyond the *65 nm* technology, the thickness of $SiO_2$ based gate oxides reduced to *<1 nm*. At these gate dielectric thicknesses, the gate leakage current, channel mobility, and oxide breakdown degraded. So it is better to replace the dielectric with higher permittivity (*high-k*) material. The suitable *high-k* material should be of higher resistivity, barrier height, and should form an ideal interface (junction / contact layer, defect free) with the Silicon. It can be grown for the equivalent oxide thickness, thus considerable gate leakage reduction [20-22]. The considerations on leakage, limits the physical gate length to *20 nm* [23]. Some oxides such as $HfO_2$, $Y_2O_3$, and $ZrO_2$ are in the focus for research work. Metal silicates (Hf, Y and Zr) are also the area of interest due to their thermal stability with Silicon.

The $HfO_2$ layers can be deposited by the process like atomic layer deposition, metal organic chemical vapor deposition or molecular beam deposition [24-26]. *High-k* materials can also be deposited on the Germanium (*Ge*) surface by physical or chemical vapor deposition.

The $HfO_2$ based RF MOSFET switches are interesting in microelectronics and nanotechnology for microwave systems due to superior characteristics such as scaling, high isolation, low insertion loss, low signal distortion, and higher switching speed. These parameters show a possibility in RF applications compare to traditional MOSFETs. The switching mechanisms of RF switches are formed in capacitive contact (metal to dielectric) and dc contact (metal to metal). The $HfO_2$ layer above the $SiO_2$ layer provides strong capacitive coupling and electrical isolation performance due to high permittivity, and thermal isolation as shown in fig. 2.

In this work a CSDG MOSFET has been considered. The basic of the CSDG MOSFET is the DG MOSFET which has been rotated along its horizontal axis [12, 27, 28] as shown in fig. 1. After designing the CSDG MOSFET, its dielectric material combination has been changed as shown in the fig. 2 with the $HfO_2$. In the present work, author has implanted a high-k dielectric material as $HfO_2$ in between the gate and Silicon substrate. The motivation to replace $SiO_2$ with $HfO_2$ is due to its high dielectric constant (*20* to *25*) and for $SiO_2$ it is only *3.9*. The $HfO_2$ has its superb adhesion property to the metals (connecting wires), which is a substitute for ultra-thin gate oxide in the MOSFET due to thermal stability.

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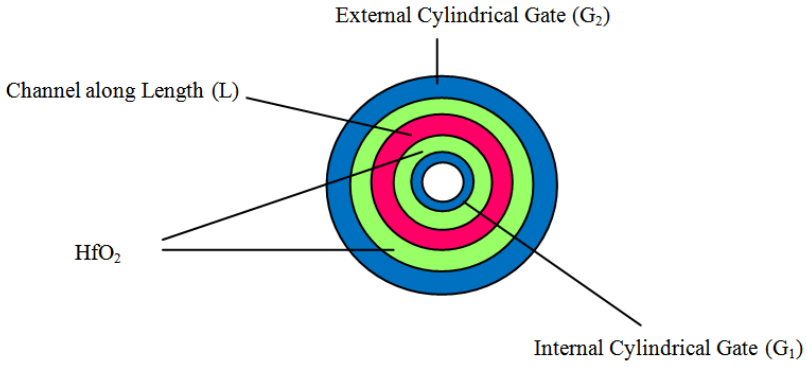


(b)

Fig. 2. Basic model of $HfO_2$ based a) Double-gate MOSFET and b) side view of cylindrical surrounding double-gate MOSFET.

The $HfO_2$ is thermally stable with the Si for deposition and for high temperature fabrication and processing. The *k*-value below *25* reduces the fringing effects. High permittivity, moderate band gap and band alignment to the substrate, better film morphology, interface quality are compatible with presently used materials in processing of MOS devices. It also has Fermi level controllability, process compatibility and reliability.

## IV. PARAMETERS ANALYSIS

The designed $HfO_2$ based CSDG MOSFET with layer $SiO_2$-$HfO_2$-Metal has been analyzed in this section. The main objective is to observe the parameters related to the $HfO_2$ and cylindrical structure. In this work, some physical parameter as scaling, thermal effect, resistor and capacitors, equivalent oxide thickness, capacitance equivalent thickness, and breakdown has been discussed.

### *A. Scaling of Si: $SiO_2$: $HfO_2$: Metal*

For very large and ultra large scale devices (VLSI and ULSI), the transistors are of micro and nano sized, having a benefit of the short connecting wires, which reduces the path delay ($CV_{DD}/I$) and low switching energy ($CV_{DD}^2/2$). So the channel length and other lengths of the devices should be as smaller as possible. In the CSDG MOSFET, two channels are formed (as compared to the same traditional sized MOSFET) which creates double path (channel) for the flow of current, so the path delay will be half such as ($CV_{DD}/2I$). It means the signal can travel faster with CSDG MOSFET. The low power demands low $V_{DD}$ so lower $I_{off}$ [29]. The $HfO_2$ used in the CSDG MOSFET can also be scaled down due to its crystal size and thickness as shown in table I.

Also, the *high-k* gate dielectrics are amorphous and can be deposited by chemical vapor deposition, not like the crystalline film's molecular beam epitaxy. This is due to the variations in grain size (*10 μm*) and orientation of crystallographic structure. The leakage current increases with the grain boundaries of crystallized films [18]. This effect can be minimized in the $HfO_2$ based CSDG MOSFET due to the availability of $SiO_2$.

### *B. Thermal Effect*

In the latest technologies, the *high-k* dielectrics, such as hafnium oxide ($HfO_2$) is replacing the traditional $SiO_2$ dielectric in silicon devices. The $HfO_2$ has melting point *2812 °C*, the crystal temperature is *1100 °C* and for $SiO_2$ it is *500 °C*. The $HfO_2$ is thermodynamically stable and resistive to the impurity diffusion because of high density with the lattice parameter which is comparable to the Silicon with a small lattice misfit (*<5%*) [30]. In fig. 2, the $HfO_2$ layer is on the external to the $SiO_2$ layer, so the device can be used in high temperature application, as the external $HfO_2$ can tolerate the higher temperature. Also, as the temperature increases, the thickness of the $HfO_2$ layer is high enough such that the heating effect can't affect the properties of the $SiO_2$. So the properties of the switching will not be affected. That's the reason of using the $HfO_2$ layer at the external to the $SiO_2$ layer. It can be used in the high power switches, boiler temperature meter, and process temperature.

Due to the cylindrical structure, it needs less contact area on the base / board. Hence less heat effect will be on this device, makes suitable this for applications.

### *C. ON-Resistance*

The effective *ON*-resistance ($R_{ON}$) of the $HfO_2$ based CSDG MOSFET is resistance measured at ON condition from drain to source terminal. The $R_{ON}$ changes with temperature, connection in application, and the supply voltage etc. The ON-state resistance for the model of fig. 2(b) can be approximated as:

$$R_{ON} = \frac{1}{\mu_{eff} C_{ox} \frac{W}{L}\left(V_{gs_{eff}} - V_{th_{eff}}\right)} \tag{1}$$

where $L$ and $W$ are the gate length (depending on technology) and gate width ($2\pi r$, where $a < r < b$, in the discussed model), respectively. The $V_{gs}$ and $V_{th}$ are gate or control voltage and threshold voltage respectively. Here these voltages are the effective voltage with the $HfO_2$ and $SiO_2$. Means $V_{gs,eff} = V_{gs,HfO2} + V_{gs,SiO2}$ and $V_{th,eff} = V_{th,HfO2} + V_{th,SiO2}$. In this equation, $\mu_{eff}$ is the effective electron mobility given is:

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_{SiO_2}} + \frac{1}{\mu_{HfO_2}} \tag{2}$$

where it is *1400 $cm^2/Vs$* for $SiO_2$ and *40 $cm^2/Vs$* for the $HfO_2$. Also $R_{ON_{HfO_2}(based)} < R_{ON_{SiO_2}}$. This concludes that the ON-resistance is less in the designed model (with $HfO_2$). So the higher signal can pass through the proposed CSDG MOSFET at the switch-ON state. Since these two resistances are parallel to each other. Hence

$$R_{total-HfO_2\ based} = R_{SiO_2} \text{II} R_{HfO_2} \tag{3}$$

The attenuation depends upon $R_{ON.}$ To lowering the attenuation, $R_{ON}$ should be low. It can be done by using $HfO_2$ as $L/W$ is low, $\mu_{eff}$ is high, and $R_{total}$ is low by Equation (3) as compared to the traditional MOSFET. The resistive switching in metal oxide thin films can be used in non-volatile memory (NVM).

*D. Total Oxide Capacitance*

The oxide capacitance is the combination of the silicon and hafnium oxide capacitances. In this design the $C_{ox}$ is the parallel combination as follows:

$$C_{ox} = C_{ox_{SiO_2}} \text{II} C_{ox_{HfO_2}}$$

So finally,

$$C_{ox_{(total-HfO_2\ based)}} = C_{ox_{SiO_2}} + C_{ox_{HfO_2}} \tag{4}$$

By this phenomenon the overall oxide capacitance increases for the $HfO_2$ based CSDG MOSFET, which helps to reduce the leakage of electrons across the dielectric (also due to two layers one is $HfO_2$ and second is $SiO_2$). In this way the SCE can be improved. Also the switch ON time can be increased which increases the switching speed of the device.

*E. Equivalent Oxide Thickness*

An equivalent oxide thickness (EOT) is a measure of thickness of a layer by which circuit designer can analyze about the $SiO_2$ film thickness to produce the same effect for the *high-k* material (for $HfO_2$) for the same device [13]. The device performance can be improved by reducing the thickness of $SiO_2$ layer. But this reduction has the limitations, so the $HfO_2$ is useful to get the same EOT from a thicker layer as discussed below with the help of equivalent oxide thickness. In scaling the Silicon-dioxide can be thinner but direct tunneling can occur that's the reason in this work $HfO_2$ above the layer of $SiO_2$ as shown in the fig. 2 has been used. As the thickness approaches below *22 nm* (based on technology), leakage is a challenging problem and alternate materials such as $HfO_2$ becomes necessary to increase the thickness for the same switching speed. The EOT can be written as:

$$EOT = \frac{k_{ox}}{k_{high-k}} t_{high-k} \tag{5}$$

where $k_{ox}$ and $k_{high\text{-}k}$ are the dielectric constant of oxide and high-k dielectric oxide, and $t_{high\text{-}k}$ is thickness of high-k dielectric layer. This equation doesn't have the channel length term so it is independent of the structure. It only depends on the dielectric constant and the thickness of the layers. According to the Equation (5) a high-k material with thicker films can be used. As the $HfO_2$ has dielectric constant of *20* to *25* and $SiO_2$ has *3.9*, detailed in Table I ($k_{ox} < k_{high\text{-}k}$). So if the ratio of the t/k is matched then the suitable EOT can be achieved and the scaling properties will be satisfied. In this case, it can make approximately six times thicker than silicon dioxide. Hence the tunneling current reduces accordingly. As per the *45 nm* technology node, the EOT of the silicon dioxide required to be less than *1 nm*.

*F. Capacitance Equivalent Thickness*

With the limit on the number of layers as discussed with EOT, the gate metal and the thermal efficiencies, a highly scaled gate stack can be designed. The parameter used to realize these gate dielectrics are the capacitance equivalent thickness (CET), can be written as [21]:

$$CET = \frac{\varepsilon_o k_{SiO_2} A}{C} \tag{6}$$

where *C* is the capacitance of the MOSFET structure measured at a given gate bias. For the designed $HfO_2$ base CSDG MOSFET, it can be written as:

$$CET_{HfO_2-based} = \frac{\varepsilon_o k_{SiO_2} (2\pi rL)}{C_{ox_{SiO_2}} + C_{ox_{HfO_2}}} \tag{7}$$

Here the *L* is the channel length and the *r* is radius $a < r < b$. The CET depends on the chosen gate bias. In this equation it has been assumed that the other capacitors (like parasitic and overlapping) are very small or negligible. For this structure the CET decreases as the capacitance increases by the value of $HfO_2$ based capacitance and the *r* is lower as *a* and *b* is small due to nanotechnology scaling. This CET can also be influenced by gate leakage. Generally, the CET below *1 nm* is required for technology nodes beyond *16 nm* technology [31]. Using the $HfO_2$ based CSDG MSOEFT as in fig. 2 with the Equation (4), the capacitance increase, which reduces the CET as in Equation (6). So the CET lowers for the proposed model.

### *G. Dielectric Strength or Breakdown*

In the MOSFET, the breakage or cracks of the oxide layer can cause due to initial defect (at the time of fabrication) and / or deterioration of the oxide layer. This strength is the maximum electric field of a material that can withstand before breaking down and if the applied electric field is beyond this limit then the oxide layer may be broken. Also, if low electric field is applied for the long time then it can be a reason of oxide layer breakage [32]. As in the designed CSDG MOSFET, the *high-k* material is used as a layer onto the Silicon oxide layer, so the initial defects can be straightforward removed. In the second case, electric field is applied, then due the addition of $HfO_2$ layer this electric field will have less effect as compared to the only $SiO_2$ layer.

Bur if in any circumstances, breakdown occurs then the second gate ($G_2$) can be used as this is the opposite of the first gate ($G_1$). So this designed device can withstand or tolerate the breakdown of the device for the longer period. This property is useful for the high current applications.

## V. CONCLUSIONS AND FUTURE RECOMMENDATIONS

In the above discussions of the $HfO_2$ based CSDG MOSFET, it can be conclude that the thermal effect (decreases), resistance (decreases) and capacitances (increases), equivalent oxide thickness, capacitance equivalent thickness, and breakdown (reduces) has been improved.

The low gate leakage current, thinner EOT are the challenges which has not been discussed in this work. It can be considered in future analysis. The insulating properties of the high dielectric material can be tuned by applying specific electrical fields (resistive switching property) can also be discussed in future work with the help of NVM.

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