An Innovative Design Approach of SoC Based Smart CMOS Sensor for Mixed Signal Processing based Applications

RajinderTiwari
Department of Electrical & Electronics Engineering
ASET, Amity University, Lucknow
email: trajan@rediffmail.com

***Abstract*—The CMOS based sensor design technology has evolved with tremendous applications in MSP domain with enhanced characteristic of maximized S/N ratio. This feature has been obtained with the utilization of pixel-based amplification in addition to minimizing the presence of the noise at the output of the device. It means that the noise present in the various active device of the system has been suppressed with the help of SoC based design technique i.e. three level pixel implementation. This system basically supports all the SoC components such as feedback amplifier, buffers, tapered reset device, etc. The CMOS based smart system has both software as well as hardware modules which in turn behave as a complete system on chip (SoC) and has got tremendous use in mixed signal based applications. The main application fo this system is in the computational analysis of the various images captured from the real world. The author present a novel approach of implementing a smart system based on SoC design approach with required performance in the domain of mixed signal processing. The simulation of the system has been carried out on LabVIEW with optimum results desired. Some the result has been carried with mathematical modeling based approach using MatLAB software. The minimum S/N ratio of the system is 55 dB with 1920 X 1080 frame readout at 550 Hz.**

Keywords: CMOS sensor, HDTV, FPA, CCD, APS, SoC, LabVIEW, MatLAB, PID algorithm, MSP, CCD.

I. INTRODUCTION

The advent of the sensor dependent image processing technology has come into existence late back to 1970's with the use of MOS devices. The functioning of this system primarily depends on the utilization of array of image sensors which in turns rely on the proper functioning of the array of CCD technology so as to provide better and enhanced quality imaging arrays. With further advancement in this technology i.e. with the availability of CMOS based smart sensors, the analysis of the image becomes quite simple, cost effective, enhanced accuracy of the results. In this system, CMOS readouts with millions pixel capacity are used in addition to the detector arrays with the help of flip chip fabrication technology i.e. the most important feature of a SoC design based system.

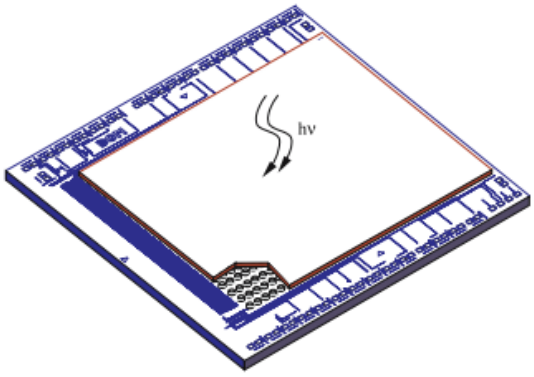

Fig. 1 Crossectional view of CMOS Image Sensing Device [1]

The above fig 1 shows the schematic arrangement i.e. crossectional view of the CMOS sensing system.The system on chip design based systems are normally follows the Moore's Law which utilized CMOS technology so as to produce higher performance sensors in various range of visibility. Due to this reason, CMOS technology without any doubt has now emerged the most common approach for the design of both infrared and visible range sensors that in turn finds enormous applications in the domain of MSP. Based on this features, it has been found that most of the mixed signal processing based industrial applications are still dependent on CMOS Image Sensors (CIS) technology as compared to CCD approach [2-8].

This smart CMOS based sensors requires to be designed and implemented using system on chip (SoC) design approach because most of the MSP based applications requires the portability features so that it can be utilized in remote areas. The basic requirement of this SoC design approach is embedded processors, memories and various hardware modules.In addition to this, this system requires the design flow of the functional executable model that meets the required specifications of the system from hardware and software prospective. The functional software module of the system can either be simulated on a transactional model of the hardware or it can be simulated on an Instruction Set Simulator (ISS). In case of this type of design flow approach, the system requires a programming tool that spans all the levels of the model i.e. a system specification language (UML). Although, this language meant for the specification, design, validation and documentation of the system, UML has been utilized to provide the complete model of the system. In addition to this, the SoC design approach requires System C or Embedded C as the system implementation language [9-16].

II. BASICS OF SoC DESIGN SYSTEM

Many of today's embedded systems are based on system-on-chip platforms, which,in turn, consist of one or more embedded microcontrollers, digital signal processors (DSP),application specific circuits and read-only memory, all integrated into a single package.These blocks are available from vendors of intellectual property (IP) as hard cores or softcores. A hard core, or hard IP block, is one where the circuit is available at alower level of abstraction such as the layout-level; it is impossible to customize ahard IP to suit the requirements of the embedded system. As a result, there are limitedopportunities in optimizing the cost functions by modifying the hard IP. For example, ifsome functionality included in the IP is not required in the present application, we cannotremove the function to save area. Soft IP refers to circuits which are available at a higherlevel of abstraction, such as register-transfer level. It is possible to customize thesoft IP for the specific application. The designer of an embedded SoC integrates the IPcores for processors, memories, and application-specific hardware to create the SoC.

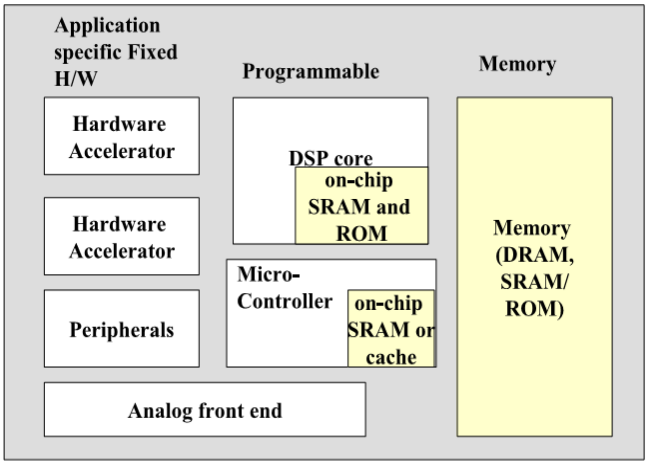

Fig. 2 Block diagram of an Embedded SoC System [17]

The above fig 2 illustrates the architecture of an embedded system-on-chip (SoC) which consists of basic four modules i.e.

- An Analog Front End which includes the analog/digital and digital/analog converters.
- Programmable Components which include microprocessors, microcontrollers, andDSPs. The number of embedded processors is increasing every year. An interestingstatistic shows that of the nine billion processors manufactured in 2005, less than 2%were used for general-purpose computers. The other 8.8 billion went into embeddedsystems. The microcontroller/microprocessor is useful in handling interrupts,house-keeping and performing timing related functions. The DSP is useful for processing the audio and video information e.g., compression and decompression ofaudio and video information. The application software is normally preloaded inthe memory and is not user programmable, unlike general-purpose processor-basedsystems.
- Application-specific components – these include hardware accelerators for computeintensive functions. Examples of hardware accelerators include digital image processors which are useful in cameras

The memory sub system of SoC consists of the following type i.e.

- On-chip memory organization
- Cache-based memory organization
- Scratch Pad Memory-based Organization

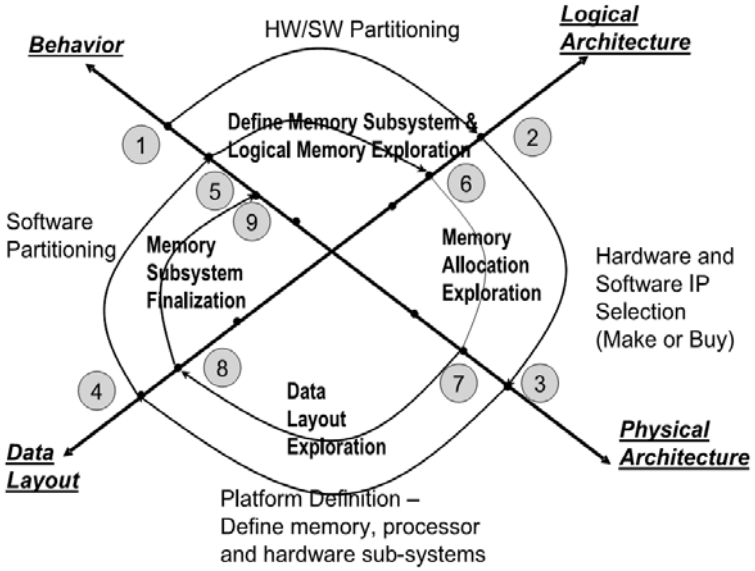

Fig. 3 Application Specific SoC Design Flow [18]

The design of an embedded system begins with a behavioral description as shown in above fig 3.In the present scenario, there are many languagesavailable to capture the system behavior, e.g., System Verilog, System C, and soon. The hardware-software partitioning is performed so as to identify which functionalities of thedescription are best performed in hardware and which are best implemented in software.Hardware implementation is cost-intensive, but improves the performance [19-25].

III. DESIGN & IMPLEMENTATION OF THE SoC BASED SMART CMOS PIXEL SENSOR ARRAY

The design and implementation approach of the proposed system is entirely dependent on the operational functionality of the various hard and soft modules with desired level of accuracy. For this same, UML 2.0 has been utilized along with the Embedded C to implement the system. In addition to this, author has also gone through the feasibility of the use of other programming and simulation tools that can be used to implement this system with enhanced level of the performance. Following steps are required to undergo so as to implement the simulation behavior of the system i.e.

- Define a UML profile for Embedded C
- Structural and behavioral features of the system
- Extended state diagram of the system
- Behavioral model with extended state machine diagram

These behavioral models of the system are conceived for code generation and modeling the operational performance with an isomorphicEmbedded C implementationapproach. The structural descriptionis completed by the composite structure diagrams that describe the connections of thesystem components and by the object diagrams that contain also the actual parametersof the objects. We provide a design environment where both the application and thearchitecture are described together in UML. EmbeddedC models the hardwarearchitecture within UML and provides the overall system simulation environment [26-30].

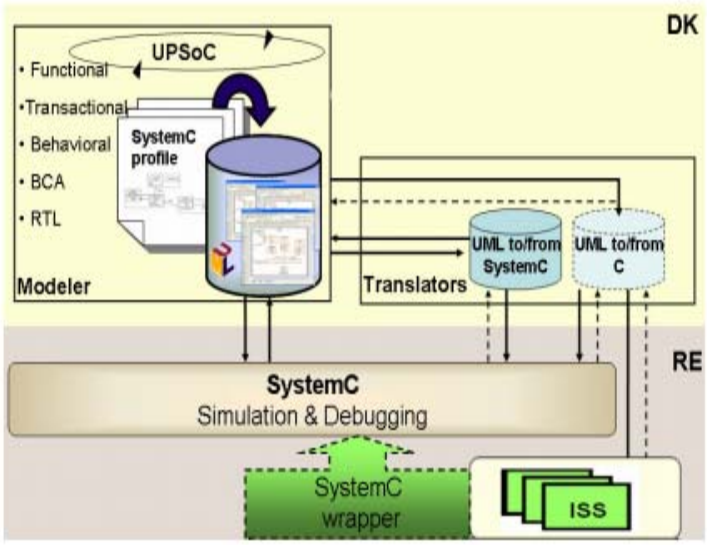

Fig. 4 Functional & Behavioral Model of the System [31]

The above fig 4 shows the design environment of the system. This approach of the design and implementation of the system is still under discussion with the development of the executable models. It can be categorized into two modules i.e. a development module or kit (DK) and a runtime environment module (RE).

In this design approach, the development module is further consists of UML 2.0 profile for Embedded C. In this approach of modeling the system are basically categorized in various sub modules which are further implemented as interfacing programs for RTOS environment. The UML profile of the system has been implemented with the use of Embedded C that elaborates the behavioral functionality of the smart system in terms of state diagram.

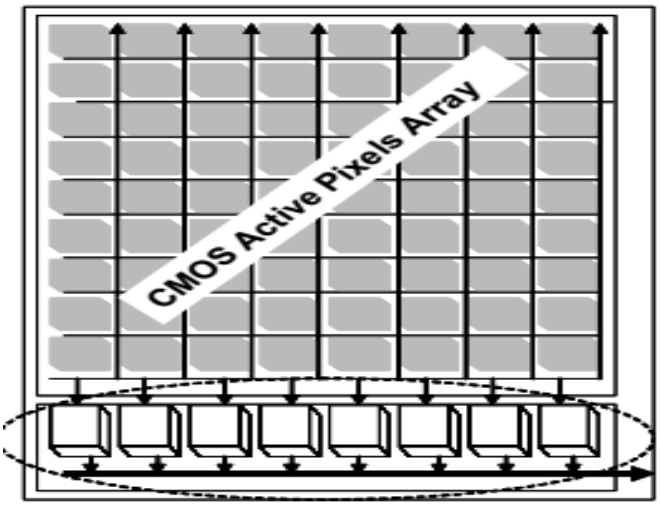

Fig. 5 Schematic diagram of CMOS pixels array [32]

The above fig 5 shows the schematic arrangement of the distribution of CMOS pixel array sensors. With this approach, we are interested in implementing the device with a technical aspects of image processing of the signal within a system on chip. Although, with SoC approach, the system has to compromise within various characteristics i.e. versatility, parallelism, processing speed and resolutions. The author has implemented the proposed system by keeping these limitations in mind and provides the mechanism with an overall increase in the system performance. It means that this smart system provides a high degree of parallelism and a balanced output within communication & computations.

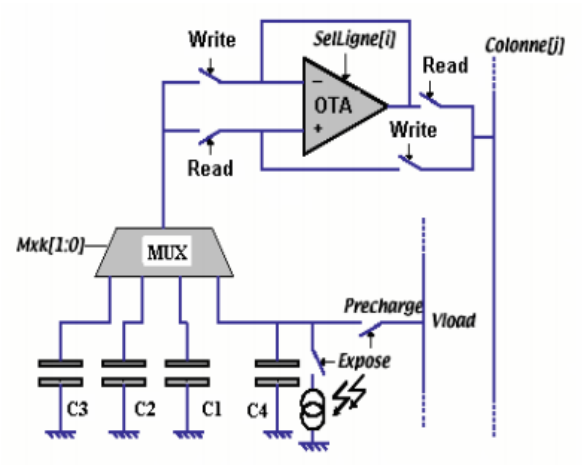

Fig. 6 Pixel Diagram of CMOS Sensor [33]

The above fig 6 shows the pixel diagram i.e. pixel area of the CMOS sensor array. This diagram depicts the storage capability of the system within the desired range i.e. 40 x 40 μm² and a fill factor of 9 %.

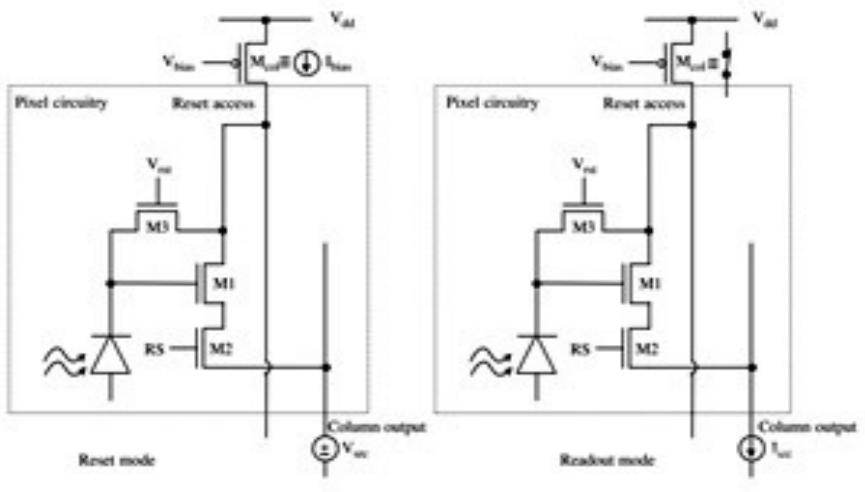

Fig. 7 CMOS based pixel array amplifier [34]

The above fig 7 shows the schematic arrangement of the designed model for the proposed smart system that has got tremendous utilization in mixed signal processing based applications. This model of the system provides an enhanced level of accuracy at the output with less amount of unwanted noise signal. The most effected parameter of this system is the channel resistance which in turn detoriates the overall performance of the system [35-46].

IV. SIMULATION RESULTS & DISCUSSION

The simulation work of the CMOS based smart pixel sensor circuit has been carried out with MatLAB software. The mathematical model of the system is first of all designed and then the various plots are obtained so as to undergo the analysis of the system. This simulation work can also be done with the help of either LabVIEW or pSpice software but the author has made the use of MatLAB 2014 version since its quite easily to model and analyze the performance of the system.

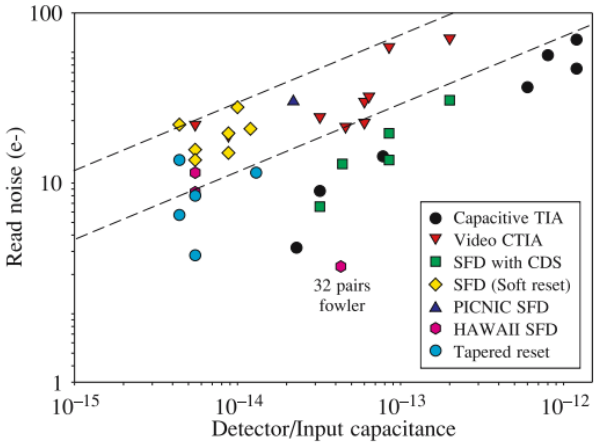

Fig 8: Noise Model Behavior of SoC Based CMOS Smart Image Sensors

The above fig 8 shows the simulated result of the noise model of the proposed circuit i.e. the behavior of the noise has been plotted with respect to the capacitance of the CMOS transistor. It means that this above figure conceptually shows the system-on-chip (SoC) architecture for the proposed CMOS active pixel sensor. The noise optimization has been achieved with the help of three CMOS transistors in the pixel array with active components available in the buffer location of the system.

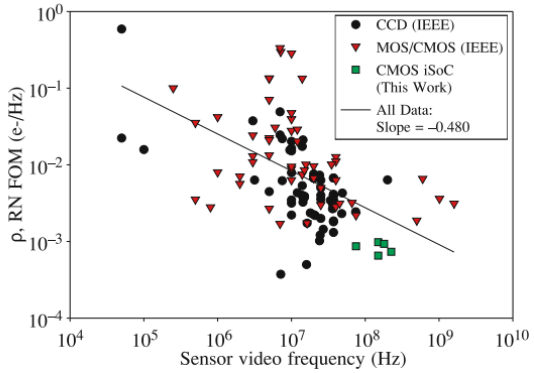

Fig 9: Normalized FoM of SoC Based CMOS Smart Image Sensors

The basic motive in analyzing the model of this system is to optimize the presence of the noise at the output. For this same reason, the noise parameter has been plotted with different dominant parameters of the system that determines the performance of the system.The distributed and pixel components work together to alternately constitute a source follower amplifierduring pixel readout. During pixel reset, the SoC embodiment transforms to a single-stage amplifier with feedbackcapacitor and reset switch having variable resistance. Thenumber of pixel transistors is minimized and thus opticalfill factor maximized. The distributed feedback amplifierresets each pixel using a tapered reset clock that is tailored by additional support circuits in the sensor periphery to extinguish reset noise and limit mode-switching noise.

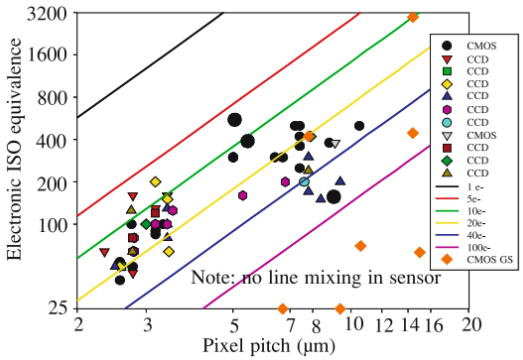

Fig 10: Speed Vs Pixel Pitch of SoC Based CMOS Smart Image Sensors

V. CONCLUSION

Table 1.1 Comparative Study Data

S.No.	SoC Reference Data	SoC Theoretical Data	Soc Obtained Data
1.	100	105	098.50
2.	150	145	148.00
3.	200	195	199.25
4.	250	245	249.00

The theoretical advantages of CMOS-based imagers havebeen validated on infrared and visible imaging sensors.While the read noise of competing CCD imagers has notimproved significantly over the last decade except whenthe video rate is lowered to rates unacceptable for newcameras, SoC CMOS now yields superior performance including lower read noise at comparable sensitivity.In this discussion, the author has reported a system-on-chip technique forsuppressing kTC noise that is used in a progressive image pixel sensors so as to generate 12-bit video with acceptable noise level and 2.2 V/lux-s sensitivity at 90 Hz frame rate. The minimum random noise at 18dB gain is 8e-, independent of video frequency, using a SoCdistributed amplifier to minimize noise. The SoCbased approach provides a way to circumvent physicallimitations inherent in high resolution sensors having smallpixel pitch by significantly reducing random noise below the desired level.

VI. ACKNOWLEDGEMENT

The authors are thankful to Hon'able C – VI, Mr. AseemChauhan (Additional President, RBEF and Chancellor AUR, Jaipur), Maj. General K. K. Ohri (AVSM, Retd.) Pro-VC Amity University, Uttar Pradesh Lucknow, Wg. Cdr. Dr. Anil Kumar, Retd.(Director, ASET), Prof. S. T. H. Abidi (Professor Emeritus), Brig. U. K. Chopra, Retd.(Director AIIT), Prof. H K Dwivedi (Director, ASAP), Prof O. P. Singh (HOD, Electrical & Electronics Engg.) and Prof. N. Ram (Dy. Director ASET) for their motivation, kind cooperation, and suggestions.

REFERENCES

[1] E. Riccobene, P. Scandurra, A. Rosti and S. Bocchio. A UML 2.0 Profile for SystemC. STMicroelectronics Technical Report, 2004.
[2] E. Riccobene, P. Scandurra, A. Rosti, S. Bocchio. A SoC Design Methodology Based on aUML 2.0 Profiles for SystemC. In DATE 05.
[3] E. Riccobene, P. Scandurra. ModellingSystemC Process Behavior by the UML MethodState Machines. In RISE 04, Springer-Verlag 2004.
[4] P.-A. Muller, P. Studer, F. Fondement, and J. Bézivin. Platform independentWebApplication Modeling and Development with Netsilon. Journal SoSym, 2005
[5] P. Dudek, J. Hicks, "A CMOS General-Purpose Sampled-Data Analogue Microprocessor". Proc. of the 2000 IEEE InternationalSymposium on Circuits and Systems. Geneva, Suisse.
[6] Y. Ni, J.H. Guan, "A 256x256-pixel Smart CMOS Image Sensor for Linebased Stereo Vision Applications", IEEE, J. of Solid State Circuits, Vol.35 No. 7, Juillet 2000, pp. 1055-1061.
[7] A. Elouardi, S. Bouaziz, R. Reynaud, "Evaluation of an artificial CMOSretina sensor for tracking systems". Proceeding of IEEE IntelligentVehicles Symposium 2002, Versailles, France.
[8] A. Dupret, J.O. Klein, A. Nshare "A DSP-like Analog Processing Unitfor Smart Image Sensors", International Journal of Circuit Theory andApplications 2002. 30: p. 595-609.
[9] A. Dupret, E. Belhaire, J.C Rodier "A high current large bandwidthphotosensor on standard CMOS Process" presented at EuroOpto'96,AFPAEC, Berlin, 1996.
[10] D. Litwiller "CCD vs. CMOS: Facts and Fiction". The January 2001issue of PHOTONICS SPECTRA, Laurin Publishing Co. Inc.
[11] R. Deriche, "Fast algorithms for low level-vision".IEEE Transaction ofPattern Analysis and Machine Intelligence, vol 12-1, 1990.
[12] F. Garcia Lorca, L. Kessal, D. Demigny "Efficient ASIC and FPGAimplementation of IIR filters for real time edge detections", Proc.International Conference on Image Processing, IEEE ICIP 1997.
[13] A. Dupret, J.O Klein, A. Nshare, "A programmable vision chip for CNNbased algorithms". CNNA 2000, Catania, Italy: IEEE 00TH8509.
[14] A. Elouardi, S. Bouaziz, A. Dupret, J.O Klein, R. Reynaud, "On ChipVision System Architecture Using a CMOS Retina". Proceeding of IEEEIntelligent Vehicle Symposium, IV'04. Pages 206-211. ISBN 0-7803-8311-7. June 14-17, 2004. Parma, Italy.
[15] Drumea, Al. Vasile, P. Svasta, M. Blejan, System on Chip Signal Conditioner for LVDT Sensors, 1st Electronics SystemintegrationTechnology Conference ESTC06, Dresden, Germany, September 2006, pp. 629-633.
[16] Drumea, Al. Vasile, P. Svasta, I. Ilie System on Chip Signal Conditioner for LVDT Sensors, 2nd Electronics SystemintegrationTechnology Conference ESTC08, September 2008
[17] W. Guimei,et al., "Mine Pump Comprehensive Performance Testing System Based on Labview," In Measuring Technology andMechatronics Automation 2009.ICMTMA'09,International Conference on 2009,pp.300-303
[18] G. Beitao, et al., "Application of LabVIEW for Hydraulic Automatic Test System," in Industrial and Information Systems, 2009.IIS'09.International Conference on,2009,pp.348-351
[19] Embedded control handbook - Volume 1, MicrochipInc., 1997.
[20] K. Astrom, B. Wittenmark, Computer – Controlled Systems. Theory and Design, 3rd Edition,Prentice Hall ,1997,pp.324-369.
[21] L. Bierl, Das grosse MSP430 Praxis Buch, Franzis, 2004, pp. 110-190.
[22] J. Travis and J. Kring, "LabVIEW for Everyone: GraphicalProgramming Made Easy and Fun," 2006.
[23] National Instrument's PID Control Toolset User Manual.
[24] Active pixel sensors: Are CCD dinosaurs? ER Fossum IS&T/SPIE's Symposium on Electronic Imaging: Science andTechnology, 2-14A.
[25] http://www.vision-systems.com/articles/2015/03/sony-rumored-to-discontinue-production-of-ccd-sensors.html

[26] CCD vs. CMOS, Dave Litwiller, Photonics Spectra, 2001
[27] Determination of the optimal electrical bandwidth in CCD- and CMOS-based image detector applications, Robert H.Philbrick, SPIE 5499, Optical and Infrared Detectors for Astronomy, 2004
[28] CMOS vs. CCD: Changing Technology to Suit HDTV Broadcast, Lester J. Kozlowski, 2003
[29] Fundamental performance differences between CMOS and CCD imagers: Part 1, James Janesick et al., SPIE 6276, High Energy, Optical, and Infrared Detectors for Astronomy II, 62760M, 2006
[30] A 0.7 e-rms Temporal Readout Noise CMOS Image Sensor for Low Light Level Imaging, Y. Chen et al., IEEE International Solid-State Circuits Conference (ISSCC), 2012.
[31] http://www.caeleste.com/caeleste_publications/2011CNES/20111207_CNES_caeleste_presentation.pdf
[32] L²CMOS Image Sensor for Low Light Vision, Pierre Fereyre et al., International Image Sensor Workshop, 2011
[33] Night Vision CMOS Image Sensors Pixel for SubmilliLux Light Conditions Amos Fenigstein, International Image SensorWorkshop, 2015
[34] A Review of the Pinned Photodiode for CCD and CMOS Image Sensors Eric R. Fossum, et al., IEEE Journal Of TheElectron Devices Society, Vol. 2, no. 3, may 2014
[35] No image lag photodiode structure in the interline CCD image sensor, N Teranishi et al., Electron Devices Meeting,1982 International (Volume:28), 1982
[36] http://www.sony.net/Products/SC-ZP/new_pro/may_2014/icx825_e.html
[37] A 3D stacked CMOS image sensor with 16Mpixel global-shutter mode and 2Mpixel 10000fps mode using 4 millioninterconnections, Symposium on VLSI Circuits (VLSI Circuits), T. Kondo et al., pages C90 - C91, 2015
[38] M. S. Robbins and B. J. Hadwen, "The noise performance of electron multiplying charge-coupled devices," IEEETransactions on Electron Devices, vol. 50, no. 5, pp. 1227–1232, May 2003
[39] Electron Multiplying Device Made on a 180 nm Standard CMOS Imaging Technology, Pierre Fereyre et al.,International Image Sensor Workshop, June 2015
[40] First Measurements of True Charge Transfer TDI (Time Delay Integration) Using a Standard CMOS Technology, F.Mayer et al., International Conference on Space Optics, 2012
[41] CMOS long linear array for space application G. Lepage, Proc. SPIE 6068, Sensors, Cameras, and Systems forScientific/Industrial Applications VII, 606807, 2006)
[42] Time-Delay-Integration Architectures in CMOS Image Sensors G. Lepage et al., IEEE Transactions On Electron Devices,vol. 56, no. 11, November 2009
[43] R. Shimizu and Al., "A Charge-Multiplication CMOS Image Sensor Suitable for Low-Light-Level Imaging" IEEE Journalof Solid-State Circuits, vol. 44, no. 12, pp. 3603-3608 December 2009
[44] The lock-in CCD-two-dimensional synchronous detection oflight, T. Spirig, P. Seitz et al., IEEE Journal of QuantumElectronics, Vol. 31, Iss. 9, p. 1705 – 1708, Sep 1995
[45] Demodulation pixels in CCD and CMOS technologies for time-of-flight ranging Robert Lange et al., Proc. SPIE 3965,Sensors and Camera Systems for Scientific, Industrial, and Digital Photography Applications, 177 (May 15, 2000)
[46] 320x240 Oversampled Digital Single Photon Counting Image Sensor N. AW. Dutton, VLSI Circuits Digest of TechnicalPapers, 2014

AUTHOR PROFILE

Mr. RajinderTiwari, PhD (P), M.Tech,MIETE is a member of academic staff of Department of Electronics & Electrical Engineering (ASET), Amity University Uttar Pradesh, Lucknow, where he is serving in the capacity of Asstt. Professor in the Department of Electronics Engineering (ASET). He has done M.Tech (I&CE) and M.Sc (Electronics) from NIT, Kurukshetra and University of Jammu, respectively. Presently, he is pursuing Ph.D. (ECE) from Department of Electronics Engineering, Kumaon Engineering College, Dawarahat (Almora) under Uttarakhand Technical University. Mr. Tiwari has given his contribution to the area of Microelectronics (Modeling & Simulation of the Analog CMOS Circuits for ASP Applications), Embedded System Design, Digital System Design and Process Industries Automation and Control System Design (using Graphical Programming Language with dedicated Hardware). He has published several research papers in International/National Journals/Seminar/Conference. He is associated with several technical institutions and bodies as a life member. Before taking the assignment of Amity University, Uttar Pradesh, Lucknow, he had worked in Electronics for Societal Group, CEERI, Pilani, as a Project Scientist and a Multi – National Company as a Sr. Software Engineer (Bridge Instrumentation Division). He is also associated with the successfully implementation of the Hardware and Software for number of projects undertaken by him and in organizing number of International/National Conferences and Seminars.