SSTL Based Energy Efficient FIFO Design for High Performance Processor of Portable Devices

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***Abstract*— Now days green computing is major research area in the computer science field, where we want to reduce the total power consumption of our device by applying different techniques .Having this concern we have designed our FIFO (First In First Out) circuit and calculated its total power dissipation at different-different families of SSTL with frequency scaling techniques. In this technique we used following (20 GHz, 40GHz, 60 GHz and 80 GHz) frequency range. In our work first we have worked with SSTL12 and found that when we scaled down the frequency from 80 GHz to 20 GHz 71.55% reduction in total IO power. In second we have worked with SSTL15 and got 74.02% of reduction in total IO power when we reduced frequency from 80 GHz to 20 GHz. In last we worked with SSTL18_I and SSTL18_II and found 74.29% and 74.28% of reduction in total power respectively, when we scaled down the frequency from 80 GHz to 20 GHz. We have designed our FIFO on 28 nm kintex-7 FPGA family**

Keyword- SSTL IO standard, Low Power, Energy Efficient, 28 nm FPGA, FIFO

I. INTRODUCTION

FIFO abbreviates first in first out which is a kind of data structure to manage/organize and manipulate data or entries where the oldest entry will be accessed or processed first. In other words the entries will get preference in the order as they came.

In data structure, this concept gets implemented as queue. The insertion, deletion or other operations get performed on the head or oldest data entry. As a CPU scheduling Algorithm, In First Come First Serve Algorithm FIFO get used in which CPU becomes available to those processes first which came first on the other hand FIFO disk scheduling also get used on this concept.

Through FIFO, we get a fair processing and complexity level reduces to serve the processes but sometime this approach becomes inefficient (or time taking). As if the newest entry's process is very short and will take negligible amount of time comparatively then it have to wait for long time till the oldest one completes, then somehow efficiency of work get affected. Overall, this approach is too good if everything have to be done in sequential manner.

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Figure:1 Top Level of Schematic of FIFO

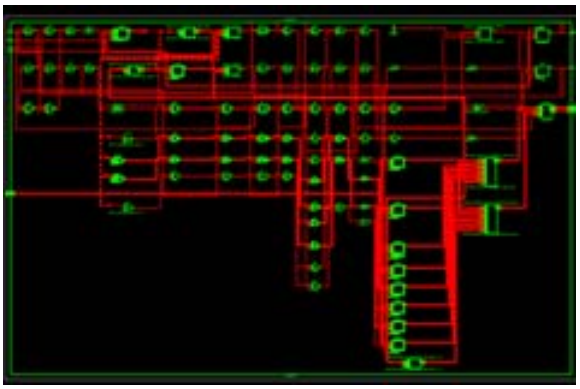

Figure:2 RTL Schematic of FIFO

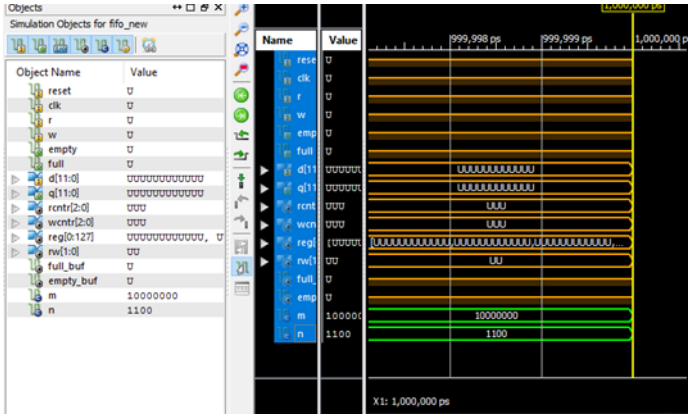

Figure:3 Behavioural Model of FIFO

II. Related Work

High performance FIFO design for processor through voltage scaling technique [1]. Stub series terminated logic (sstl) is an input/output standards for driving transmission lines commonly used with dram based ddr memory [2]. Sstl i/o standards used not only in energy efficient arithmetic logic unit (alu) [3] but also in fire sensor [4], parallel integrator [5], analog-to-digital converter [6], image alu [7], read only memory (rom) [8]. Sstl is one of the common used i/o buffer architecture for programmable devices [9]. Hstl io standards based processor specific green counter[10]. Leakage power reduction with various io standards and dynamic voltage scaling in vedic multiplier on virtex-6 fpga[11]. Capacitance scaling based low power comparator design on 28nm fpga[12].

III. Power Analysis

We have designed our FIFO on 28nm FPGA Kintex-7 family through VHDL language. For the power analysis we have used the Xpower analyzer tool in Xilnix software.

Table 1: Power Consumption with SSTL12

	Clock	Logic	Signal	IOs
20 GHz	0.167	0.055	0.195	0.473
40 GHz	0.334	0.080	0.370	0.869
60 GHz	0.501	0.105	0.545	1.266
80 GHz	0.668	0.130	0.720	1.663

In table 1 we have worked with SSTL12 IO standards where we have scaled down the frequency from 80 GHz to 20 GHz and found 71.55% of reduction in total power consumption. We have also convert this data through the bar chart as shown in figure 4.

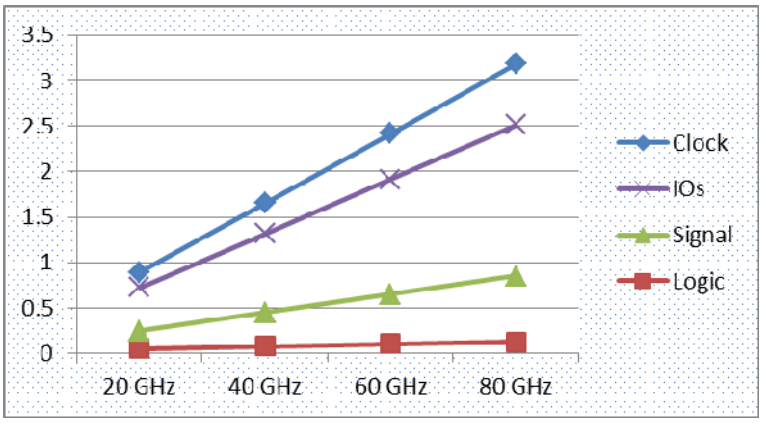

Figure: 4 Power analysis at SSTL12

Table 2: Power Consumption with SSTL15

	Clock	Logic	Signal	IOs
20 GHz	0.225	0.057	0.157	1.217
40 GHz	0.450	0.085	0.303	2.373
60 GHz	0.676	0.111	0.436	3.529
80 GHz	0.904	0.133	0.597	4.685

In table 2 we have worked with SSTL15 IO standards where we have scaled down the frequency from 80 GHz to 20 GHz and found 74.02% of reduction in total power consumption. We have also convert this data through the bar chart as shown in figure 5.

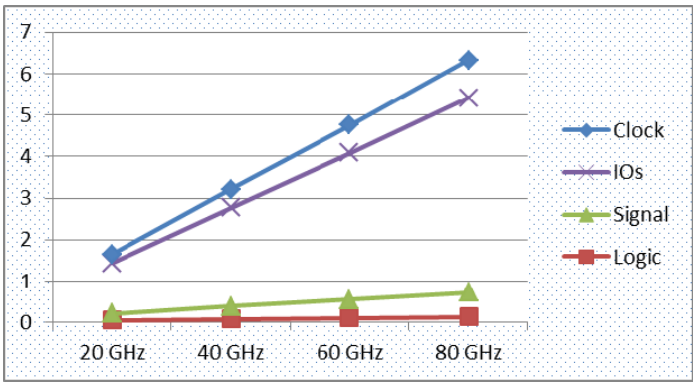

Figure: 5 Power analysis with SSTL15

Table 3: Power Consumption with SSTL18_I

	Clock	Logic	Signal	IOs
20	0.225	0.057	0.157	1.989
40	0.450	0.085	0.303	3.905
60	0.676	0.111	0.436	5.821
80	0.904	0.133	0.597	7.737

In table 3 we have worked with SSTL18_I IO standards where we have scaled down the frequency from 80 GHz to 20 GHz and found 74.29% of reduction in total power consumption. We have also convert this data through bar chart as shown in figure 6.

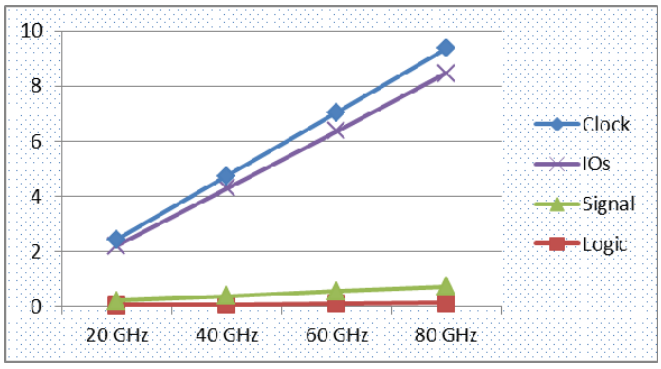

Figure: 6 Power analysis with SSTL18_I

Table 4: Power Consumption with SSTL18_II

	Clock	Logic	Signal	IOs
20	0.225	0.057	0.157	2.358
40	0.450	0.085	0.303	4.628
60	0.676	0.111	0.436	6.898
80	0.904	0.133	0.597	9.168

In table 4 we have worked with SSTL18_II IO standards where we have scaled down the frequency from 80 GHz to 20 GHz and found 74.28% of reduction in total power consumption. We have also convert this data through bar chart as shown in figure 7.

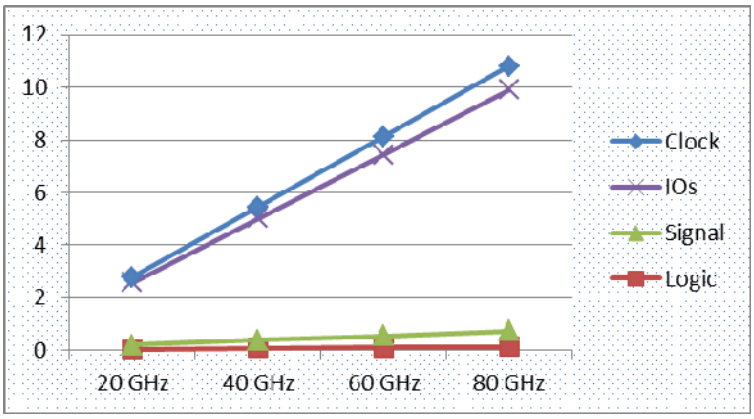

Figure: 7 Power analysis with SSTL18_II

IV.Conclusion:

In this work we have worked with different-different SSTL IO standard family and calculated total IO power through frequency scaling techniques, in frequency scaling techniques we have used (20 GHz,40 GHz,60 GHz,80 GHz)frequency ranged. With SSTL12 we found 71.55%, with SSTL15 we got 74.02%, with SSTL18_I we got 74.29% and with SSTL18_II we got 74.28% reduction in total power consumption. In last we found that SSTL12 IO standard is suitable for our FIFO design.

V. Future Scope:

In this work, FIFO Design is implemented on 28nm on Kintex-7 FPGA family, but we have scope to redesign our FIFO with different FPGA family like Virtex 7,Virtex 6, Virtex 5 or we can also apply different- different techniques for calculating total power consumption.

VI. References

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