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Design of Energy Efficient Dual Spacer Delay Insensitive Ripple Carry Adder with better Slew Rate

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Abstract:- **The main goal of this paper is to provide the low power solutions for Very Large Scale Integration (VLSI). Design of low power and area efficient logic systems forms an integral part in the field of VLSI design. The addition is the most fundamental part in the arithmetic operations. To perform fast arithmetic operation, Ripple carry adder (RCA) is one of the fastest adder used in many data processing applications. Various Delay Insensitive techniques are available for designing low power applications. In this paper, the features of Multi-threshold Null Convention Logic (MTNCL) are discussed and we implement Ripple Carry Adder using proposed Multi-threshold Dual-Spacer Dual-Rail Delay-Insensitive Logic (MTD^{3}L). Proposed and existing techniques are compared in terms of various performance metrics like power, delay, energy and slew rate.**

Keywords:- Ripple carry adder, arithmetic, half adder, full adder, low power, Dual- Rail CMOS logics.

I. INTRODUCTION

In early 1970's, the major challenges for the VLSI designer is to provide the high speed operation and with minimum area. The design tools were all concentrated on these two parameters. In the present scenario, power dissipation and delay are focused by the VLSI designer [1, 2, 3]. The best performance or metric levels of power- delay product provides in asynchronous (clock-less) design. So, ripple carry adder was implemented in various asynchronous designs.

An adder is basically a circuit used in digital arithmetic to add two N bit numbers which can be designed with the help of asynchronous techniques (single bit dual rail) [3]. Mostly asynchronous design is used because it provides low power consumption, low Electro-Magnetic Interference (EMI) and high robustness compared to the synchronous (clocked) design. This paper deals with two asynchronous techniques which are Multi-threshold Null Convention Logic (MTNCL) [4] and proposed Multi-threshold Dual rail Dual spacer Delay insensitive Logic (MTD^{3}L).

The basic components to design the ripple carry adder are half adder and full adder.

A. Basic Half adder

A half adder is essentially used for addition purpose and consist two inputs (A_n, B_n) where A_n and B_n are the n^{th} order bits of the numbers A and B respectively and it provides two outputs Sum (S), carry (C) as shown in figure.1. The table.1 represents the truth table for Half adder [6].

$$\text{Sum} = \overline{A}.B + A.\overline{B}, \text{Carry} = AB$$

Table 1. Truth table for Half Adder

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

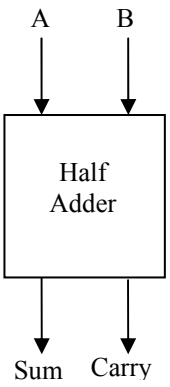

Fig.1 Basic block diagram of Half adder

B. Basic Full adder

A full adder is basically used for adding and consist three inputs (A_n, B_n, C_{n-1}) where A_n and B_n are the n^{th} order bits of the numbers A and B respectively and Cn-1(C_{in}) is the carry generated from the addition of $(n-1)^{th}$ order bits and provides Sum (S), Carry Out (C_{out}) as shown in figure.2. The table.2 represents the truth table for full adder [6,7].

$$Sum = A \oplus B \oplus C$$
$$Carry = AB+BC+CA$$

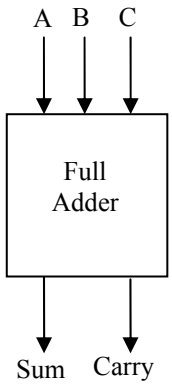

Fig.2 Basic block diagram of Full adder

Table 2. Truth table for Full adder

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

This paper is organized as follows: In section 2, implementation of Half adder and Full adder in asynchronous techniques. Section 3, explains about ripple carry adder and design in asynchronous techniques. Section 4 deals with a few applications of design and results are evaluated in section 5 and section 6 concludes.

II. DESIGN OF ASYNCHRONOUS CIRCUITS

The Asynchronous (self-timed circuits) techniques are Multi-threshold Null Convnetion Logic (MTNCL) and proposed Multi-threshold Dual rail Dual spacer Delay insensitive Logic (MTD^3L) [9]. The Half adder and Full adder were implemented with some threshold gates of 27 Fundamental threshold gates. In this self- timed circuits, each single bit as a dual rail**.** Consider Half adder and full ADDER implementation in clock-less circuits [5,13].

A. Half adder:

A half adder consists 2 inputs (A, B) and 2 outputs (Sum, Carry), each single input and output acts as a dual rail (A_0, A_1, B_0, B_1, Sum_0, Sum_1, $Carry_0$, $Carry_1$) as shown in figure.3 and table.3 represents the truth table of Half adder in dual rail. To design the half adder in clock-less circuit, four different threshold gates are required which are TH_{22}, TH_{12}, TH_{23W2}, TH_{33W2} out of 27 fundamental gates[10].

Table 3. The truth table for Dual rail Half adder

A		B		SUM		CARRY	
A_0	A_1	B_0	B_1	S_0	S_1	$Cout_0$	$Cout_1$
1	0	1	0	1	0	1	0
1	0	0	1	0	1	1	0
0	1	1	0	0	1	1	0
0	1	0	1	1	0	0	1

B. Full adder

A Full adder consists of 3 inputs (A, B, C) and 2 outputs (Sum, Carry) as shown in Figure.4 and table.4 represents the truth table of full adder in dual rail [8,10]. Each single input and output acts as a dual rail (A_0, A_1, B_0, B_1, C_0, C_1, S_0, S_1, $Cout_0$, $Cout_1$). To design the full adder in self- timed circuit, two different threshold gates are required which are TH_{23}, TH_{34W2} out of 27 fundamental gates.

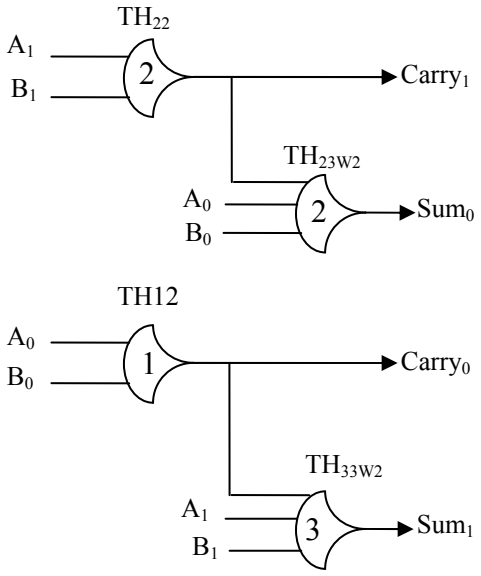

Fig.3 Design of Dual rail Half adder

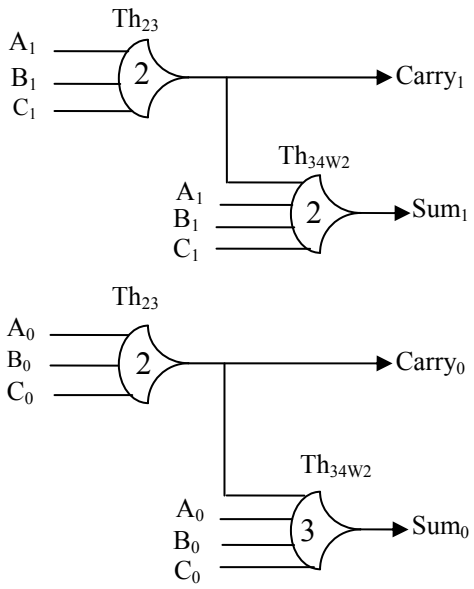

Fig.4 Design of Dual rail Full adder

Table 4. Truth table for Dual rail Full adder

A		B		C		SUM		CARRY	
A_0	A_1	B_0	B_1	C_0	C_1	S_0	S_1	$Cout_0$	$Cout_1$
1	0	1	0	1	0	1	0	1	0
1	0	1	0	0	1	0	1	1	0
1	0	0	1	1	0	0	1	1	0
1	0	0	1	0	1	1	0	0	1
0	1	1	0	1	0	0	1	1	0
0	1	1	0	0	1	1	0	0	1
0	1	0	1	1	0	1	0	0	1
0	1	0	1	0	1	0	1	0	1

C. Multi-threshold Null Convention Logic (MTNCL)

The basic Null Convention Logic consists of SET, RESET blocks for circuit operation and $Hold_0$, $Hold_1$ blocks for state holding capacity[14]. While applying the multi-threshold to NCL logic, the circuit area and power consumption will be reduced i.e., transistor count is decreased. For MTNCL, only $Hold_0$ and SET blocks [15] are required and additionally few high threshold voltage transistors (V_{th}) are used to reduce the leakage problem as shown in figure.5 [19].

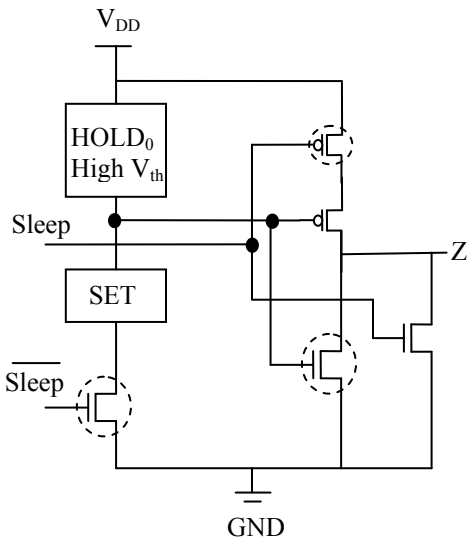

Fig.5 Block diagram of MTNCL

III. PROPOSED MULTI-THRESHOLD DUAL-SPACER DUAL-RAIL DELAY-INSENSITIVE LOGIC (MTD^{3}L) - RIPPLE CARRY ADDER

The block diagram of MTD^{3}L is similar to MTNCL logic, but two sleep signals (sleep0, Sleep1) are required in this logic as shown in figure.6 [14]. The circuit will operate with respect to the input signal, when two sleep signals are transitioned to 0 as shown in table.5. If sleep 1 signal is asserted, then all one spacer is obtained as the output. If sleep0 is asserted, then all zero spacer is obtained as the output[15,20].

Table 5. MTD^{3}L Sleep signals

Sleep		Output
S0	S1	
0	0	Normal operation
0	1	All-One Spacer
1	0	All-Zero Spacer
1	1	Invalid

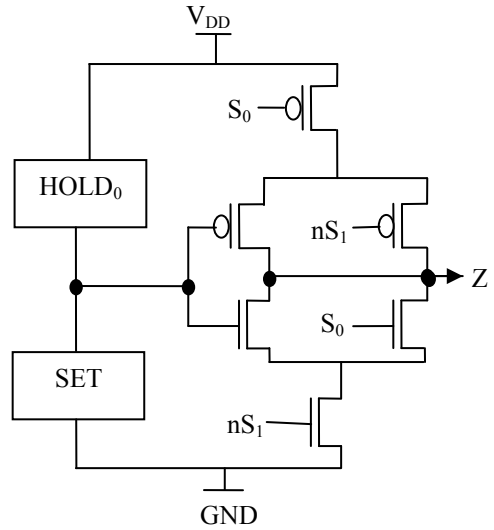

Fig.6 Block diagram of MTD^{3}L

Ripple carry adder is constructed by cascading full adder block in the series or it can be constructed by merging half adder and full adder blocks. This paper deals with the combination of full adder and half adder block in series for 8- bit ripple carry adder circuit with multiple full adders and half adder can be used to add N numbers and each full adder inputs a C_{in}, which is the C_{out} of the previous full adder. Such kind of adder is known as Ripple carry adder, since each carry bit ripples to the next full adder as shown in figure.7. So ripple carry adder in digital electronics is that circuit which produces the arithmetic sum of two binary numbers [12]. The input bits of 'X' are added to the input bits of 'Y', respectfully of their binary position. Each bit addition creates a sum and a carry out. The carry out is then transmitted to the carry in of the next higher order bits. The final result creates a sum of N bits plus a carry out [16,18].

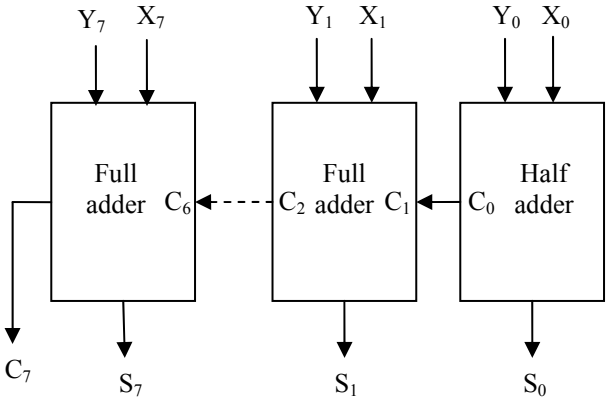

Fig.7 Design of 8- bit Ripple carry adder

The 8- bit ripple carry adder was implemented in two asynchronous circuits (MTNCL and MTD^{3}L logics) as shown in figure 8 and 9.

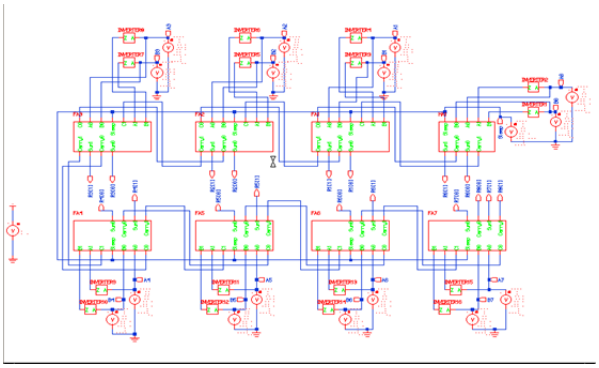

Fig.8 Schematic of Ripple carry adder using MTNCL Logic

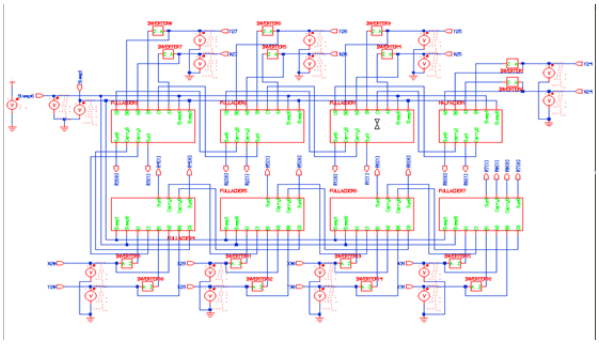

Fig.9 Schematic of Ripple carry adder using MTD^{3}L Logic

In many computers and other kind of processors, adders are not only used in the arithmetic logic unit, but also in other parts of the processor, where they are used to calculate addresses, table indices and similar applications [11]. Some other applications of adders are in Multiply–Accumulate (MAC) structures, Arithmetic

Logic Unit (ALU). Adders are also used in multipliers, in high speed integrated circuits and Digital signal processing (DSP) to execute various algorithms like FFT, IIR and FIR [17].

IV. SIMULATION RESULTS

This work has been developed with Mentor Graphics tools with 130nm technology. The simulation results (output waveforms of a single rail) of the ripple carry adder using the two asynchronous techniques (MTNCL and MTD^{3}L) as shown in figure 10 and 11. Table.6 shows the comparison of two asynchronous techniques (MTNCL, MTD^{3}L). The parameters which compared on power dissipation, delay, energy and slew rate.

A.Power Dissipation

Power dissipation is one of the main criteria which, considered in the VLSI design. As power dissipation (heat) is reduced, the output waveforms will obtained accurately without any glitches. Average dissipated power for ripple carry adder in two self-timed logics are tabulated in 6.

$$\text{Pavg} = \text{Pstatic} + \text{Pdynamic}$$

Where Pavg is the total average power, Pstatic is the static power dissipation,Pdynamic is the dynamic power dissipation of the circuit.

B.Propagation delay

Propagation delay or Gate delay is the time required for a digital signal to transit from the input voltage of a logic gate to the output voltage. Delay must be reduced to obtain the circuit performance accurately (high speed) and glitches will extract. It is given by

$$\text{Tpd} = \frac{\text{Tphl} + \text{Tplh}}{2}$$

C. Power Delay Product

Power Delay Product (PDP) is the measure of energy and is defined by the product of power and delay to measure the circuit performance. It is measured in Joule. The advantage of increasing the energy is short circuit dissipation (leakages) is minimized. It is given by

$$\text{PDP} = \text{P(Power)} \text{ x } \text{T(delay)}$$

Where P is the average power and T is the propagation delay or gate delay.

D. Slew Rate

Slew rate is defined as the rate of change of voltage per unit time. The unit of measurement is Volts/Sec.

$$\text{SR} \geq 2\pi \text{fVpk}$$

Where f is the frequency ($\frac{1}{T}$) and Vpk is the peak amplitude of the waveform. The high slew rate gives quicker response, i.e., changes the state of the output with respect to the input, especially at high frequencies as shown in waveforms and tabular form 6.

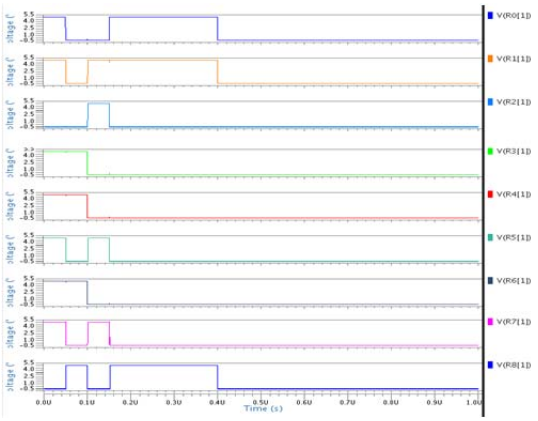

Fig.10 Schematic results of Ripple carry adder using MTNCL Logic

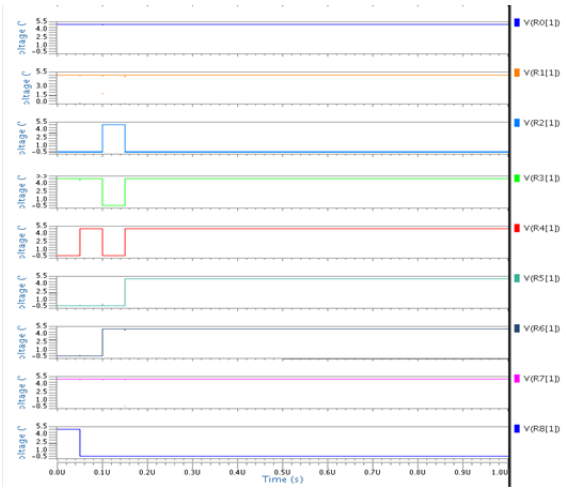

Fig.11 Schematic results of Ripple carry adder using MTD^{3}L Logic

Table 6. Comparison of delay and power for two asynchronous circuits

Parameters	MTNCL	Proposed MTD^{3}L
Power dissipation (nWatts)	202.69	857.17
Delay (nSec)	299.88	0.175
Energy (p Joule)	60.78	1.505
Slew Rate (G Volt/Sec)	12.92	65.90

V. CONCLUSION & FUTURE SCOPE

The ripple carry adder is designed using two CMOS asynchronous techniques. Proposed MTD^{3}L gives better performance interms of delay, % of energy savings and slew rate. With proposed method we achieved 97.5% energy savings. The ripple carry adder design may further optimized in terms of all these performance metrics by using Return To One Protocol and leakage reduction technique like LECTOR algorithm.

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