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Full Custom Layout Optimization Using Minimum distance rule, Jogs and Depletion sharing

Umadevi.S[#1], Vigneswaran.T[#2]
[#] Assistant Professor [Sr], School of Electronics Engineering,
VIT University, Vandalur- Kelambakkam Road, Chennai, India.
umadevi.s@vit.ac.in
[#] Professor, School of Electronics Engineering,
VIT University, Vandalur- Kelambakkam Road, Chennai, India
vigneswaran.t@vit.ac.in

***Abstract* – Layout design of an Integrated Circuit (IC) is the representation of IC in terms of geometric shapes which corresponds to the pattern of metal, polysilicon, oxide and semiconductor layers that constitutes the components of IC. Layout optimization plays a key role in producing an IC with less inter connect delay, parasitic effect, signal integrity issues and power dissipation etc. This research work proposes the methodology through which unwanted white space present in the layout has been minimized which tends to reduces the total area of the layout. The proposed methodology has been checked by designing the single ended differential amplifier as an example circuitry and by using Cadence® virtuoso® 64 tool. The proposed methodology reduces the layout area by applying three methods together and the methods applied are i) working towards minimum distance rule ii) introducing jogs and iii) depletion sharing. After using above mentioned methodologies together in Single ended differential amplifier, the total area of the layout has been reduced to 77.81% when compared to original schematic driven layout of the same.**

Keywords: Layout area, Depletion sharing, Differential amplifier, Jogs, Layout optimization.

I. INTRODUCTION

Application Specific Integrated Circuit (ASIC) design flow is a sequence that specifies step by step procedure to complete a specified task and to design a chip. It specifies how to convert the decided idea into a chip. Fig 1 shows the basic steps in ASIC design flow.

The first step of ASIC design flow is to define the functionality and specifications that is required for the chip. It includes performance figures like power, speed, accuracy etc. Each chip consists of different functional blocks that perform a particular task. The architecture denotes where to place each blocks, what should be the size of each blocks what is the relationship between them. The aim of physical design step is to design a circuit that performs all the desired operation. The circuit representation is then converted into a geometric representation, which is layout. Layout data is converted into photolithographic masks during fabrication process and finally each chip is packaged and tested.

In the IC design process, layout optimization is one of the important criterions. It becomes the bottleneck in determining the performance of the Integrated Circuit. The rapidly improving design complexity and the demand for the capability of handling, introduce challenges in Layout improvement.

The critical area reduction and white space allocation in congested regions are some methods to improve the layout aspect ratio without compromising much. Critical area is the region of chip where the chance of occurrence of errors and defects are more [8]. Powerful and robust routers can effectively reduce critical area and wirelength [4], [3], [1].

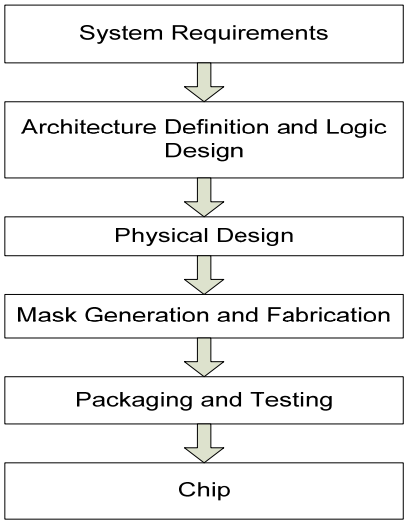

Fig. 1: ASIC Flow

Even though the techniques such as recursive top down partitioning, iterative refinement, embedded multi-level optimizations, path-based algorithms and routability optimization are leading to better placement [5], those existing placement solutions are far from optimal. Repartitioning [6] methods proposed by introducing placement feedback controllers improve partitioning result. Improved mincut bisection leads to better placement and less congestion which enhances the quality of the layout in post layout stage. Congestion driven white space allocation algorithms have been proposed [2] [3], which has been applied after placement stage and which results in better routability and reduced wirelength without worsen the original placement.

Layout modification tools [1] with practical extraction and reporting language (Perl) enables complex layout modification algorithms to be built with Perl features. Layout of an IC can be made more robust by applying minor modifications which includes [9] [10] adding extra Via's, thickening wires and moving wires.

This research work presents a new methodology to minimize the unwanted white space present in the layout which tends to reduce the total area of the layout. The designed Single ended differential amplifier has been taken as an example circuitry to check the same.

II. METHODOLOGY

Cadence® virtuoso® 64 is a powerful tool that provides numerous capabilities for easy and fast design entry. Well defined component libraries and sophisticated wire routing capabilities allow faster design. The proposed technique has been implemented on an example circuitry of single ended differential amplifier.

Fig 2 shows the procedure on which the layout of the example circuitry is made and to reduce the total area of the layout. Cadence® Virtuoso® 64 tool has been used to make the transistor level implementation of the circuit. Schematic of the example circuitry has been created using technology libraries and checked for connection errors. Different analyses were made on the circuit and checked whether it satisfies all the given specification or not. Layout of the same design has been created using Cadence Layout editor. It is a schematic driven layout in which physical view of the active components will be readily available, only interconnections alone has to be made. In order to avoid IR drop issues, lower metal layers have been used for signal routing and higher metal layers for power routing. After the layout design completion, the two physical checks namely i)Design Rule Check (DRC) and ii) Layout Vs. Schematic (LVS) performed on the layout design. The DRC checks for design rule specific constraints like spacing between the metal layers, sizes of each layer, contacts etc.The LVS compares the layout with schematic diagram for which the layout has been drawn and lists the errors if any shorts and opens are there between two designs. If any violation found, it has to be corrected and re-physical check has to be done on the corrected layout design.

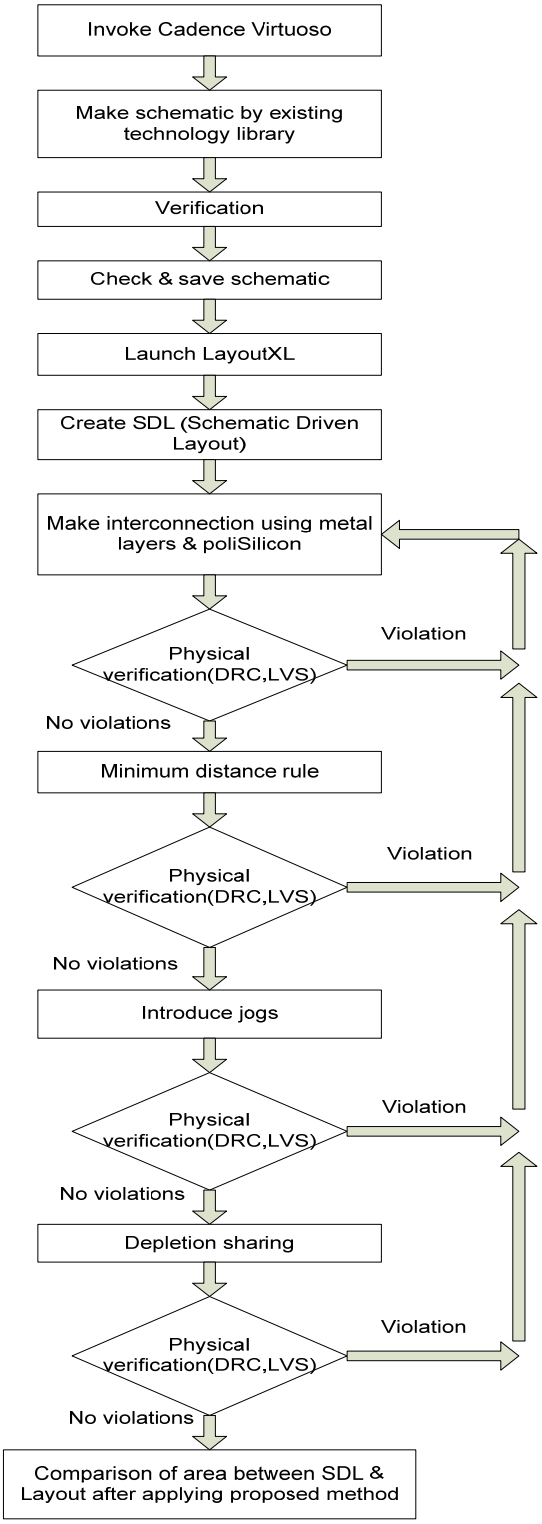

Fig. 2: Layout creation procedure, Physical check procedure and optimized layout procedure applied on example circuitry using Cadence® virtuoso®64

On the physically verified layout, the three proposed methodologies namely i) working towards minimum distance rule ii) introducing jogs and iii) depletion sharing applied one by one and through which total area of the layout has been minimized and during optimization procedure physical checks has been done in frequent interval to make sure that the new optimized layout was not introducing any other new violations to the design. The area of the layout which was obtained by applying the proposed methodologies together, compared with schematic driven layout.

III. PROPOSED WORK

A differential amplifier biased by N-type Metal Oxide Semiconductor (NMOS) current mirror and loaded with P-type Metal Oxide Semiconductor (PMOS) current mirror is taken as an example circuitry. The schematic of the example circuitry made using Cadence® Virtuoso® 64 schematic editor which is shown in Fig 3.The schematic driven layout of the same drawn using Cadence® layout editor which is shown in Fig 4. In this research work, the three techniques called i) working towards minimum distance rule ii) Introduction of jogs iii) Depletion sharing are used together to reduce the unwanted white space present in the layout have been proposed.

i) The minimum distance rule

The size of the components is controlled by how the designers draw metal layers in a layout. As manufacturing must follow certain rules for making the components, so the layout designers also follow those. The minimum distance rule specifies the minimum distance between two adjacent objects. Some examples of minimum distance rule in Cadence® virtuoso® 64(180nm) are

- Poly to Poly spacing must be greater than or equal to 0.3µm.
- Metal to Metal spacing must be greater than equal to 0.3µm.
- N-well to Oxide spacing must be greater than or equal to 0.5µm
- N-well to N-well spacing must be greater than or equal to 1µm.
- Nimp to Nimp spacing must be greater than equal to 0.4µm.

Fig 5a, 5b and 5c shows some examples of minimum distance rule. It would show DRC error if the distance between two objects is less than the specified minimum distance. In order to get better layout, the layout objects can be arranged in such a way that the distance between them is equal or slightly more than the specified minimum distance. This technique is applied on the layout of differential amplifier and it leads to reduction in the layout area. Fig. 6 shows the layout of differential amplifier after the application of minimum distance rule.

ii) Introduction of jogs

The small pieces of metal that are formed by splitting the conductor are called bricks [7]. Jogs are short pieces of metal wire running perpendicular to the preferred direction of routing. Instead of using straight conductors, jogs were introduced in between the conductors and through that the white space available effectively used which tends to reduce the total area of the layout. Layout after the introduction of jogs is shown in Fig. 7

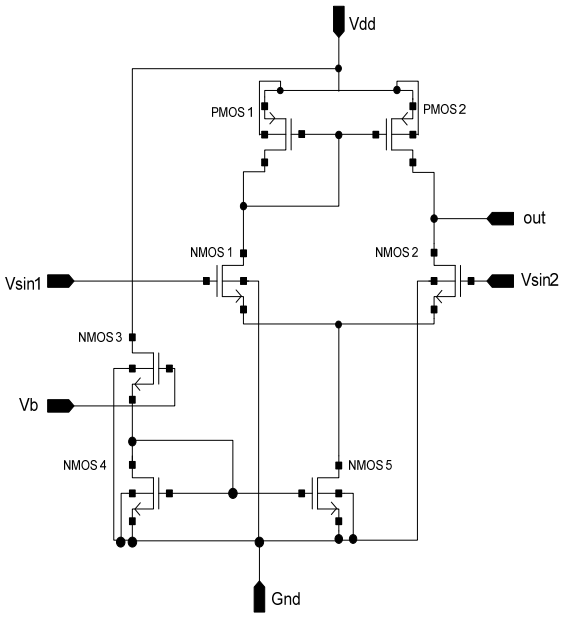

Fig. 3: Schematic Diagram of Differential Amplifier

iii) Depletion sharing

Layout area can be further reduced by a technique called depletion sharing. If the drain/source of one transistor is connected to drain/source of another transistor, instead of connecting those terminals using wire, the depletion area can be shared thus space between the two active regions can be eliminated. So that the total layout area can be reduced.

Fig. 8 shows the arrangement of three NMOS transistors. Nimp to Nimp spacing must be greater than equal to 0.4µm. The drain of first NMOS is connected to source of second NMOS and its drain is connected to drain of third NMOS. Instead of keeping them 0.4 µm away and connecting it using metal layer, by merging and sharing appropriate depletion areas of the three NMOS transistors, more than 12 µm length has been reduced. If the above said procedure used for the designs which has more number of transistors and more possibility of having depletion sharing, then more total layout area reduction is possible. Depletion sharing technique is applied on the layout of the differential amplifier and the resultant layout is shown in Fig. 9.

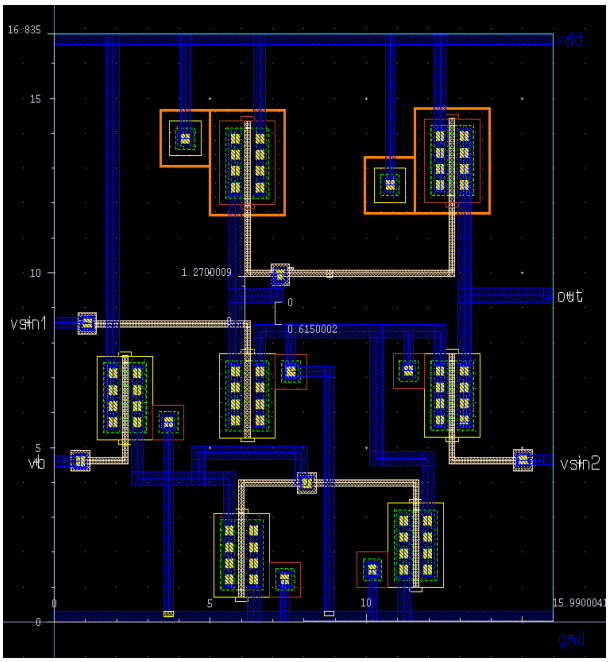

Fig. 4: Layout: Schematic driven layout of differential amplifier

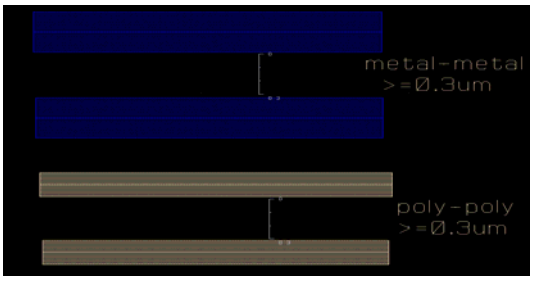

Fig. 5a: Spacing between Metal layer to Metal layer and Polysilicon to Polysilicon

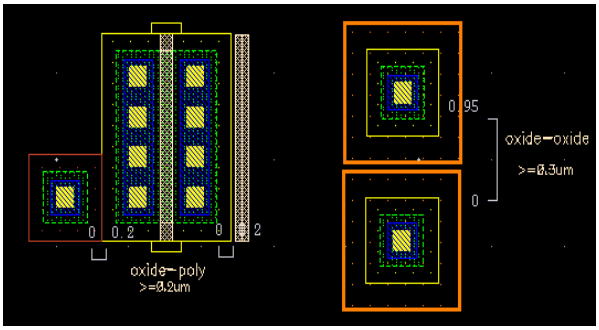

Fig. 5b: Spacing between Oxide- Oxide layers and Oxide to Polysilicon

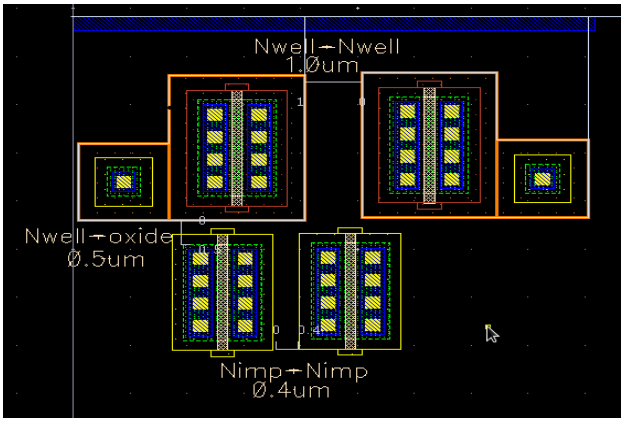

Fig. 5c: Nwell- Nwell spacing, Nwell – Oxide Layer spacing and Nimp- Nimp spacing

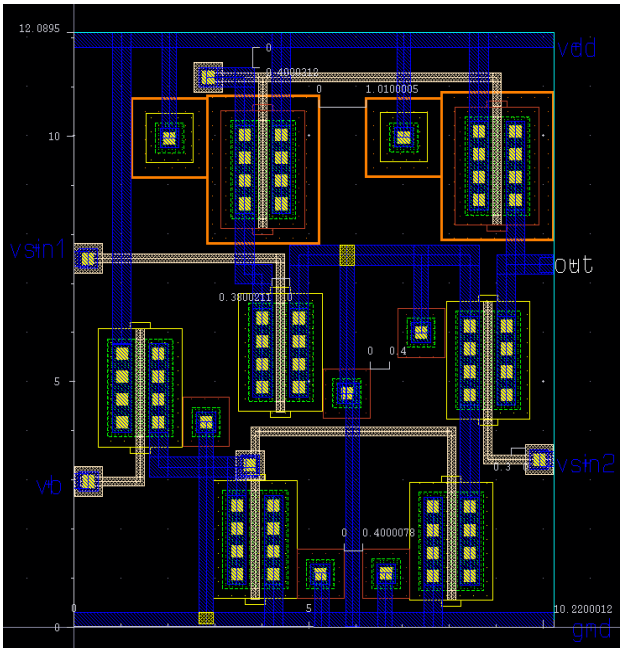

Fig. 6: Layout: After working towards minimum distance rule

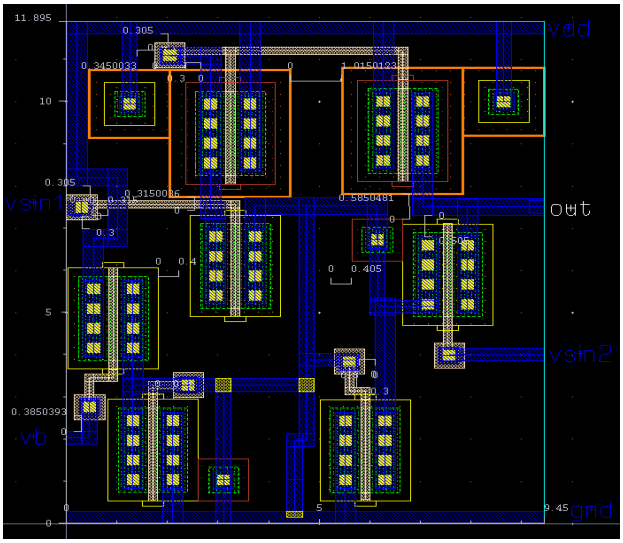

Fig. 7: Layout: After the introduction of jogs

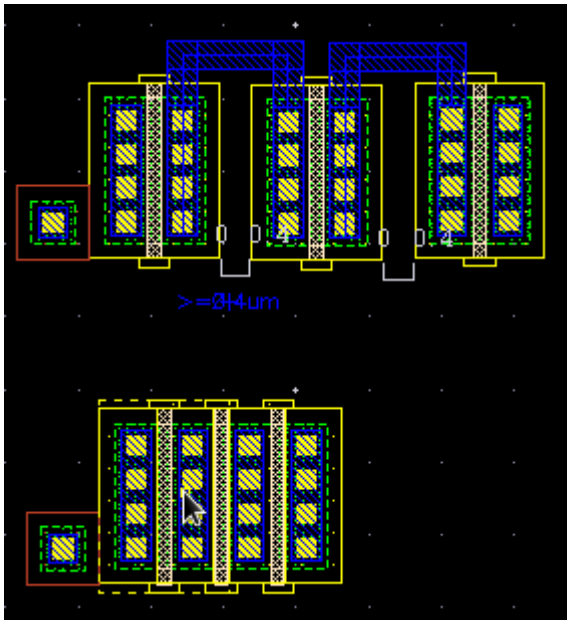

Fig. 8: Placement of three NMOS transistors to reduce critical area

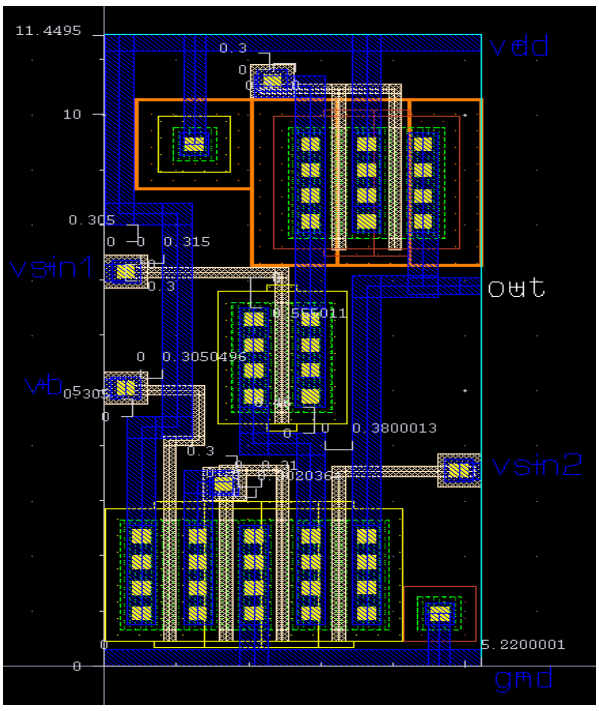

Fig. 9: Layout: After introducing depletion sharing

IV. RESULTS AND DISCUSSIONS

The objective of this proposed work is that reducing the unwanted white space present in the layout and through which the total area of the layout will get reduce. Single ended differential amplifier has been considered as an example circuitry to check the same. The differential amplifier has been designed by using two identical single stage common source amplifiers with NMOS current mirror as a biasing circuitry and PMOS current mirror as a load. The schematic driven layout of the example circuitry given by the tool mentioned in Fig 4 occupied an area of 269.52 µm². After applying minimum distance rule on layout shown in Fig 4, the total layout area has been reduced to 123.55 µm². Fig 6 shows the layout after an application of minimum distance rule and the rearrangement of the components. Then jogs are introduced on this layout, which reduce the area further to 114.25 µm² and which is shown in Fig 7.

Table I: Layout area occupied by each method and percentage of reduction obtained by each method.

Method	Length	Width	Layout area	Percentage reduction in area
Schematic driven layout by the tool	16µm	16.85 µm	269.52 µm²	-
Layout after applying strict minimum distance rule	10.22 µm	12.09 µm	123.55 µm²	54%
Layout after the introduction of jogs	9.45 µm	12.09 µm	114.25 µm²	57.6%
Layout after depletion sharing	5.22 µm	11.45 µm	59.79 µm²	77.81%

Finally depletion sharing has been introduced on the layout shown in Fig 7. Instead of keeping the transistors PMOS1 and PMOS2 1µm away and giving a connection using metal layer, the source of two transistors are shared and kept together. So that only one N-well is needed for both the PMOS and 1µm space can be saved. Similarly source of NMOS4 and NMOS5 are shared. Instead of connecting source of NMOS3 and drain of NMOS4 using metal layer, the depletion area is shared, likewise the drain of NMOS5 and the source of NMOS2 are shared. Thus the area further reduced to 59.79 µm². After applying minimum distance rule, in either the case that is introducing Jogs first then introducing depletion sharing or introducing depletion sharing first and then introducing Jogs were resultant with the same area reduction in the layout. Compared to schematic driven layout, after applying the proposed techniques the total reduction in area achieved is 77.81%. The percentage given in the table I against each method represents area reduction achieved by that method when compared to schematic driven layout.

V. CONCLUSION AND FUTURE WORK

This research work proposed the methodologies through which the unwanted white spaces present in the layout area have been reduced which tends to reduces the total layout area. Experimental result shows that above proposed methodologies significantly reduces the layout area on the example circuitry taken and this leads to big impact on yield improvement of the chip. If the same procedure applied for complex layouts, better white space reduction and through which better area reduction in the layout is possible. If the above said proposed methodologies are automated by using any one of the scripting language, then this can be used in any industrial design project which follows the same technology library.

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