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Advanced Pulse Width Technique in Impedance Source Cascaded Multilevel Inverter with Asymmetric Topology

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***Abstract*— In this research, a single phase Z-source cascading Multilevel Inverter, Nine-level inverter topologies with a trinary DC sources are offered. The recommended topologies are expanded by cascading a full bridge inverter with dissimilar DC sources. This paper recommends advanced pulse with modulation technique as a switching scheme. In this PWM technology, trapezoidal modulation technique is used as variable amplitude pulse width modulation. These topologies compromise reduced harmonics present in the output voltage and superior root mean square (RMS) values of the output voltages linked with the traditional trapezoidal pulse width modulation. The simulation of proposed circuit is carried out by using MATLAB/SIMULINK.**

Keyword - Z-Source Multilevel Inverter, Total Harmonic distortion, Variable amplitude Pulse Width Modulation, Cascaded multilevel inverter

I. INTRODUCTION

Multilevel DC-AC converter have drained incredible interest in recent years and have been planned for several high-voltage and high-power applications. Switching losses in these high-power high-voltage DC-AC converters characterize an issue and any switching conversions that can be rejected with Z-source cascaded multilevel inverter. The term multilevel starts with the outline of the nine-level DC-AC converter. All probable steady states of a Z-source inverter are recognized and analyzed with the objective of developing design plans for the symmetrical impedance network [1]. Three level Z-source inverters are latest single stage topological explanations proposed for buck boost energy conversion with all encouraging advantages of three level switching recollected [2]. A multi loop controller for a *Z*-source inverter was established for distributed generation applications. En route for that end, the *Z*-source inverter was demonstrated with a state space an average of technique, and essential transfer functions are derivative [3]. To overcome the restricted operating range, these inverters necessity to be connected with a discrete DC-DC converter step in the front end. This permits them to operate in both buck and boost operation. This topology is frequently known as a two stage inverter. Lesser scale two stage inverters have been developed for domestic distributed generation applications with fuel cells [4]–[6].

A five level cascaded multilevel inverter built Z-source inverter has been offered. In the suggested topology output voltage amplitude can be enhanced with Z network shoot through state controller [7]. The improvement of two three level cascaded Z-source inverters, whose the output voltage can be paced down or up dissimilar a outdated buck three level inverter. The anticipated inverters are premeditated using two three phase voltage source inverter bridges, provided by two exclusively designed Z-source impedance systems [8]. The Z-source neutral point clamped inverter has been projected with different three levels up - down power conversion resolution with upgraded output voltage waveform superiority. In principle, the design of Z-source inverter gatherings by selectively shooting through its input power sources, joined to the inverter using two inimitable Z-source impedance systems, to boost up the inverter three level output voltage waveform [9]. A seven level Z-source cascaded multilevel inverter premeditated with three midway Z-source networks system associated between the input dc source and multilevel inverter circuit [10]. Trinary three phase cascaded multilevel inverters with nine level output voltage generation in different PWM [11].

II. IMPEDANCE NETWORK

The arrangement of impedance network is shown in the Fig. 1. It comprises of a pair of inductors and capacitors respectively. The rate of inductors and capacitor can be preferred based on the output voltage requirement of inverter. A diode is coupled in the impedance network as shown Fig. 1 to block the reverse flow of current. A voltage nature impedance source inverter can assume all active and null switching states of voltage source inverter. Unlike predictable voltage source inverter, an impedance source (Z-source) fed inverter has a unique feature of permitting both power semiconductor switches of a phase leg to be turned ON instantaneously (shoot through state) without injuring the inverter. The impedance network (Z-source) changes the circuit

arrangement from that of a voltage source to an impedance source (i.e. Z-source). It permits the voltage source inverter to be operated in a new state called the shoot through state in which the two power semiconductor switching devices in the same leg are instantaneously turned on to effect short circuit of the dc link. During this state, energy is transmitted from the capacitors to inductors, thereby giving rise to the voltage boost ability of the impedance source (Z-source) fed inverter. The effect of the phase leg shoot through on the inverter presentation can be investigated by allowing for the circuit.

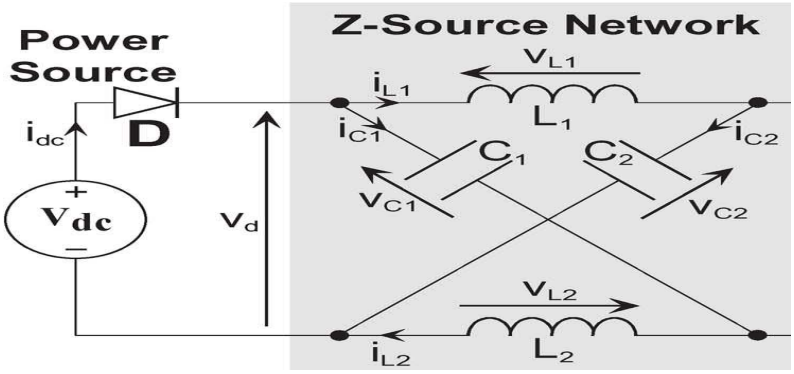

Fig. 1. Impedance Network Circuit

III. Proposed Impedance Source Cascaded Multilevel Inverter

The Simulated circuit structure of an impedance source (Z source) nine level cascaded multilevel inverter is shown in Fig. 2. It comprises of series single phase half bridge inverter units, (Z) impedances and input DC source voltages. Input DC voltage sources can be found from battery bank, solar cells and fuel cells. It contains of eight IGBT/Diode power semiconductor switches. Each Half bridge contains of four power semiconductor switches respectively. Input source for each half bridge is fed from impedance network (Z-source). This voltage will be lesser or larger than input DC source voltage. Nature of the load is resistive and inductive. Based on the rate of capacitor pairs and inductor pairs in the impedance network (Z-source) magnitude of V_{dc} is preferred. Since each and every half bridge in an inverter circuit can offer three output voltage levels ($0V_{dc}$, $+V_{dc}$ and $-V_{dc}$). The output voltage of the inverter values for −4Vdc, −3Vdc, −2Vdc, −1Vdc, 0, 4Vdc, 3Vdc, 2Vdc, 1Vdc, can be planned, as represented in Fig. 1. The output voltage of the first bridge is indicated by Vdc and the second full bridge is indicated by 3Vdc. Then the output voltage of the load is V=Vdc+3Vdc.

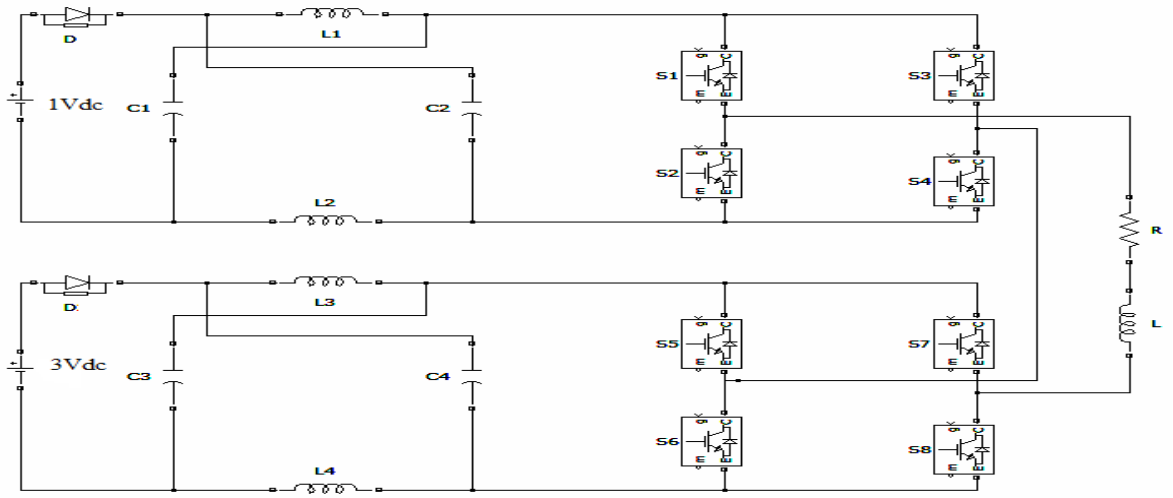

Fig. 2. Proposed impedance source cascaded multilevel inverter.

IV. Simulation Result

A single phase impedance source (Z- source) cascaded multilevel inverter with unequal voltage sources to yield nine level inverter output is modeled in SIMULINK using power systems block set. Simulations are implemented for different values of m_a ranges from 0.8 to 1 and the equivalent %THD is measured using the FFT block and their values are shown in Table I. Table V shows the fundamental V_{rms} of inverter output for the same values of modulation indices. Table III and Table IV show the corresponding values of crest and form factor. Table II demonstrate percentage distortion factor of the inverters output voltage. Fig. 3-12 display the simulation output voltage and FFT plot of single phase multilevel inverters and their respective harmonic order of a spectrum with various modulation techniques but for only one sample of modulation indices(ma=0.85).

For ma= 0.9, it is represents in the Fig. (4, 6, 8, 10, and 12) the harmonic energy level is displayed in: Fig. 4 shows 40th order in phase disposition PWM techniques. Fig. 6 shows 23rd, 35th, 40th orders phase opposition disposition PWM techniques. Fig. 8 shows 29th, 31st, 35th, 37th, 39th orders in alternate phase opposition disposition PWM techniques. Fig. 10 shows 5th, 40th orders in carrier overlap PWM techniques. Fig. 12 shows 19th, 23rd, 29th, 31st, 37th, 40th orders in variable frequency PWM techniques. Simulation results are obtained by using following parameter such as V_{dc} = 50V, Load resistance is 100Ω, carrier frequency (f_c) is 2000H_Z, modulation frequency (f_m) is 50Hz.The following parameters value is used in simulation: VDC=100, 3VDC = 300 Resistive (load) = 100, Carrier frequency is fc=2000 Hz and reference frequency fm=50.

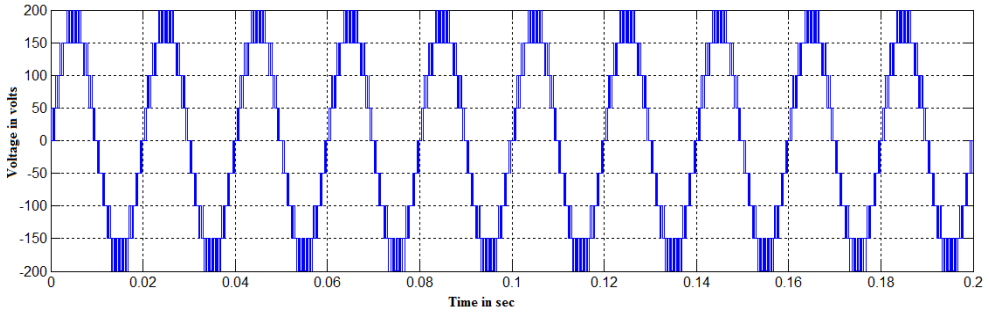

Fig. 3. Output voltages generated by phase disposition PWM control

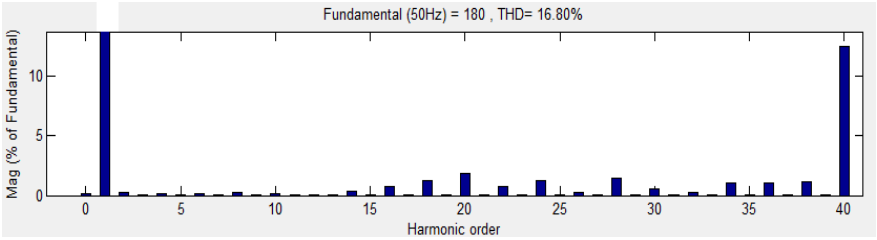

Fig. 4. FFT plot for output voltage of in phase disposition PWM control

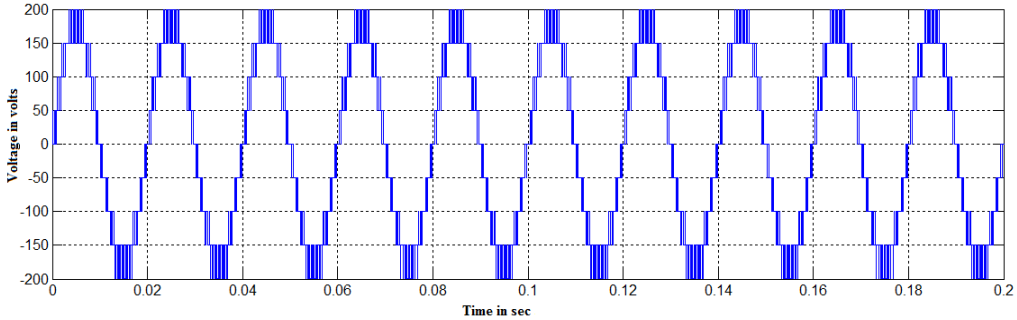

Fig. 5. Output voltage generated by phase opposition disposition PWM control

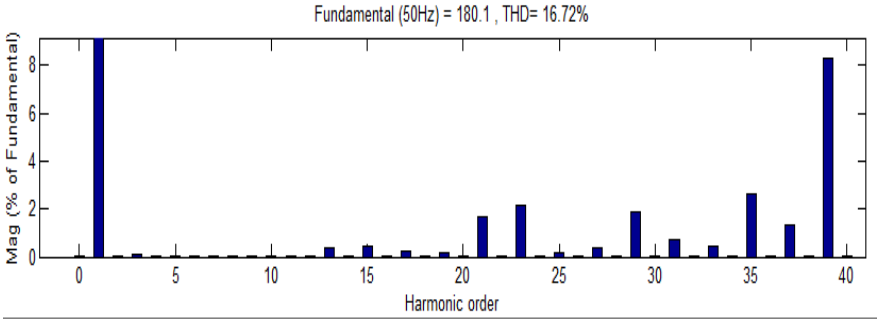

Fig. 6. FFT plot for output voltage of phase opposition disposition PWM control

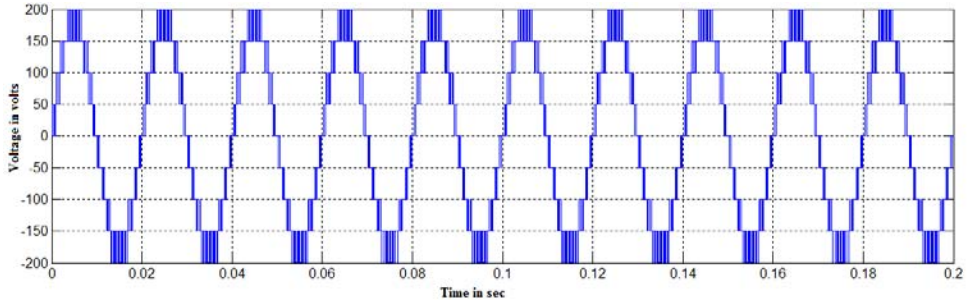

Fig. 7. Output voltages generated by alternate phase opposition disposition PWM control

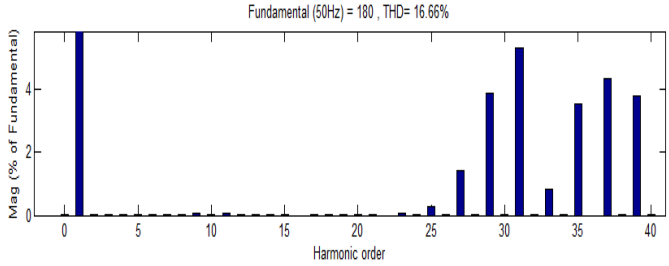

Fig. 8. FFT plot for output voltage of alternate phase opposition disposition PWM control

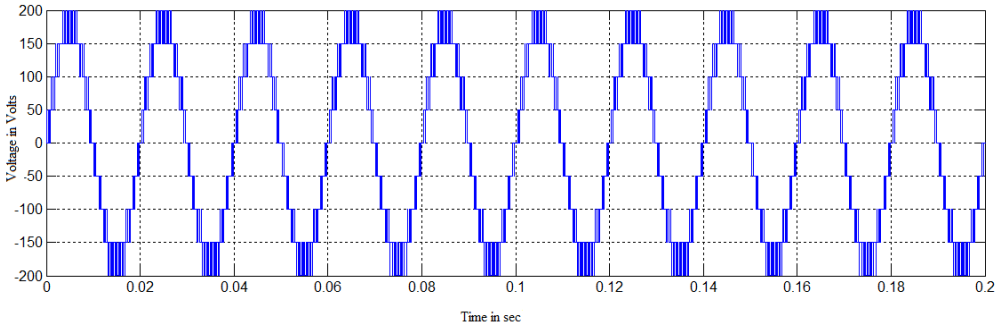

Fig. 9. Output voltages generated by bipolar carrier overlap PWM control

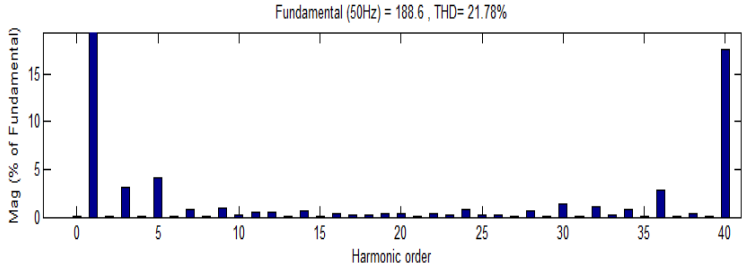

Fig. 10. FFT plot for output voltage of bipolar carrier overlap PWM control

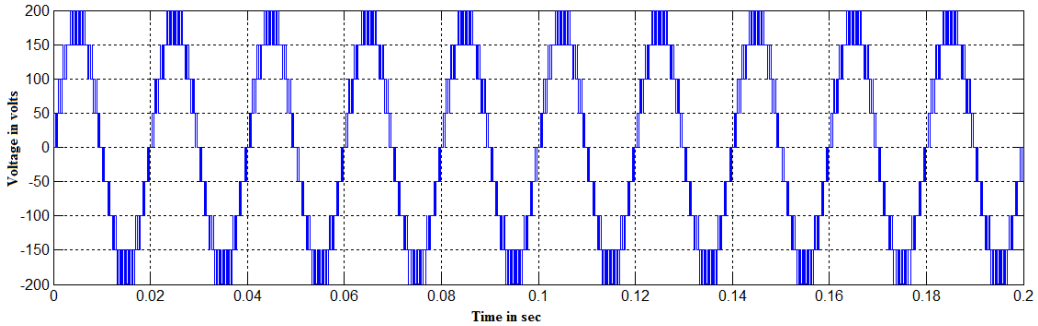

Fig. 11. Output voltages generated by bipolar variable frequency PWM control

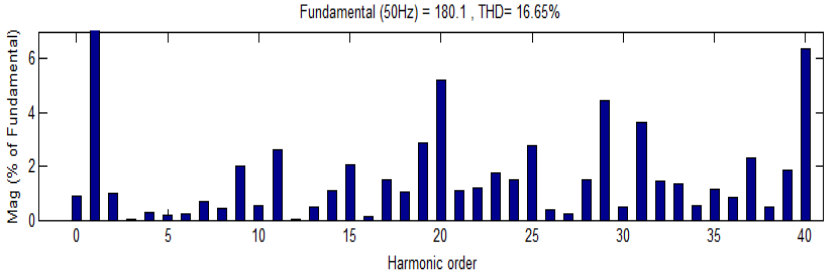

Fig. 12. FFT plot for output voltage of bipolar variable frequency PWM control

TABLE I. %THD for Different Modulation Indices

Ma	PD	POD	APOD	CO	VF
1	13.69	16.90	13.26	18.28	13.81
0.95	17.14	15.58	15.63	20.17	15.58
0.9	16.80	16.72	16.66	21.06	16.65
0.85	16.98	17.00	16.85	23.62	17.07
0.8	17.14	16.90	17.53	26.07	16.73

TABLE II. Distortion Factor for Different Modulation indices

Ma	PD	POD	APOD	CO	VF
1	0.00035	0.00035	0.00013	0.0018	0.00059
0.95	0.00138	0.00041	9.24E-05	0.0025	0.00096
0.9	0.00487	0.00013	9.27E-05	0.0037	0.0043
0.85	0.00138	0.00035	0.00022	0.0064	0.00438
0.8	0.0004	0.00061	0.00015	0.0052	0.00431

Table III. Crest Factor for Different Modulation Indices

Ma	PD	POD	APOD	CO	VF
1	515.49	54.03	865.36	888.61	557.57
0.95	296.61	611.91	616.23	400.29	121.29
0.9	509.40	5.8E+08	5.8E+08	765.21	79.41
0.85	154.85	5.6E+08	100.58	474.70	65.899
0.8	296.61	5.4E+08	5.3E+08	173.33	63.36

Table IV. Form Factor for Various Modulation Indices

Ma	PD	POD	APOD	CO	VF
1	1.4146	1.4137	1.4146	1.4144	1.4144
0.95	1.4143	1.4140	1.4143	1.4143	1.4136
0.9	1.4139	1.4143	1.4140	1.4147	1.4146
0.85	1.4146	1.4136	1.4144	1.4143	1.4137
0.8	1.4144	1.4137	1.4526	1.4146	1.4143

TABLE V. Fundamental RMS Voltage for Different Modulation

Ma	PD	POD	APOD	CO	VF
1	141.4	113.1	141.4	145.2	141.4
0.95	113.1	134.5	134.4	139.4	134.4
0.9	127.3	127.4	127.3	133.3	127.3
0.85	120.2	119.8	120.2	126.7	120.2
0.8	113.1	113.1	113.1	119.2	113.1

V. CONCLUSION

In this work the simulation results of single phase impedance source (Z source) cascaded multilevel inverter with R load with different modulation Techniques are obtained with help of MATLAB/SIMULINK. Various performance parameter measures such as THD, Fundamental V_{RMS}, form factor and Crest factor was obtained and tabulated. Single phase impedance source (z source) cascaded multilevel inverter produce the nine level output voltage. It is showed that phase opposition disposition techniques provides the low harmonics distortion and in phase disposition techniques provides larger value of fundamental RMS voltage compared to all other pulse width modulation techniques.

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