Adiabatic Logic Circuits Using FinFETs and CMOS – A Review

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***Abstract*—With continuous advancements evolving in the VLSI design arena, the real time chips which operates on the principle of charge recovery logic realizes substantially lower power dissipation levels than the conventional circuit technique counterparts. In early times, the research in adiabatic logic computing engrossed on the asymptotic energetics of computation, discovering new VLSI techniques in the process, which utilizes reversible logic and the adiabatic switching (or the so called energy recovery logic). In this paper, a review of the Adiabatic Logic circuits found in the literature has been presented, while operating these logic circuits using the FinFET devices. The performance benefits acquired in the circuits while using the FinFET devices in place of CMOS devices are explored. The quasi-adiabatic circuits operating with four phase power clock supplies, namely, the 2N-2P, 2N2N-2P, PFAL, PSAL, DCPAL, CPAL and ICPAL structures have been considered for the analysis. The 32nm & 45nm conventional CMOS devices and 32nm double gated FinFETs have been used for the performance analyses carried out using the industry standard Cadence® EDA tools.**

Keyword-Adiabatic computing, Energy-recovery circuits, Energy Recovery Using FINFET, Low Power VLSI Circuits

I. INTRODUCTION

The low power and low energy operation are very essential in portable devices like mobile, laptop etc. In these devices the battery life is of primary concern. Several conventional low power circuit design techniques have been proposed in the literature [1] [2] [3] [4]. They primarily concentrate on certain parameters such as, the physical capacitance, the power supply voltage and the activity factor[5]. The reduction of voltage commendably reduces the energy consumption, however, at the cost of increased physical capacitance, and the circuit switching frequency [6]. Curtailing the capacitance switching can be restricted by the current drive requirements. However, the voltage cannot be reduced imprudently, since the energy dissipation due to leakage can become a dominant factor.

Conventional CMOS circuits do not allow the recovery of the energy, since the energy gets dissipated in the pull-up and pull-down networks during the charging and discharging processes of the nodal capacitances respectively. Hence, a large amount of heat or energy is dissipated across the devices in the conventional CMOS circuits. These disadvantages led the circuit designers to the non-conventional logic called the *adiabatic logic* or the *charge Recovery logic* or *Energy recovery logic*[7] [8]. These adiabatic circuits recover a major portion of the energy that is stored in the nodal capacitances during the logical computation, and they also enable the reuse of the energy for successive computations. Hence, these are called as energy recovery or charge recovery logic [9].

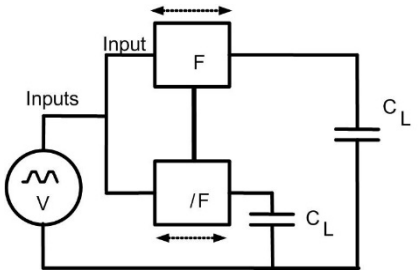

Fig. 1. Adiabatic Logic Circuit

The basic structure of an adiabatic logic circuit is shown in Figure 1. These circuits employ ac power clock signal in place of a dc power supply for enabling the recovery of the energy. Theoretically, an adiabatic logic circuit consumes zero power. However, in practical circuits, they show inherent loss in energy due to the non-zero resistance in the switching devices, leakage of stored charge in the circuit nodes and incomplete energy recovery from the logic nodes [8]. While comparing with the conventional CMOS circuits, the maximum

switching frequency of operation of an adiabatic circuit is very low due to the usage of time varying voltage source [10] and the inherent nature of the adiabatic circuit operation.

This article is organized as follows. Section 2 describes the classification of adiabatic logic. Section 3 illustrates asymptotically adiabatic logic circuits. Section 4 reviews various Quasi-adiabatic logic circuits found in the literature, implemented using CMOS and FinFETs. Section 5 explains the structure and various modes of operation of the FinFETs and their effect on adiabaticity. Section 6 presents the simulations results and inferences. Section 7 concludes the paper.

II. CLASSIFICATION OF ADIABATIC LOGIC

Adiabatic circuits are majorly classified into i) Energy/Charge Recovery Logic and ii) Reversible Logic

i) Energy/Charge Recovery Logic recovers partial energy with some amount of inadvertent energy loss due to the irreversible energy while operating the circuit.

ii) Reversible Logic is one in which the input vector is uniquely recovered from output vector in one-to-one correspondence, which in turn enables the use of the output states.

Many results [6] [7] [8] portray that the minimum energy requirement is directly related to the number of informational bits spent. Hence, if a design technique can be conceived without incurring any loss of information, the energy requisite for operating such a circuit could hypothetically be reduced to zero. Bennett and Landauer [11] at IBM performed reversible computation and demonstrated that there can be no information loss and hence hypothetically zero energy could be required. A system is said to be reversible if there is no loss of information at any time during its transformation [12]. Further classification of Energy/Charge Recovery Logic is described in detail and depicted in Figure 2.

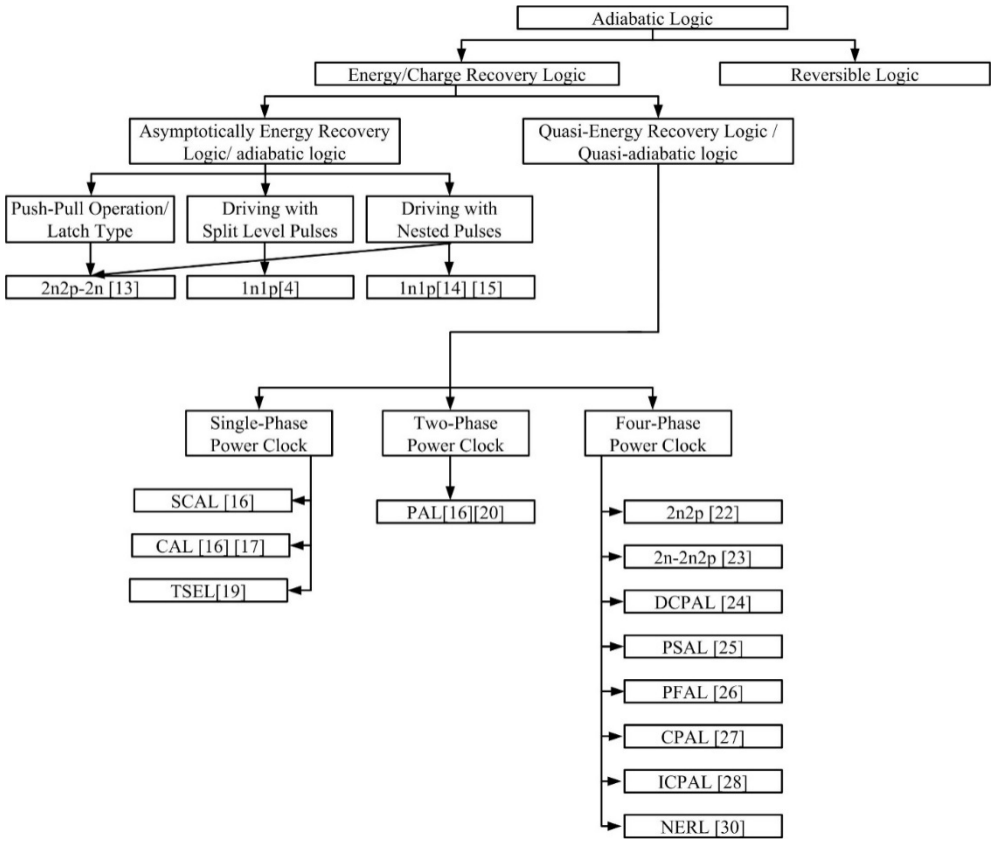

Fig. 2. Classification of Adiabatic Logic

III. ASYMPTOTICALLY ADIABATIC LOGIC

The asymptotically adiabatic logic circuit incurs power dissipation due to the non-zero rate of change of supply voltage and it can be decreased to any desired low level at the cost of operating frequency. Normally the asymptotically adiabatic logic is classified into the following categories:

i) Push-Pull/Latch Type
ii) Driving with Split Level Pulses
iii) Driving with Nested Power Clock Pulses

The push-pull latch type 2n2p-2n shown in Figure 3a is similar to the 2N2P with the modification that it employs additional transistors MN3 and MN4 in the pull down network, which is controlled by antiphase output signals fed back. Devices forming the pair MP1-MN3 and MP2-MN4s make a transistor conducting such that a conductive coupling between the common source terminals and common drain terminals are maintained [13]. The nested driving pulses shown in Figure 3 (b) are applied for the cascaded chains of logic. However, this arrangement leads to some major disadvantages, such as, 1) The asymptotically energy recovery logic, while using nested pulses cannot provide pipelining, 2) The driver design is very hard and energy dissipated is inversely proportional to the width of the driving pulse edges and 3) By the structure, there arises in inherent limitation on the maximum operating frequency and the logic latency of the circuit.

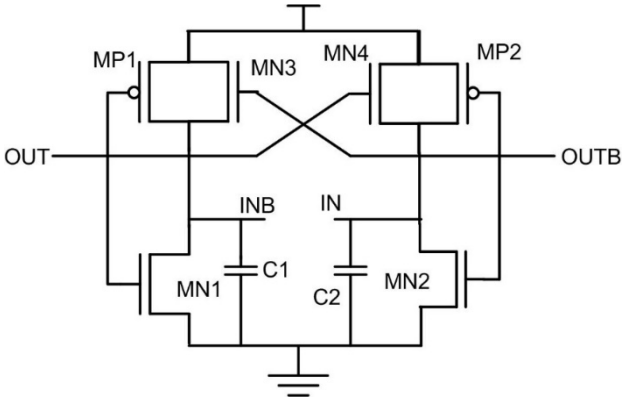

Fig. 3. (a) 2n2p-2n Logic

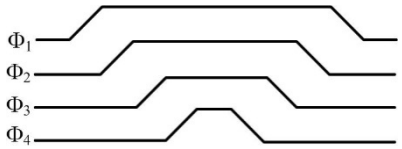

Fig. 3. (b) Nested Pulses

Figures 4 (a) and 4(b) represent the structure of 1N1P, with a split-level driving pulse. Here, the CMOS gates are connected to two complementary split level pulse voltage drivers. The maximum voltage of the supply clock is maintained to be Vdd/2. The Foremost hitch of this asymptotically adiabatic logic is that it cannot provide pipelining and it remains a challenge to design the voltage driver for the circuit. The Split Level Charge Recovery Logic (SCRL) is similar to the CMOS inverter, connected with an additional pass gate at the output. The clock Φ_1 and Φ_1'drive the inverter as shown in Figure 5. Φ_2 and Φ_2' control the pass gate. The SCRL inverter cascades are powered by the split level pulses.

The SCRL is so called since Φ_1, and Φ_1' start at Vdd/2 and split towards Vdd and GND. When input IN is high, the output follows Φ_1' and when low, follows Φ_1. When the output is sampled by a successive gate, the pass gate of this inverter is turned OFF, thus tristating the output. Then, Φ_1, Φ_1' are restored back to Vdd/2[14].

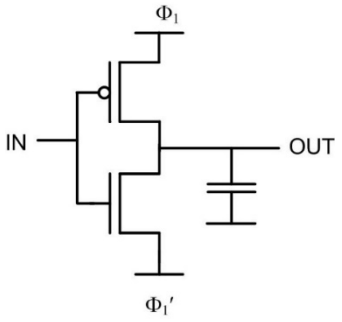

Fig. 4. (a) 1n1p logic

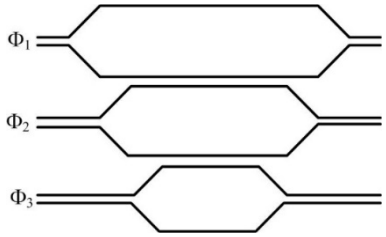

Fig. 4. (b) Split level pulses

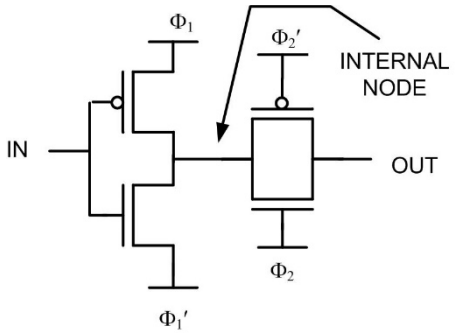

Fig. 5. Split-level charge-recovery logic

IV. QUASI ADIABATIC LOGIC STRUCTURE

The source coupled adiabatic logic (SCAL) works using a single-phase power-clock. The basic structures of the PMOS SCAL and NMOS SCAL are shown in Figures 6 (a) and 6(b) respectively. The current source present at the top of the device controls the current flow. The sinusoidal power clock PCLK is supplied to the circuit as shown. The PMOS SCAL operates in the discharge phase and the evaluate phase alternately. When the PCLK ramps down from V_{dd} to Gnd, the energy stored in the output node is recovered back during the discharge phase. When the PCLK ramps up to V_{dd} from 0V, the devices MP1 and MP2 are switched *on* and when $V_{gs}$of MP7 is greater than the threshold voltage V_{th}, device MP7 is switched on[15]. This in turn rises the voltage V_x at the node X. If IN is high and INB is low, then a pull down path for theoutput node is created and hence the node OUTB follows V_x down. This is called the *evaluation phase*. In the basic structure of a SCAL, the outputs are pre-charged *high*. The two phases of operation are the charging phase and the evaluating phase [16].

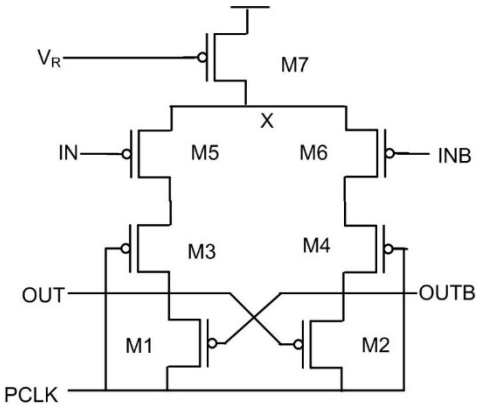

Fig. 6. (a) SCAL PMOS

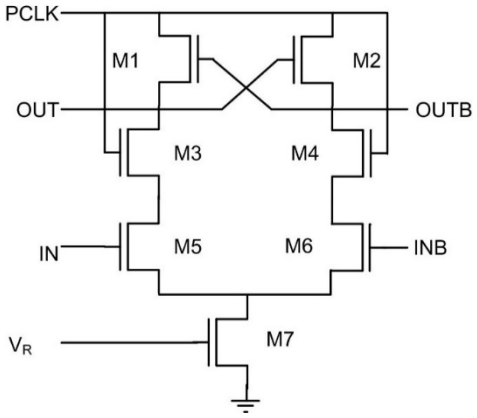

Fig. 6. (b) SCAL NMOS

Figure 7 shows the Clocked Adiabatic Logic (CAL) [17], an adiabatic logic structured vaguely similar to 2N-2N2P. While comparing with the 2N-2N2P, the adiabatic logic CAL requires additional devices, namely, MN5 and MN6 NMOS device as shown in Figure 7. It utilizes a single phase power clock along with another clock input at the gate terminal of devices MN5 and MN6. However, the CAL circuits achieve half the throughput of corresponding 2N-2N2P circuits, as they enable logic evaluation only in alternate clock cycles. Moreover, the CAL designs are more dissipative due to their increased device count when compared with 2N-2N2P and also their additional clock input X.

The structure of the PMOS True Single Phase Energy Recovery Clock (TSEL) and NMOS TSEL are shown in Figures 8(a) and 8(b). It is similar to the NMOS SCAL except for the additional footer device M7. The TSEL using PMOS operates in two phases, namely, 1) discharge phase and ii) evaluate phase. During the discharge phase, when the power clock ramps from $V_{dd}$to Gnd, it pulls OUT and OUTB to the threshold value and hence the energy stored in the output nodes are allowed to discharge. The output of the gate is evaluated during the evaluation phase. When the input IN is high and INB is low, the power clock turns on the devices MP1 and MP2. This boosts up the difference of the output nodes. When this difference exceeds the threshold voltage of the PMOS device, MP1 is turned OFF and the node OUTB is charged adiabatically. The operation of NMOS TSEL is complementary to that of the PMOS TSEL [18] [19].

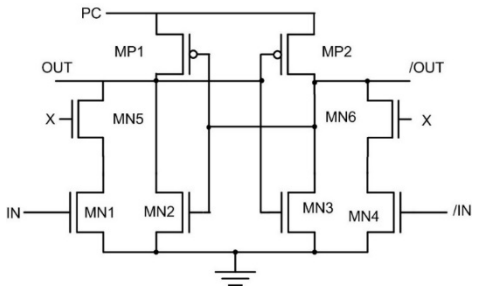

Fig. 7. Clocked Adiabatic Logic

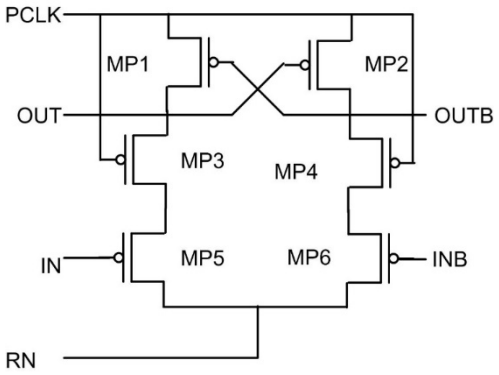

Fig. 8. (a) True Single Phase Energy Recovery Clock PMOS

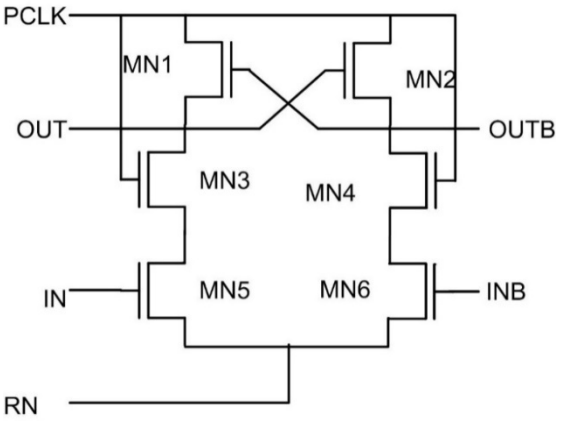

Fig. 8.(b) True Single Phase Energy Recovery Clock NMOS

Figure 9 shows the structure of Pass Transistor Adiabatic Logic (PAL), an adiabatic logic family similar to 2N-2P. In PAL, the ground node of 2N-2P is connected to the power supply for eliminating non-adiabatic energy consumption. PAL uses two-phase power clock for its operation [20] with every alternate stage of the adiabatic pipeline operated by the alternate phases of the power clock.

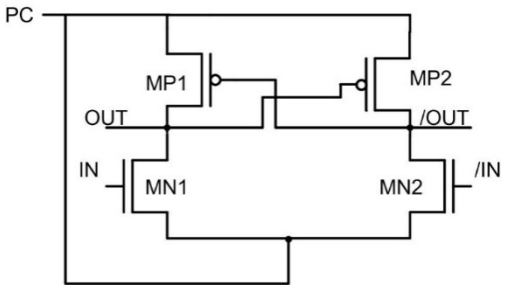

Fig. 9. Pass Transistor Adiabatic Logic

V. SIMULATION AND ANALYSIS

All the four phase power clock adiabatic circuits have been designed using the 32nm FinFET PTM models. In adiabatic circuits, there is an inherent phase shift of 90^o introduced between the input and output. Furthermore, it may be noted that each of the power clock signals lag behind the succeeding one by 90^o as shown in Figure 10. This feature helps in efficient cascading of pipelined stages during the Evaluate, Hold, Recovery and Wait phases. In other words, each stage is supplied with the clock pulses of same amplitude and each clock pulse is out of phase with its successive clock pulse by 90^o [21].

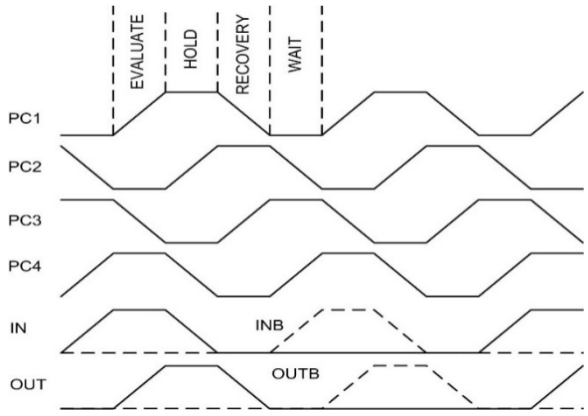

Fig. 10. Four-state power clock signals, Input and Output Signals

The 2N2P circuit or the Efficient Charge Recovery Logic (ECRL) shown in Figure 11 consists of two PMOS devices MP1 and MP2 in the pull up network. Input IN leads the power clock by 90^o. The dotted lines in the pull down network marked F and /F represents the functional logic blocks. These functional blocks can be replaced by any other desired logic for creating the required stage in the adiabatic pipeline. When the input signal IN is at logic 1, device MN1 starts to conduct and OUT is pulled down to ground. At this point, the power clock PC ramps up from 0 to V_{dd}. This phase is named as the Evaluate Phase. The PMOS device MP2 is switched ON, as

OUT goes to 0.This shorts the /OUT to PC and node /OUT follows PC. This phase is called the Hold Phase. During the recovery process, power clock PC ramps down from V_{dd}. Charge at /OUT is at higher potential than the PC, which is reclaimed back to PC and hence /OUT starts to fall. The Wait Phase helps in resetting the current stage and waits for next evaluation stage. This cycle of operation repeats across the stages of the adiabatic pipeline [22].

The input applied for the pipeline through successive evaluation stages reaches the output of the last stage, and it may be noted that it will be in phase with the power clock operating the last stage. However, the 2N-2P suffers from floating output node problem. This occurs when the /OUT voltage falls below V_{tp}. The charge present in the /OUT node cannot find the discharge path. Floating output node can be eliminated in 2N-2N2P adiabatic logic, when both MP2 and MN2 do not conduct with respect to /OUT node, or when both MP1 and MN1 do not conduct with respect to node OUT [23]. The structure of 2N-2N2P is shown in Figure 12.

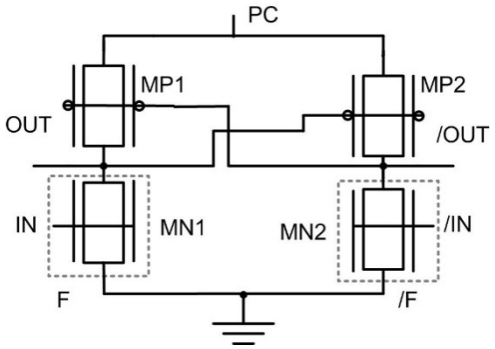

Fig. 11. 2N2P Adiabatic Logic

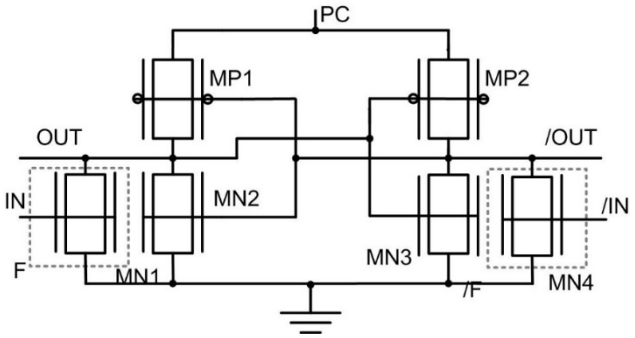

Fig. 12. 2N2N2P Adiabatic Logic

One of the interesting characteristic of the dynamic logic is the *pre-charging*. This feature has been employed in the Differential Cascode Pre-resolved Adiabatic Logic (DCPAL) [24]. The pre-resolving phase *pre-resolves* the input to reflect on the output nodes. The name *pre-resolving* represents the fact that one of the two nodes, based on the inputs, are going to be pre-resolved or made to reach the ground potential. A pre-resolving footer NMOS device MN3 is placed at the common source terminal of MN1 and MN2 as shown in Figure 13. As can be noted, it employs two power clock signals. The power clock PC3 is applied to the gate of MN3, which leads the second power clock PC1 by 180^{o} and the input signal IN by 90^{O}. During the pre-resolving phase, the input IN is seen rising, power clock PC3 is kept at logic high. Based on the input, when MN3 is switched ON, the node N1 is pulled to ground thus pre-resolving the input, for further evaluation phase for the present stage.

When IN reaches the threshold voltage of MN1, the transistor starts conducting and the node OUT remains at 0V. The power clock PC1 ramps up to V_{dd} and hence MN2 is switched on. This results in raising the voltage at node /OUT up following the power clock PC1. Now, MN2 remains OFF and it allows only the minimum amount of leakage current to go through. When PC3<V_{tn}, device MN3 is OFF. This further enhances the reduction of leakage current due to the body effect. When IN goes low, OUT and /OUT retains their nodal values and MN3 is OFF. During the recovery phase, /OUT follows PC1 and OUT falls below 0 due to the capacitance of MP1.

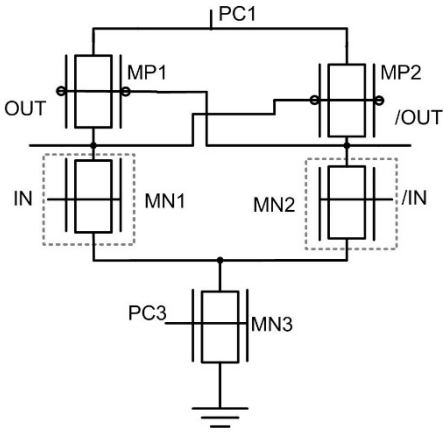

Fig. 13. Differential Cascode Pre-resolved Adiabatic Logic

The pipelined operation of the adiabatic circuits can be realized by operating the successive power clocks with 90^o phase shift between each other and in that order. Pre-resolve Sense Adiabatic Logic (PSAL) [25] operates similar to the DCPAL, with its 2P latch replaced by a 2N2P latch in the pull-up and pull-down networks as represented in Figure 14. The PSAL has a unique advantage of the capability to operate at very low frequencies as low as, kHz to MHz because of the 2N-2P latch which eliminates the floating output node effectively. The leakage current in the circuit is also reduced, due to the fact that the footer transistor of the structure introduces the stacking effect, which abets the leakage current reduction process.

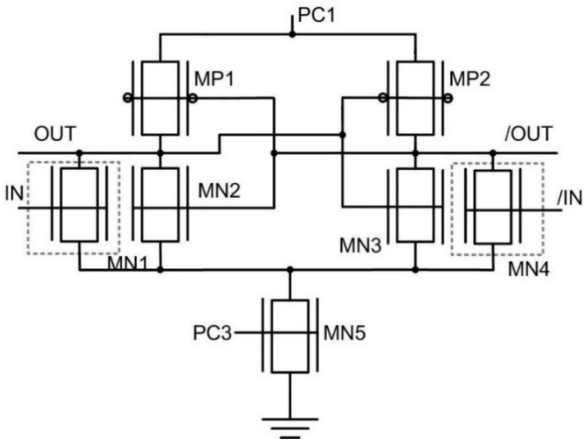

Fig. 14. Pre-resolve Sense Adiabatic Logic

Figure 15 shows the structure of the Positive Feedback Adiabatic Logic (PFAL) [26]. This circuit can be designed with the use of the cross-coupled inverters formed by MN1-MP1 and MN2-MP2 as shown. The functional blocks are connected in the pull up network. Assuming input IN High, the device MN3 conducts and pulls the OUT node towards power clock, which in effect makes MP2 to switch off and OUTB is disconnected from power clock. It may be noted that the pull up network resistance R_{on} decreases with the parallel path formed by MP1 and MN1.

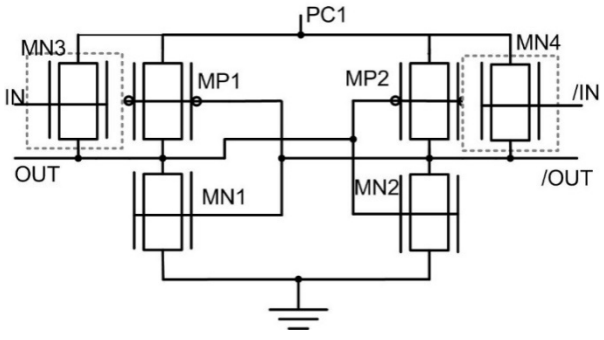

Fig. 15. Positive Feedback Adiabatic Logic

Complementary Pass-Transistor Adiabatic logic (CPAL) [27] is designed using the logic functional block and a load drive circuit. The structure of CPAL shown in Figure 16 consists of the functional block formed by NMOS transistors MN5-MN8. Load drive circuit consists of transmission gates (MN1, MP1 and MN2, MP2). Transistors MN3 and MN4 avoids floating output nodes. When IN is high and INB is low, MN1 and MN3 are turned ON. Node X is charged to V_{DD}-V_{TN} and Y is clamped to ground. IN falls down causing MN1 and MN2 to switch off. Voltage at node X remains same. During evaluation phase, the power clock ramps up and X is bootstrapped to a higher level than V_{DD}-V_{th} because of the gate to channel capacitance of MN5. At this point, the node OUT is charged to V_{DD} and OUTB is clamped to ground as MN8 is switched ON. During the recovery phase, the power clock falls down from V_{DD} to ground, and hence the charge in output node is recovered through MN5.

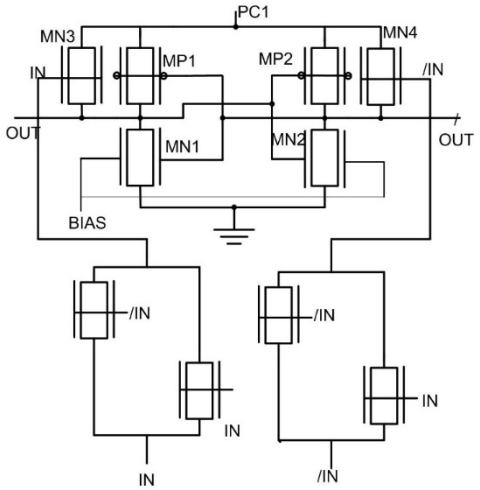

Fig. 16. Complimentary Pass Transistor Adiabatic Logic

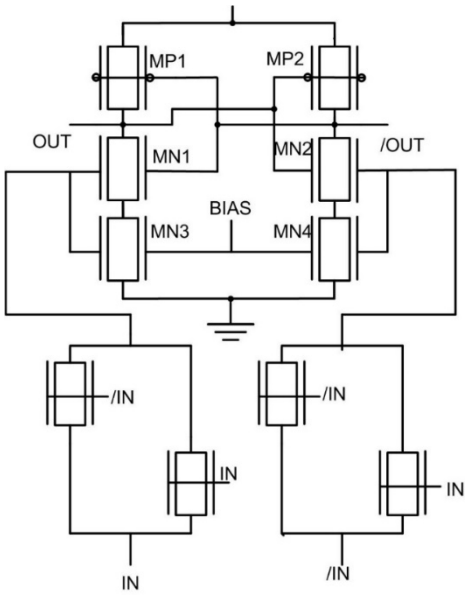

Fig. 17. Improved Complimentary Pass Transistor Adiabtic logic

Improved Complimentary Pass Transistor Adiabatic Logic (ICPAL) is shown in Figure 17. It consists of cross coupled inverters which are helpful to stabilize the complimentary outputs. ICPAL realizes reduced leakage power dissipation. Complimentary pass transistor logic produces valid logic results and passes it to the evaluation transistor MN1 and MN4. During the evaluation phase, the inputs remain stable and power clock ramps up to V_{dd} and the output follow the power clock. Furthermore, the transistors MN3-MN4 and MN1-MN2 have similar on/off states. In the recovery phase, when the input becomes low, the power clock ramps down to zero. The charge stored in the output capacitance streams back to supply via MP1 and MP2. Large charge stored in the output capacitance is recovered back again despite the fact of existing leakage path to the ground, due to the stack transistors MN3 and MN4 [28].

Figure 18 shows a 4-stage adiabatic inverter chain. The power clocks keep the adiabatic pipeline stages operate in synchronism with each other. The inverters of 2N-2P, 2N-2N2P, PFAL, CPAL, ICPAL follows this

structure for cascading. It can be noted that the DCPAL and PSAL utilize two power clocks separated by 180^o between them for each stage.

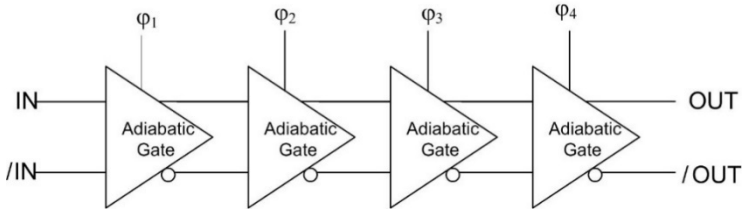

Fig. 18. Structure of a 4-stage cascaded adiabatic pipeline

To elaborate, for a certain stage in the adiabatic pipeline, if the PC3 is the pre-resolving power clock connected to the footer device, the PC1 acts as the evaluating power clock. Note that the successive stages are operated by the power clock combinations PC1-PC3, PC2-PC4, PC3-PC1 and PC4-PC2. Due to the fact that input and power clock is separated by 90^o, unwanted glitching and power spikes can be avoided.

The total energy dissipation per cycle incurred by the quasi adiabatic circuits is given by

$$E_{diss} = \left(\frac{2R_{on}C_L}{T}\right) C_L V_{dd}^2 + \left(\frac{1}{2}\right) C_L V_{th,p}^2 + V_{dd} I_{Leak} kT + E_{opn} (1)$$

$$E_{diss} = \frac{2C_L^2 V_{dd}^2}{\left[T\mu_p C_{ox}\left(\frac{W}{L}\right)\left(V_{dd} - V_{th,p}\right)\right]} + \frac{1}{2} C_L V_{th,p}^2 + V_{dd}\mu C_{ox}\frac{W}{L} V_T^2 \exp\left(\frac{V_{gs} - V_{th}}{\eta V}\right) kT + \left(\frac{1}{2T}\right) R_{on} V_{dd}^2 C_L^2 \quad (2)$$

Here, $V_{dd}$is the power-clock peak voltage, $C_L$is the load capacitance, T is the transition period of the rising /falling edge of the power-clock and k is the number of phases per cycle when the leakage currents flow through a device. The capacitance $C_L$is the sum of the selective drain-bulk junction capacitance C_{db}, the gate-drain and gate-source capacitances $C_{gd}$and C_{gs}, gate-bulk capacitance C_{gb}, the gate-drain and gate-source overlap capacitances $C_{gdo}$and $C_{gso}$of the device connected at the junction and *Co. Co* includes the wire capacitance and the capacitance offered by the next stage. The power needed to operating the latch is given by$(\frac{1}{2T})R_{on}V_{dd}^2C_L^2$. This also includes the energy that is spent in maintaining the output states during the Hold phase. The energy recovery behavior of an adiabatic circuit is determined by the charging path resistance, the load capacitance and the dissipation due to leakage and charge sharing of the nodes [29].

The basic NERL inverter circuit is illustrated in Figure 19. It consists of two main parts namely, i) bootstrapping and ii) logic function. The bootstrapping circuit is designed by bootstrapped NMOS transistors (M7 and M8) with two isolation transistors (M5 and M6). Secondly, the logic circuit consists of four pass-transistors (M1 and M4). Floating output nodes can be eliminated byM9 and M10 such as to ensure stable operation of the circuit. Two power-clock signals with 180^o phase difference are used for each logic gate. Power clock Φ_1 is used for transferring charge from the power clock to the output nodes. The other power-clock Φ_1' is utilized for pre-charging a bootstrapping node (Either A or B depending on its inputs). It keeps its voltage level high enough so that charge is transferred completely and recover the used charge fully. Next two power-clock signals follow with a 90 phase lag for pipelining [30].

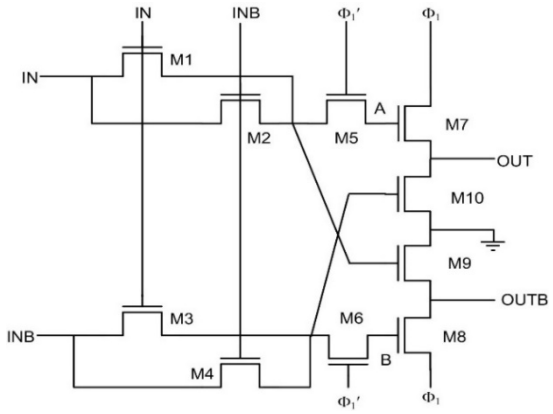

Fig. 19. NMOS Energy recovery logic

VI. FINFET

The name FinFET arises from the fact that the device has a conducting channel wrapped around by a "fin" which is made up of a thin silicon. This forms the body of the device. This structure allows excellent control over the channel. This overcome the short channel effects and reduces the leakage current. Thickness of the fin equals the effective channel length of the device. An additional gate suppresses short channel effects and improve Ion/Ioff ratios by increasing electrostatic stability [31]. Electric potential in the undoped channel is given by

$$\emptyset = C_0 . exp\left(\pm\frac{x}{\lambda}\right) \quad (3)$$

where C_0 is a constant and λ is the natural length of the device. λ, given by the following expression

$$\lambda = \sqrt{\frac{\varepsilon_{si}}{n.\varepsilon_{ox}}} t_{ox} t_{si} \quad (4)$$

λ Should be as small to influence drain potential on the channel. This is possible by using high- κ dielectric materials, decreasing oxide thickness t_{ox} and/or silicon thickness t_{Si}, or by increasing the relative control of the gate through coefficient n. Here, n is one for single-gate devices and two for double-gate devices. FinFET consists of a fin which is located between source and drain and above the substrate. This protrudes vertically above the substrate as a fin. Some of the advantages of FinFETs are high on-state current. Lower off state current and Faster Switching Speed. Structure, cross-sectional view and symbol of FinFETis shown in Figure 20 (a),(b) and (c). FinFETs operate at three different operating modes, namely,the shorted gates mode, low power mode and independent gate mode. They are according to front gate and back gate being tied up or not. Each operating mode has its own unique characteristics.

i) Shorted gate (SG) mode: Switching speed and on-state current is very high and hence achieves high performance. Here, the front gate and the back gate are shorted together to form shorted gate.

ii) Low power (LP) mode: Off-state current is low and this reduces leakage current in the circuit. Front and back gates are applied with individual voltage bias. One of the gate is reverse biased to control the leakage current. Hence, this is also called as Reverse Bias (RB) mode.

iii) Independent Gate (IG) mode: Front gate and back gate are individually operated [32].

Table I and II display the details of various parameters of 32nm CMOS and FinFET PTM models.

TABLE I. Primary Parameters of 32nm CMOS PTM Models

DEVICE		PRIMARY PARAMETERS				
		L_{gate}	W_{fin}	T_{ox}	V_{thf}	e_{ox}
CMOS	NMOS	32nm	110nm	1.65e-9	0.508V	3.9
	PMOS	32nm	100nm	1.75e-9	-0.45V	3.9

Analysis and design is performed using 32nm CMOS and FinFET model files, which was obtained from PTM. Various parameters associated with the FinFET are as follows. The L_{gate}, H_{fin}, W_{fin}, T_{ox}, V_{thf}, V_{thb}, E_{ox} and$T_{box}$are the space between source and drain called as channel length, fin height, channel width, thickness of the oxide, threshold voltage of front and back gate, permittivity of oxide and thickness of the bulk oxide, respectively. Here, the $H_{fin}$is an important parameter, which makes the processing more complicated and which makes the device vulnerable for defects. The voltage supply provided is 0.9V for both the CMOS and FinFET.

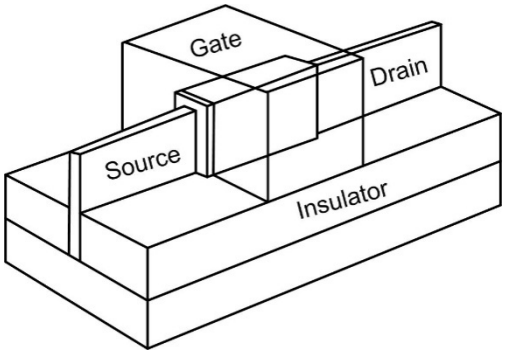

Fig. 20. (a) Structure of FinFET

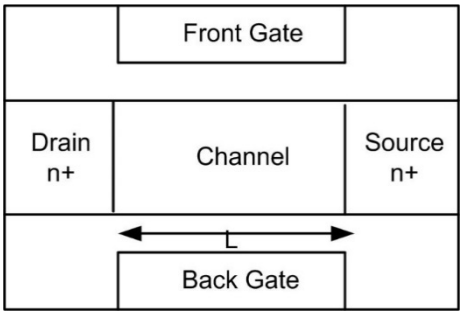

Fig. 20. (b) Cross-sectional view of FinFET

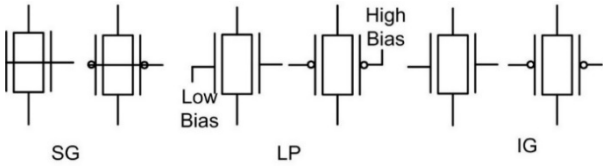

Fig. 20. (c) Symbol of FinFET

Figure. 21 shows the I-V characteristics of the devices for comparison. From the illustration, it can be clearlyobserved that the FinFET has better current capability than the CMOS counterpart, due to its lower I_{off} and progressively increasing I_{on} rate. This leads to higher switching speed. Hence, the FinFETs are capable of operating at high frequency applications as against the conventional CMOS.

TABLE II. Primary Parameters of 32nm FinFET PTM Models

DEVICE/ PRIMARY PARAMETERS		**L_{gate}**	**H_{fin}**	**W_{fin}**	**T_{ox}**	**V_{thf}**	**V_{thb}**	**T_{box}**	**E_{sib}/E_{ox}**
FinFET	**N-TYPE**	32nm	40nm	80nm	1.4e-9	0.29V	0.29V	5x10e-7	11.7/3.9
	P-TYPE	32nm	50nm	100nm	1.4e-9	-0.25V	-0.25V	5x10e-7	11.7/3.9

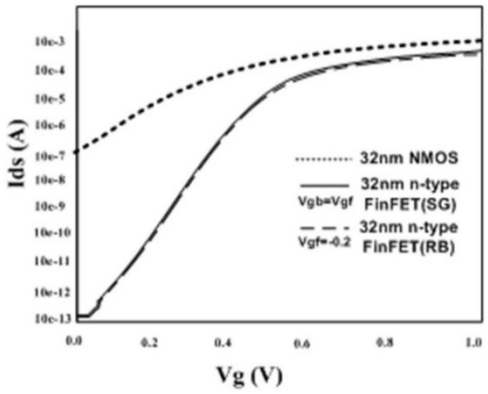

Fig. 21. I-V characteristics of 32nm of N-type MOSFET and N-type FinFET with both SG and RB mode

VII. PERFORMANCE ANALYSIS AND DISCUSSION

Leakage current, power consumption and energy are reduced in the circuits designed using adiabatic logic when compared to the conventional design techniques. Further, these adiabatic logic circuits are designed with both CMOS devices and FinFETs. FinFETs suppress short channel effects in comparison with conventional CMOS devices. Application of the FinFET is beneficial as ultra-low leakage power (10^{-12} W) can be attained at the cost of less area. Its pleasing features is being exhibited as reduced energy consumption per operation in the range of aJ for 1-bit adder circuits and also being stable trough different modes including high speed low power with normal 1V supply voltage. Energy curve of various quasi adiabatic logic circuits is shown in Figure 22.

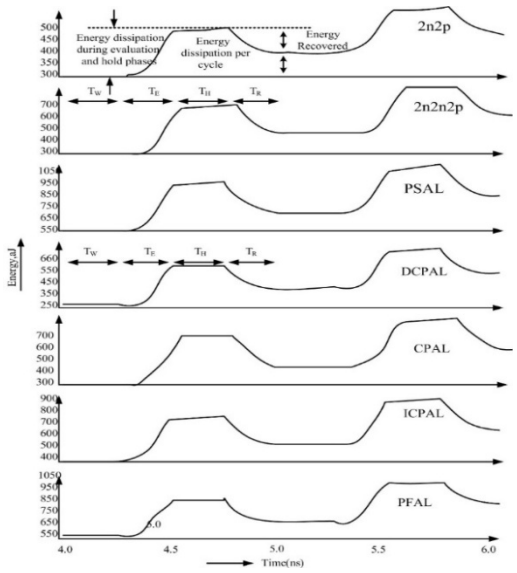

Fig. 22. Energy Curves of various Adiabatic Logic Circuits

Figures 23 and 24 show the graph which represents the comparison of power and energy analyses between CMOS and FinFETs. From the graphs, it can be inferred that power and energy consumption is very less in the FinFET based circuits rather than the CMOS based circuits. Figures 25 and 26 represent the energy and power of FinFET Adiabatic circuits over a voltage range from 0.6V to 0.9V. It is clearly seen that as the voltage increases, the power and energy also increases gradually.

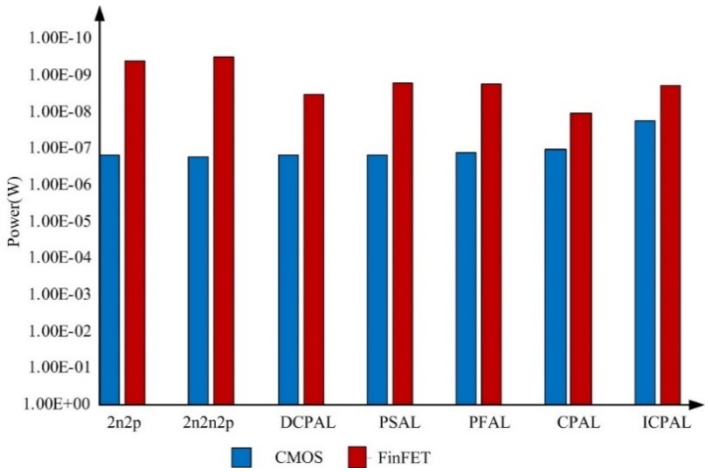

Fig. 23. Comparison of Power in Adiabatic circuits designed using CMOS and FinFET

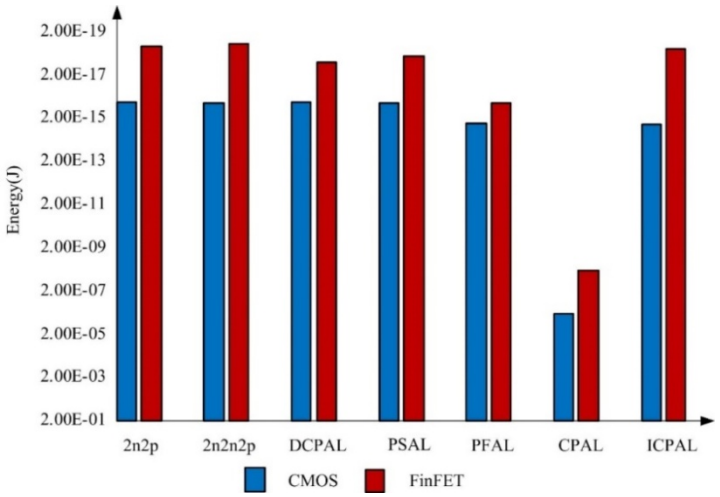

Fig. 24. Comparison of Energy in Adiabatic circuits designed using CMOS and FinFET

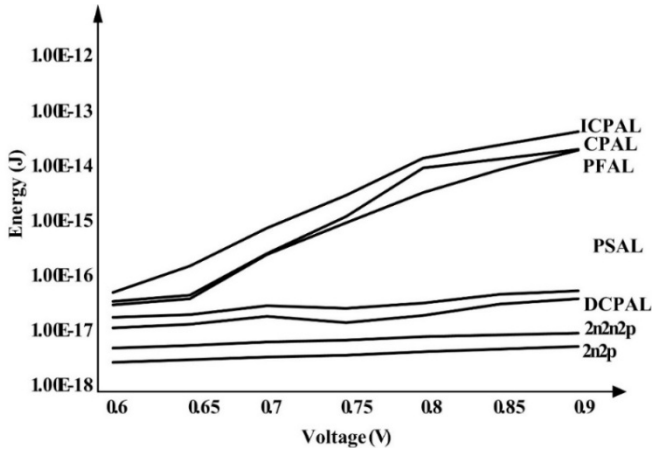

Fig. 25. Energy of FinFET Adiabatic Circuits over a voltage range

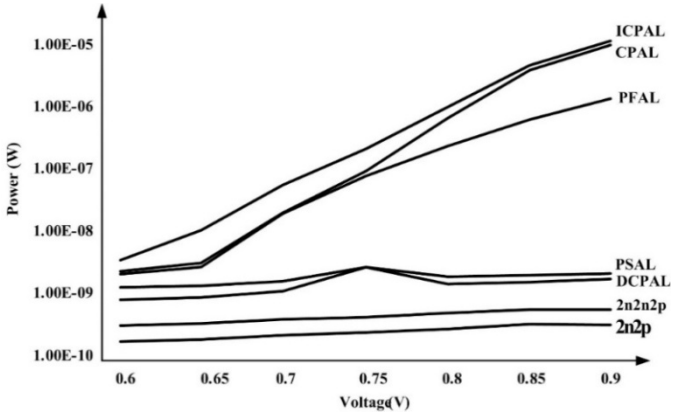

Fig. 26. Power of FinFET Adiabatic Circuits over a voltage range

VIII. CONCLUSION

This article portrait a broad overview of adiabatic logic in the first segment and provides a comparison between the performances of the circuits designed using the FinFET devices over the CMOS devices. The advantage of using FinFETs over the CMOS is validated through the considerable reduction of the power consumption in the quasi-adiabatic circuits discussed. This is due to the ability of the FinFET devices in overcoming the short channel effects and leakage currents. It is clearly presented by the analyses made using 32nm BPTM technology models. While the adiabatic circuits using CMOS incur power dissipation of the order of 1uW to 100uW for various adiabatic circuits, the counterpart circuits using FinFET incur power dissipation of the order of 0.1nW to 5nW only.

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