# Co-Simulation of BLDC Motor Commutation by using MATLAB Simulink and Xilinx System generator

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Abstract- This work mainly focuses on Matlab Simulink model for electronic commutation of BLDC motor and co simulation of the model by using Xilinx System generator tool. The BLDC motors (AKM21E) are available in small size with good speed/torque characteristics. Since, the efficiency and dynamic response is high compared to brushed DC motor, they have widely used in various applications. We are using BLDC motor for adjusting the focus in radio telescope. The efficient electronic commutation is designed and tested by using modelling in Matlab Simulink. The Co verification of the model is done by using Xilinx system generator.

Keywords- BLDC motor, Simulink, system generator.

## I. INTRODUCTION

The three phase BLDC motors are widely used in industries due to its high performance in terms of speed, torque, size, low maintenance, dynamic response, noiseless operation, and so on. Due to lot of advantages, they are widely used in industries like, aerospace modelling, consumer electronics, automation, medical electronics, automobiles, etc.. The BLDC motors are basically Alternating current (AC) synchronous motors available in single-phase, 2-phase and 3-phase motor is widely used in the applications. The BLDC motor consists of rotor and stator, rotor is made up of permanent magnet. The stator basically resembles induction motor and coils are properly placed in the slots and they are interconnected each other to make windings. Based on stator windings, they are classified as trapezoidal and sinusoidal motors.

The commutation of the BLDC motor can be done electronically by mounting three Hall Effect sensors in the stator on non driving end of the motor. The rotor position is sensed by the hall sensors and we can come know which of the stator winding is energized. The stator windings must be energized in a sequence in order to run the BLDC motor. The hall sensors require power supply from 5 volts to 24 volts and current range from 5 to 15 amps. The torque is produced due to interaction between magnetic field generated by the stator and permanent magnets. Peak torque and rated torque are the two torque parameters in BLDC motors and motor can be loaded up to rated torque in continuous operation and torque remains constant.

Nowadays there is a tremendous technological improvement in computational tools such as computer aided design (CAD) tools and widely used in the design of more complex electronic circuits. The main advantage of CAD tool is that allows the input data in graphical user format and we can reuse the simulation results. Before any hardware implementation of the model, the simulation can help the designers to design the proper model. In our work we have used MATLAB/SIMULINK for the design of BLDC motor speed control.

The hardware co simulation is done with the help of Xilinx system generator tool. This system generator provides two tools, one tool helps us to model using blocks and other tool called hardware generator used for HDL model. The Xilinx blocks are synthesizable and can be used for real FPGA implementation of the model.

## II. SIMULINK MODEL OF THE BLDC MOTOR CONTROL

The Simulink model of BLDC motor control is as shown in Fig.1 and consists of the following blocks.

- The main power circuit: constant DC voltage source which provide 100V to driver circuit.
- The motor: the module "Permanent magnet synchronous motor" is selected with the waveform of air gap magnetic flux density being trapezoidal and the width of its flux part is 120 electrical.
- Measurement unit: This unit consists of bus selecting module "Bus selector," which is used to measure the variables of the motor when it is operating such as back EMF, current, rotor speed, torque etc.
- Logic unit: Consist of logical operators, which are used for generating gate pulse signals for driving circuit that is PWM generator.
- Controller unit: This unit consist of proportional integral controller, signal generator, relational operator.

The back-EMF is given has feedback in closed loop system in order align with the voltage and it is very important in commutation. There is 120 degree phase difference between each phase of the back EMF in commutation.



Fig.1. Simulink model of BLDC motor control

The MOSFET switches are used for the realization of current commutation of BLDC motor. The switches are connected in three phase bridge structure for three phase motor as shown in Fig.2. The switches are controlled by using pulse width modulation (PWM), which easily controls the speed and torque.



#### Fig.2. Three phase bridge of MOSFET switches

The three hall sensors ha, hb and hc are required to detect the position of the rotor, which are mounted at 120 degree intervals on the stator. One of the hall sensors changes its state for every 60 degree rotation and one of the motor terminals driven high, another terminal driven low and third terminal is floating. The phase windings U,V and W are energized based upon the hall sensor signals. The implementation of the decoder for hall sensor signals is as shown in Fig.3.



Fig.3. Implementation of decoder

## III. CO SIMULATION OF THE MODEL USING SYSTEM GENARATOR

Our aim is to implement hardware co simulation of the Simulink model using HDL coder for electronic commutation of BLDC motor. The Fig. 4 shows the Xilinx blocks, HDL coder and Simulink model for hardware co simulation. The Xilinx Blockset is a library for bit and cycle true simulation and supports for custom functions. The HDL coder uses Xilinx customized IP cores and generates synthesizable code. Before real time implementation of the controller using FPGA, the prototype testing of the design is done by using HDL coder. The prototype testing of the controller design is verified successfully by using VHDL code generated from the HDL coder. The system generator generates bit file for FPGA and we have used VIRTEX II pro XS2VP30 FPGA board for the implementation purpose.



Fig.4. Co simulation of the model

The proportional integral (PI) controller is used for the regulation of motor speed which has two different techniques of speed control, one is open loop and other one is closed loop. In our work we have used closed loop speed control of BLDC motor, which can be controlled by using PI controller which regulates the duty cycle. The Speed of BLDC motor is set to reference speed and any diversion from this speed will be given as error signal to PI controller. Depending on error signal, it can increase or decrease the duty cycle of applied gate signal

## IV. RESULTS OF HARDWARE CO SIMULATION

The following table 1 shows the specifications of the motor chosen for the hardware co- simulation of the model.

Phase resistance	2.8750 ohm		
Phase inductance	8.5 mH		
Voltage constant	146 V/Krpm		
Number of phases	3		
Voltage input	100 V		
Proportional constant	0.013		
Integral constant	16.61		

TABLE 1.	BLDC Motor	Specifications
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The simulation results for closed loop operation of the motor using Xilinx system generator is as shown in Fig.5. The ha, hb and hc are the hall sensor outputs.



Fig.5. Simulation results of closed loop system

Simulation results of the stator current are as shown in Fig. 6.



The simulation results of the back EMF obtained at constant reference speed of 3000 rpm is as shown in Fig. 7.



#### Fig.7. Back EMF

The response of motor for 100V input voltage with fixed reference speed of 3000 rpm is shown in Fig. 8.

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#### Fig.8. Speed at 100V

The motor runs with a constant reference speed of 3000 rpm. The initial response may be differ for different input voltages but final speed of motor is the reference speed this is because of using proportional integral controller which regulates the duty cycle of gate pulse on receiving the error signal.

## V. CONCLUSION

The simulation results help us to verify the functionality of the model. The model is designed for the commutation of BLDC motor, which works fine and performance is better. The results obtained are close to the theoretical analysis of specifications chosen for the model. It helps us to reduce the time for writing HDL programs. The validation of the simulation results is tested by using Xilinx Virtex II pro FPGA board.

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