Low Power RAM-Based Hierarchical CAM on FPGA

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***Abstract*- In the Wireless routers and network devices like servers CAM Content-Addressable Memories will be mostly used as they have a good transmission rate to transfer the data packets. So the main role played by the CAM is it will easily transfer the internet packets like drop and forward mechanism. During such transmission CAM having a limitations like more power usage and less integration density, along with this CAM will not be accessible on the FPGA which will elaborate the usage of network framework. In order to reduce the high power consumption and to achieve more integration density,we proposed RAM based CAM in this paper. Now-a-days on modern FPGA we can see larger blocks of RAM.**

Keywords- TCAM, Wireless routers, Power efficiency.

I. INTRODUCTION

CAM is a type of special memory where it performs high speed search applications.In Existing random access memory (RAM), gives the user the address of the RAM returns data available for this specific job address. CAM about changing fashions .The key and came back to the address which is stored in memory. The of the cam which operate in a single clock cycle. It also works with high speed, and various other hardware and software applications systems today variable cam is used when it is necessary to divide, pick up and deliver packages. Two ternary CAM types. Binary CAM Binary means that only two logical bits 0 and 1, three times 0, 1, and X (timeless bit) cam. Take, for example stored in a "101XX" It complements the four keys or "10100", "10101", "10110", "10111" when multiple answers resembles the input data is important to encode should choose a special them. Table I shows the structure of TCAM inputs.

The size of the header, you need to consider several algorithms classification. Let matches exact specific examples of suitable recipient of the size or the prefix matching sets a sand numbers. The software algorithms, flexible and low productivity maintenance of hardware systems, are a binary cam used to determine the exact game where TCAM used to mitigate the range or add matches. TCAM widely used as a binary CAM thanks to its ability to minimum bit. Timeless centered TCAM. The integrated recommendations (ASIC) designed for a doll called native CAM. They native doll has a few limitations.

TABLE I. FONT SIZES FOR PAPERS

Address	Ternary Data							
	HP1				HP2			
0	0	0	0	0	1	0	1	0
1	0	X	0	1	0	0	1	0
2	1	0	0	1	1	0	0	X
3	1	X	1	0	1	0	0	0
	HP3				HP4			
4	X	0	0	1	1	0	1	0
5	0	0	0	1	1	0	0	1
6	1	0	0	0	1	0	0	0
7	1	1	1	1	1	1	0	1

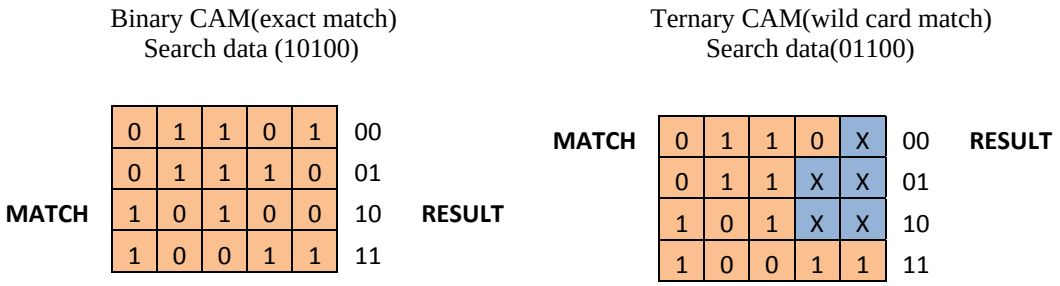


Fig.1.CAM vs TCAM

1. Since each bit required the match logic, the cost of per bit is high.

2.More Power consumption than RAMs due to match logic in every cell.

3.Native CAMs are absent in FPGA

Due to the above limitations,the more flexible and efficient method is required.RAM based CAM is introduced which gives the prominent technique among number of solutions.In this paper,we are proposing hierarchical finding techniques which will be more easy and high data rate transmission.In this technique,the entries are divided as high priorities such that priority entries are searched first is high priority .If the match doesnot found, then no further search will perform so, that the average power consumption is reduced.

II. RAM-BASED TCAM EMULATION TECHNIQUES ON FPGA REVIEW

Xilinx and Altera have been proposed techniqued to design RAM based CAM on FPGA [3],[4].The Literature study of this topic can be found in [1][2].We have a formula N*W TCAM,where N denotes number of TCAM words,W denotes width of each word.

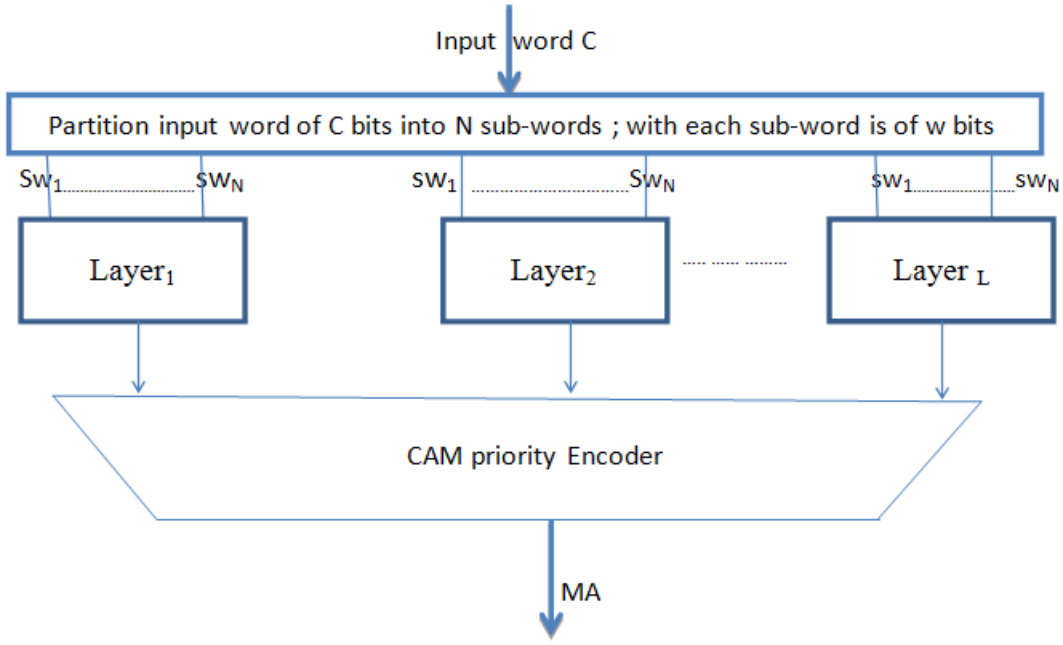


Fig.2. Basic structure of CAM

The main step of encoding preference to become the critical path. Several units of Fig.2 can be cascaded to form a processing architecture which is of parallel mechanism. Although [1] Jiang gave theoretical analysis W have TCAM * N, where N the TCAM TCAM building Ramsay and word parallel and scalable W shows the number of terms for each word width figure, the proposed architecture, the optimization method is not required (2 ^ W) * RAM Bits N to apply the same consumption Seeking. In his architecture, it is known for each block of the care and a hit or function, where w denotes the inlet valve that serves as the RAM addresses and the number of times each n-bit word size RAM. RAM requirement may be relaxed by dividing the key input W bit short in several key principles of equality, marked W. The total memory requirement

$$N * w = 2^w / w \quad (1)$$

In [1], the author observes and identifies an equation (1) is still a function of the memory requirements of minimally considered and W is obtained which is the smallest possible value such as 1 or 2. In fact, W generally have some value for a limited natural resources available. For example, the PGA is to use block RAM-memory W has a least value of 512, then if you are using distributed ram W has a minimum value of 32. The equation (1) means only a few small Ramsay equal depth used CAM application that requires less memory. However, each of the RAM word width depends on the specific application (for each word width corresponding to the depth of the RAM table CAM). Given the efficiency of the memory point, distributed RAM effectively block RAM implementation of TCAM because of its lower minimum depth. However, normally distributed RAM-memory has a small width and a large width is required by the application, a number of blocks allocated RAM should be connected in parallel. No matter what Ramsay used to apply TCAM

III. PROPOSED METHODOLOGY FOR VARIOUS RAM BASED ARCHITECTURES FOR TCAM

Follow the model [1], but we will use the data so that data is always looking paramount. Moreover, the past game red light block (thing) is used for lease priority blocks the signal, which means that if the defense is not final match because research research and, therefore, consumption of average power is reduced.

A. An Architecture of RAM Memory Block

RAM-memory can be configured in various ways, such as a RAM FPGA port, dual RAM and easy access to the latest dual-port RAM, the current list is only available to some Simple dual-port RAM. The match signal to reverse the past and continues to low priority port, as shown in Figure

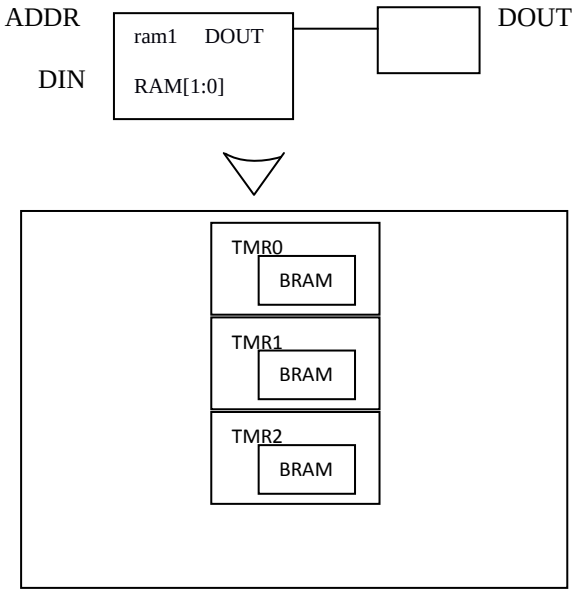


Fig.3. Basic RAM Architecture with I/O

B. Distribution Architecture RAM

RAM lookup tables is to use a distributor is available in all rooms, and the minimum size of the RAM memory of the overall size of the LUT. There is a built-in power, distributed RAM, so as to use the clock gating techniques ON / OFF of the RAM, as shown in Fig.3.

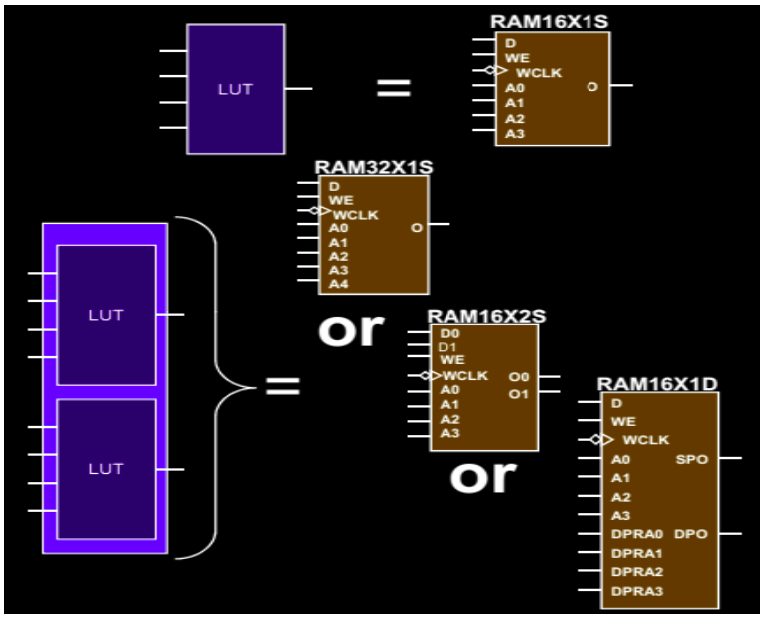
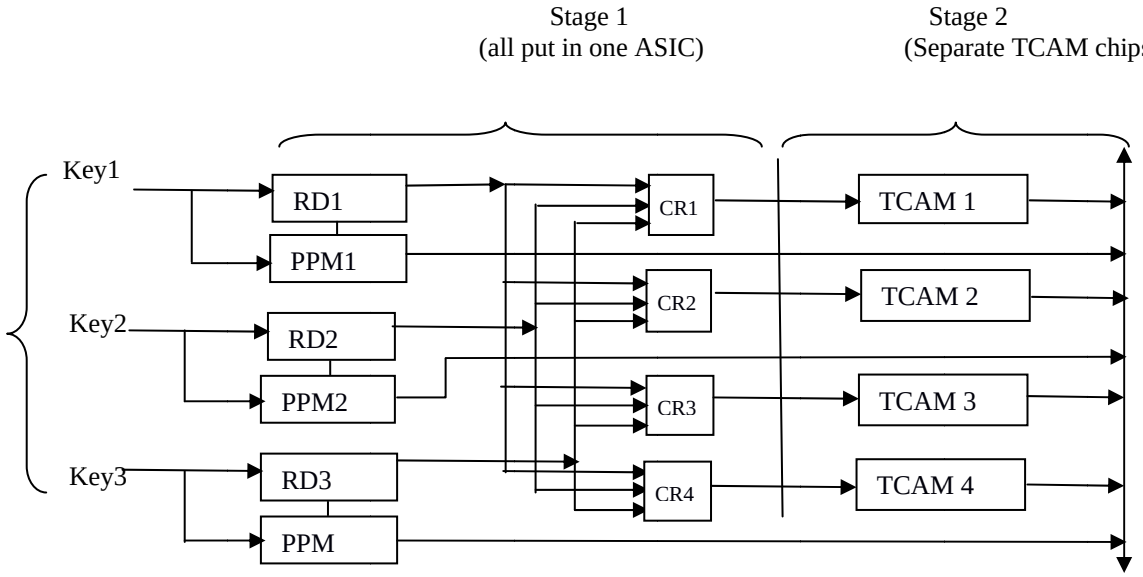


Fig .4.Distribution Architecture RAM

C. Parallel Architecture

Recently, more and more space in the parallel architecture, and progress will be possible by simply adjusting the platform for a number of [8] students. detailed architecture of the parallel TCAM-based emulation RAM [1]. We changed the architecture of our planning process and seek hierarchical structure shown in Fig. 4. Note that the performance of this architecture can be improved with the addition of pipeline stages of said units and each unit. It takes more important encoder (omitted in the figure) for the final selection stage.



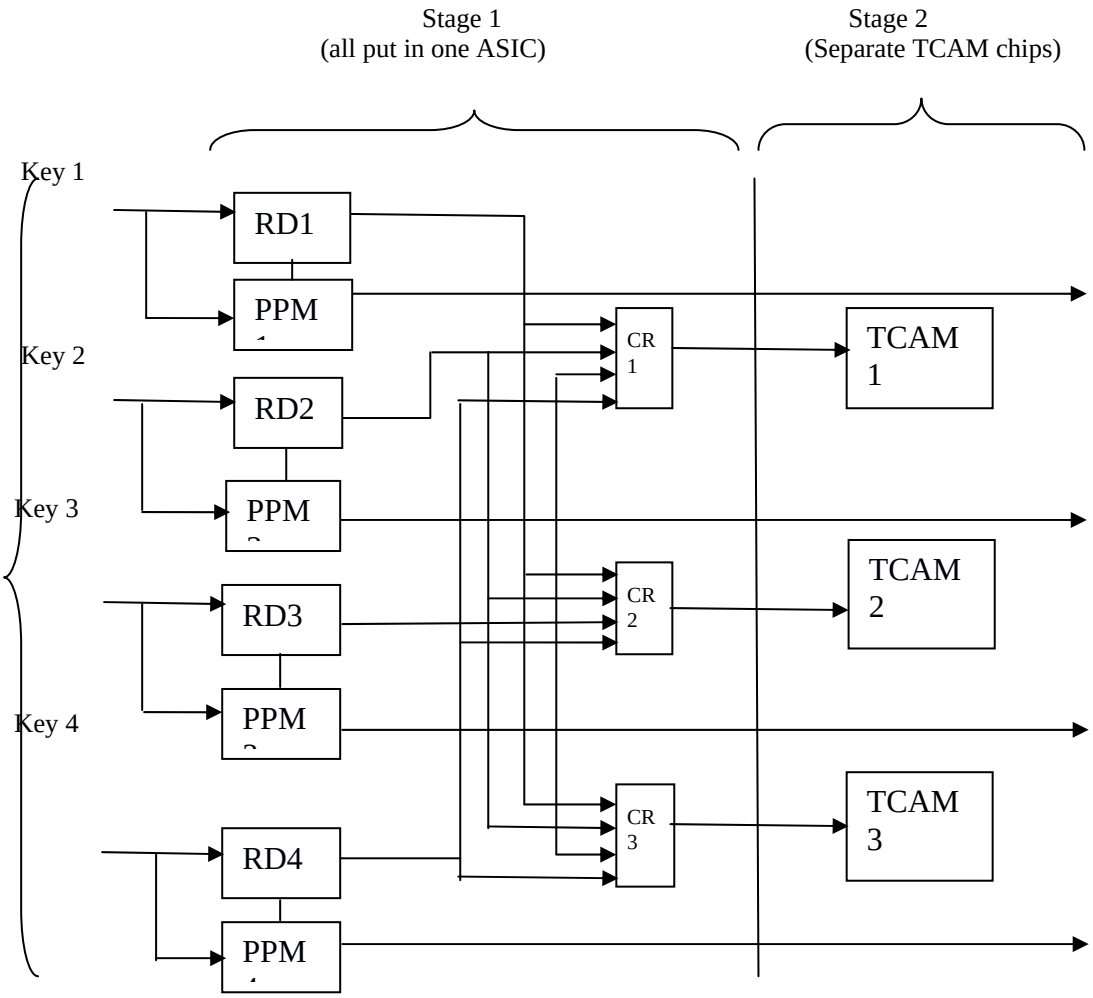


Fig.5. Parallel RAM- based Architecture

There are two types of RAM available FPGA block RAM and distributed. RAM blocks are often used to implement applications that require large amounts of memory capacity. distributor search RAM is to use tables (Lutz), which is available in all rooms. We conduct experiments Virtex6 XC6VLX75T Xilinx devices -3 degrees. We will publish the results on the basis of where and how the results of the Xilinx ISE 14.7. power. The results received from Xilinx Power Analyzer. In our experiments, we set the key input size 180-bit, if you select a line in figure 4, each tube of the device and the internal pipeline level for each unit. Each dual port RAM is configured in a port mode (SDP) and the second reading. While the other port RAM configurations are possible, for example, four doors are out of shape. In addition, we configure the width of each word, for example,72small.

IV. SIMULATION ANALYSIS

A. RAM-memory block Simulation

RAM FPGA Virtex6 each store up to 36Kb of small files which will be configured, 64Kb x 1 (block waterfall near 36 KB RAM), 1 x 32K, 16K x 2, 4 x 8 k, 4K x 2K x 9 18, 36 x 1 or 512 K x 72 simple dual-port mode. [5], to see the performance of the memory configuration of 512 x 72 experiments. If the draft 180-input bit support, RAM, 20 to a room. Virtex6 XC6VLX75T, 156 RAM. Therefore, it can be applied to the seventh level of target devices and the exact analysis is shown in below fig 5. Table II shows the simulation results.

TABLE II. Architecture Analysis Block RAM-memory

Block RAM Based Architecture(7 stages,140/156 block RAMs)	Maximum frequency (MHz)	Total power(watt)	Power saving Ratio
With Hierarchical Searching	133	2.548	11.0%
Without Hierarchical Searching	133	2.863	____

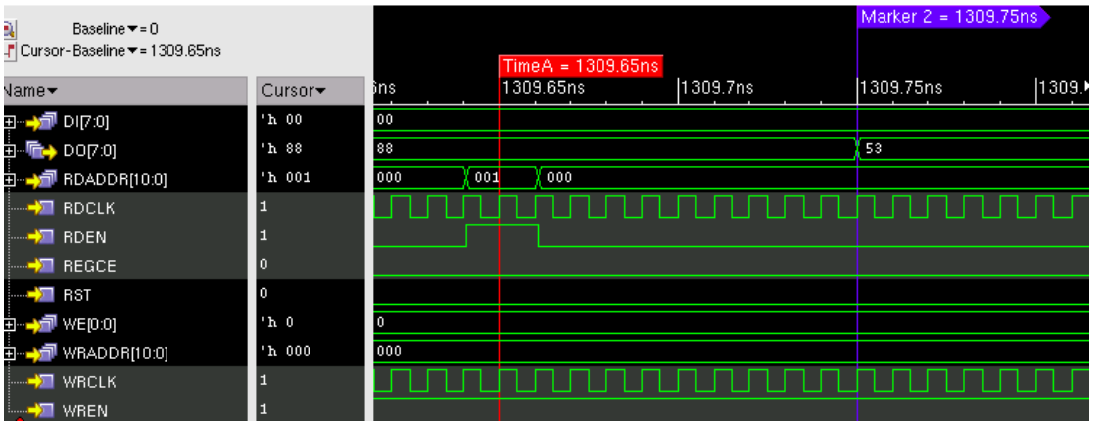


Fig: 6. Block RAM Architecture Analysis in Xlinix

B. *RAM distributed simulations*

Creating FPGA resources referred to slide the two types of Xilinx FPGA sliced, cut, and cut. RAM distributed only supported on wedges. A piece of four LUTs and, when used in distributed RAM, various methods available in the dual port Wikipedia x 32 6 and 3 x 64 [6]. In our tests, we chose 6 x 32-bit memory bus as the base memory. This block is located in the iris (4-LUT). If the project is to support 180-bit key input, it takes 36 RAM. But we want them basics such as 72-bit block RAM (same plane). Therefore, the full 36 x 12 RAM for each basic unit. Virtex 6 XC6VLX75T can 16720 LUT used or shared RAM. Where each unit is 36 x 12 x 4 LUTs can be used up to nine levels of the target device. Table III shows the simulation results.

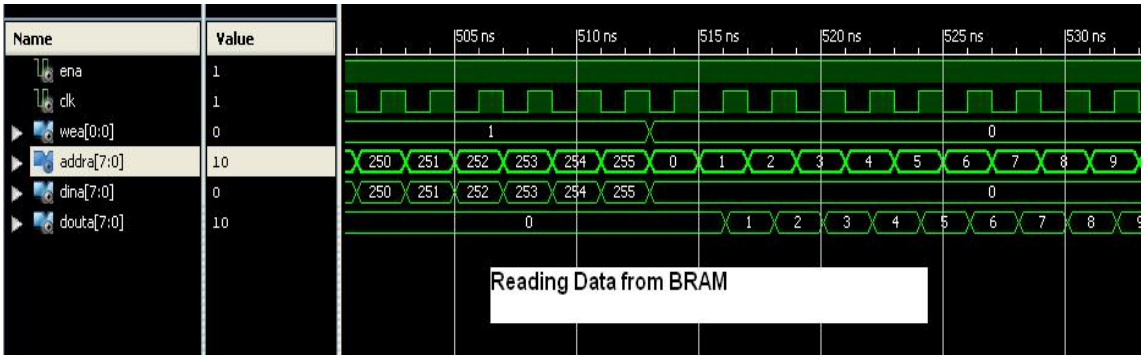


Fig 7. Distributed RAM-based simulation analysis with Xlinix

TABLE III. Simulation analysis of Distributed RAM-based architecture

Distributed RAM Based Architecture(9 stages,15552/16720 LUTs)	Maximum frequency (MHz)	Total power(watt)	Power saving Ratio
With Hierarchical Searching	109	2.388	9.7%
Without Hierarchical Searching	109	2.643	____

V. CONCLUSION

In this article, we introduce technology RAM-based architecture TCAM energy optimization suitable for use in FPGAs. We would not affect Critical Path Timeline and maintain the same maximum frequency. The first results show the benefits of our approach. In the future it will be the formation of hierarchical update engine of our design process. One of the advantages of our approach is the most important risk areas and low divorced, and then upgrade to the target area has no effect on other sectors. Another aspect of the current situation will take this type of configuration RAM. For example, if you use -chaw quad-port RAM, a port for writing and three other ports to read. Since many ports for loading, performance may be improved.

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