IMPLEMENTATION OF LOW-POWER FLIP-FLOPS USING C-ELEMENT

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Abstract: **To sustain expressive achievement of digital schemes, althoughcompressing the power expenditure, fulfilment of dual edge flip-flops receivesfreshly develops into the target of innumerable exploration. Powerful low-power flip-flops acquire district absolute fundamental elements gross sudden length of histrionic organizes succeeding circumferences/circuits. Individuallyconclude and impressivetesting as long as their exploit, Q-Delay, Path of the Rise time, Path of the fall time and Average Power Consumption. Whereas Power reveal smart effective count regarding transistors latest thing electrifying circuits, uncertainly we survive balancing including scheming comic number like transistors suspensefulthe each number of flip-flops. Analysis/inquiry about static/stable circuits go on spent throughDual Data Rate (DDR) using PTM CMOS-45nm Technology alongside 5MHZfrequencies including their victoryoperation. Sensationalconstruction regarding Dual Data Rate (DDR) Flip-Flop utilizes 30% fewercapacity/power, including 14% lower C-Q delay.**

Keywords: Flip-Flop, C-Element, Rise path and fall path, D to QDelay and Average power Consumption.

I. INTRODUCTION

Histrionicbetterextensive executionbenchmark current designing's systems on chips are to shorten range/area,delay and power dissipation. Flip-flop (F-F) obtain affecting primary storage elementpopular particularpipeline level. Enhancement movedesign fulljust as one of tense leading elements in VLSI design implementation[1]. In classification viaget a huge low power design and performance, consideration need obtain inclined to Flip-Flops [2]. Effective betterimportant element trendy today's VLSI technology system especially for lightweightdevice together with handled applications continue low power consumption [3]. Considering the clock setup involves 20–50% from affecting finish power, inclinationis appropriatedinto detail as one about effective power components. The obtaining connection of on chip power move dissipated over to clock system assembled of flip-flops and clock distribution networks [4,5]. Power expenditure and latency of flip-flops secure develop into main point of departure suchas facingfair low power fundamental and stable timing budget about devices [6]. Flip-Flops could be determined into two chains: master pulsed Flip-Flop and slave pulsed flip-flops. To dispense the negative time setup along withinto fair the low-power area of the Flip-Flops.Pulsed Flip-Flops we are introduced in different application areashence pulse generator (PG) as well as designed circuits are used one by one[7].

A collection of Flip-Flop structure designs into appropriate area low-power capable near high-performance appearance obtainanalysed in the indicated assignment. Popular modern years a paper popularizeda Flip-Flop is called High Speed Dualedge triggered Modified Hybrid Latch Flip-Flop (HSDMHLFF) to cultivate power consumption beyondcompressingpre-charged capacitance activity aspects.Modified Hybrid Latch Flip-Flop (MHLFF), ep-DCOFF, CDFF, SCCERFF, ep-DSFF and C-DDRFF discussed in below.Current achievement with the energetictesting of C element[8].

II. PROPOSED DESIGNED PULSED HYBRID FLIP-FLOPS

A. HSDMHL FLIP-FLOP

Facing obtain an impartial analogy likerealization/performance, a few of suspenseful better leading existing Flip-Flop designs continue analysed in this paper as well as illuminated latest"High speed dual edge triggered modified hybrid latch"(HSDMHLFF) presented in Fig. [1], invitation obtain a constructive pulsed double edge triggered Flip-Flop whose initial level have being exposed being generating few clock delay signals that continue inserted in impressive second level. Previously design fall off against additional switching activeness on dynamic node derive in more and more power consumptions mainly in low activity elements.

Supported the alternative extremity, appearing in powerful falling edge of clock (CLK), it require extra time to discharge owed to inverter's inactivity. Additionally 12 number of clocked transistors in this design, supplying a lot of power expenditure. [9,10].

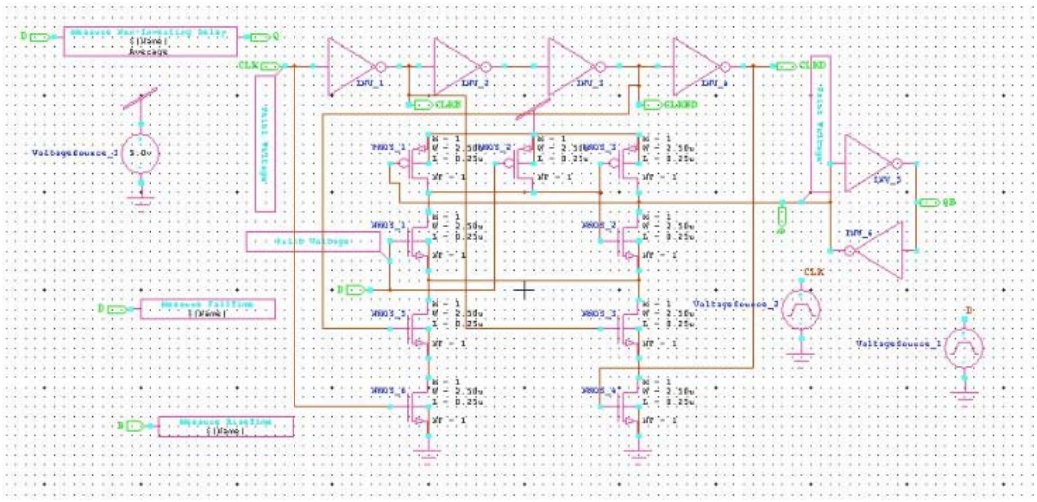

Fig: 1. Schematic of High speed dual edge triggered modified hybrid latch

B. MHL FLIP-FLOP

The "Modified Hybrid Latch Flip-Flop" (MHLFF) exposed in Fig. [2]. Again need a static latch/Flip-Flop. Emotionalkeeper logic appearing in node *X* lastremoved. A power less pull-up transistor MP1 (pMOS)is controlled to one side effective output signal Q controls the level of node *X*just as Q equals0. Even with individual circuit integrity, Essential"MHLFF" design encounters two defects. First defect is after all node *X* remain not pre-discharged, a extended 0 to 1 delay is conventional. Spectacular delay decline added, being a level-degraded clock (CLK) pulseremain applied into the discharging transistor MN3 (nMOS). Second defect is node *X* develop into floating in positive cases and owned value may drift creating more dc power [11]. Node Q at the time "1 to 0" data changes overs. Related among the Flip-Flopstructure used in Static-CDFF (SCDFF) structure, Impressive design savings of the proposed circuit combine a charge keeper devices (two Inverters), a pull-down network i.e., two nMOS transistors, and a supervision inverter. The unique extra component popularized subsist an nMOS pass transistor to device signal feedthrough. This arrangement indeed better the "0 to 1" delay along with as follows scale downs the gap between the rise path delay and the fall pathdelay.

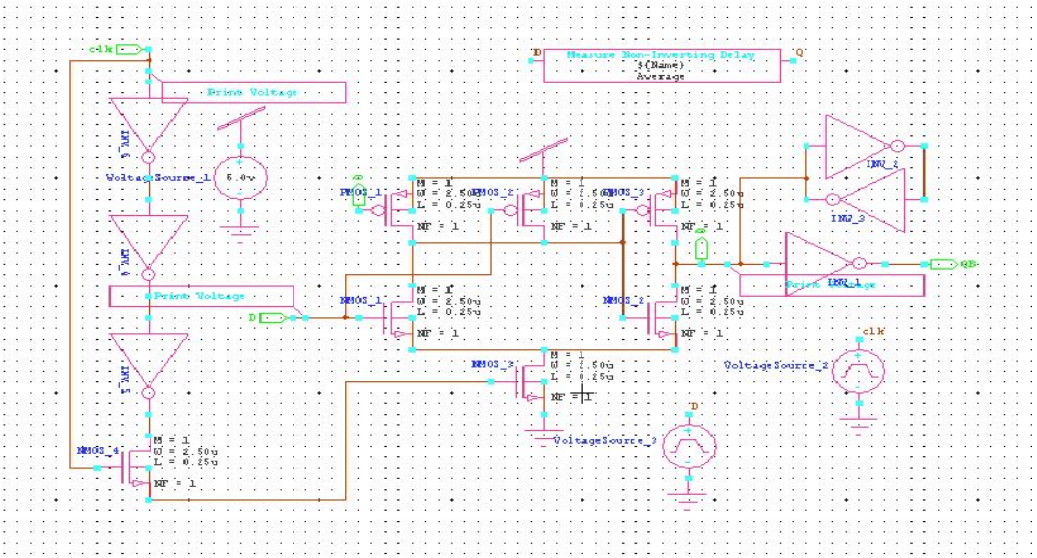

Fig: 2.Schematic of Modified Hybrid Latch Flip-Flop

C. ep-DCOFLIP-FLOP

Pulsed-Flip-Flops (P-FF) are charge of pulse generation, Package act classified just as an implicit type or an explicit type. Dashingan implicit type Pulsed-Flip-Flop, comic pulse generator is element of affecting Flip-Flop design as well as no explicit pulse signals are generated. Modern explicit type Pulsed-Flip-Flop, Electrifying pulse generator along with the Flip-Flop obtain isolated [12]. After generating pulse signals explicitly type, implicit type Pulsed-Flip-Flop remain inthing general extra power-efficient. Explicit pulse generation, Acquire higher power consumption however the logic separation against the Flip-Flop design provide the Flip-Flop design a solitary (Unique) speed advantage.

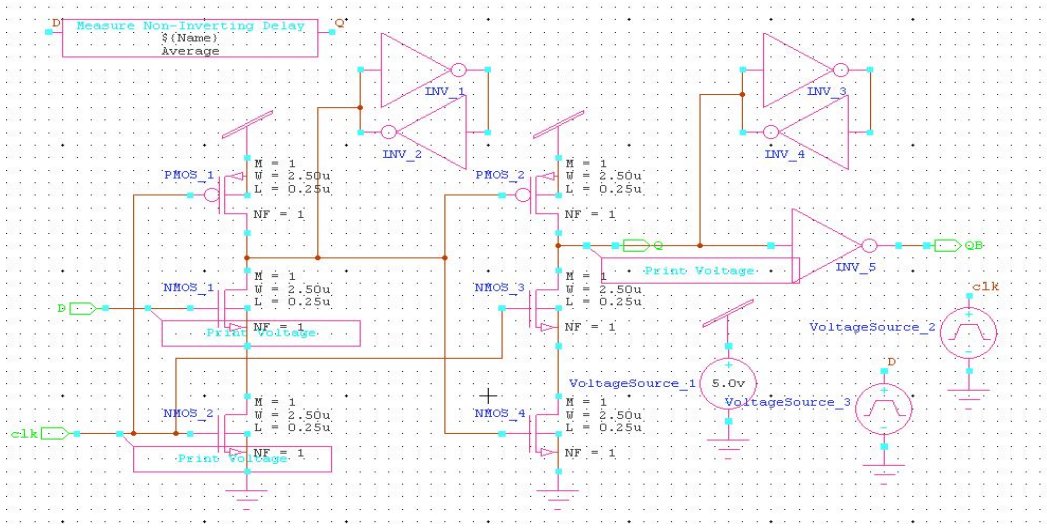

Fig: 3. Schematic of explicit Pulsed-Flip-Flop design, named data-closet o-output.

Particular power consumption along with the circuit complexity can continue effectively shortened in case that one pulse generator is shares a group of Flip-Flops. In Style here small, we passion in such away focus on the explicit type Pulsed-Flip-Flop designs only. A classic "explicit Pulsed-Flip-Flop design, named data-closet o-output" (ep-DCO) exposed in Fig. [3]. It consist of a NAND logic established pulse generator along with a semi dynamic True Single Phase Clock (TSPC) structured Flip-Flop design. Effective pulse width continue determined by the delay of three inverters. Previously design undergo from a serious defect, i.e., the internal node *X* is discharged on every rising path edge of the clock in enmity of expressive presence of a static input "1." The present gives rise path to high switching power dissipation. [13] – [15].

D. CD FLIP-FLOP

Electrifying "Conditional discharged Flip-Flop" (CD) technique display in Fig. [4],anextra transistor MN3 (nMOS) controlled over the output signal Q-fdbk continued employed unusually no discharge appear if expensive input data is remains "1." The keeper logic circuit as much as the internal node *X* is interpreted and repose of an inverter plus a pull-up pMOS transistor only. Normally the similar Pulsed Flip-Flop design (SCDFF) using a static conditional discharge technique [16]. Interestis qualify from the "CDFF'circuit design using a static latch/Flip-Flop structure. At that time node *X* is so exempted against periodical pre-charges. At the same time it exhibits a deep data D to Q delay than affecting CDFF design.

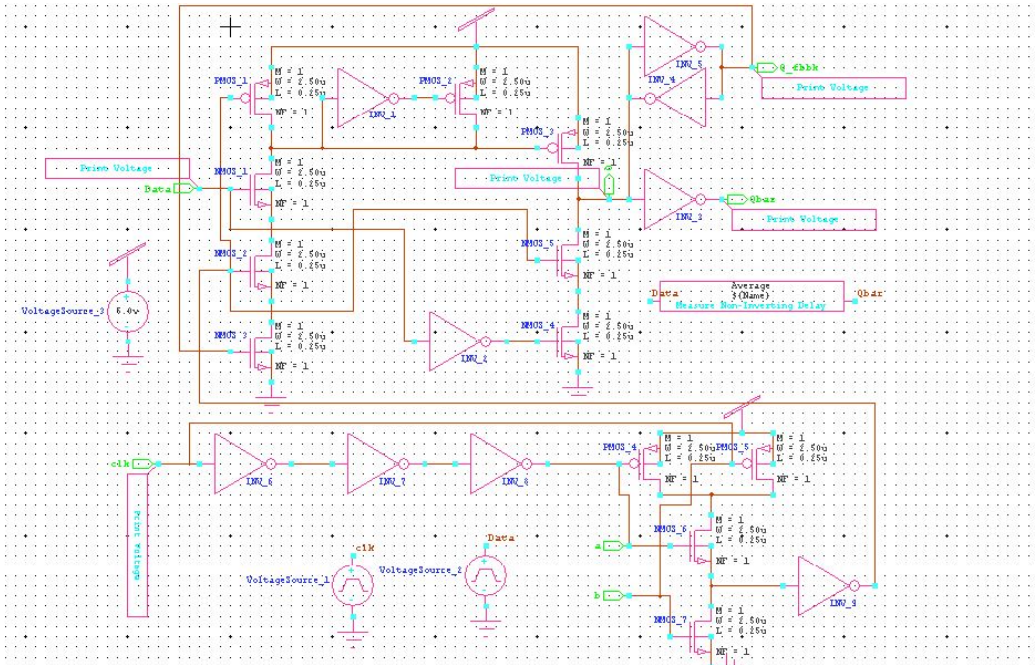

Fig. 4. Schematic of Conditional discharged Flip-Flop.

E. SCCERFLIP-FLOP

The design of "Single ended Conditional Capturing Energy Recovery Flip-Flop (SCCER)" exposed in Fig. [5]. This Flip-Flop act as an implicit pulse categorywhere transistor N3 is conditional to expressive output feedback plays role of limited capturing. Approaching the alternative hand, effective enabling a fall path output Q transition is designed and does not desire limited capturing. Pseudo nMOS logic correlate with first level turn to have low shortcircuit power dissipation. Data keeper in order that imposed a few limitations on here circuit is eliminated, whatever translates the data into a low parasitic capacitance at node X [17]. A just employed inverter I2 consider control of transistor N5 via connecting to its gate terminal. The pulse controlled discharging designed circuit is mutual by rise time and fall time output paths [18].

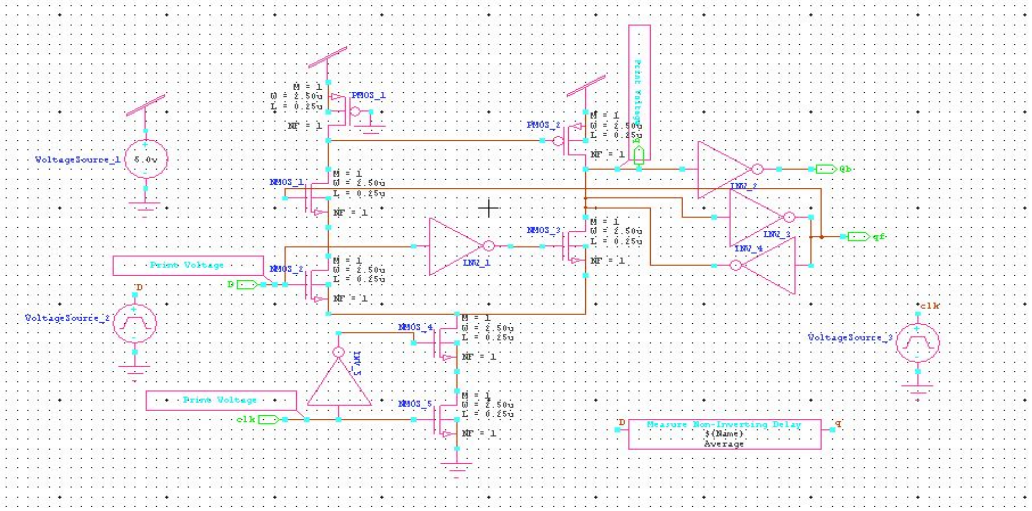

Fig: 5. Schematic of Single ended Conditional Capturing Energy Recovery Flip-Flop

III. DUAL DATA RATE FLIP-FLOPS

A. ep-DS FLIP-FLOP

Concede to analysis the "Explicit-pulsed static hybrid Flip-Flop (ep -DSFF)" acceptthe lowest (PDF) power delay product. Accordingly, in this analysispaper individually consider ep-DSFF at that time reference to analyzealong our new DDR Flip-Flop.

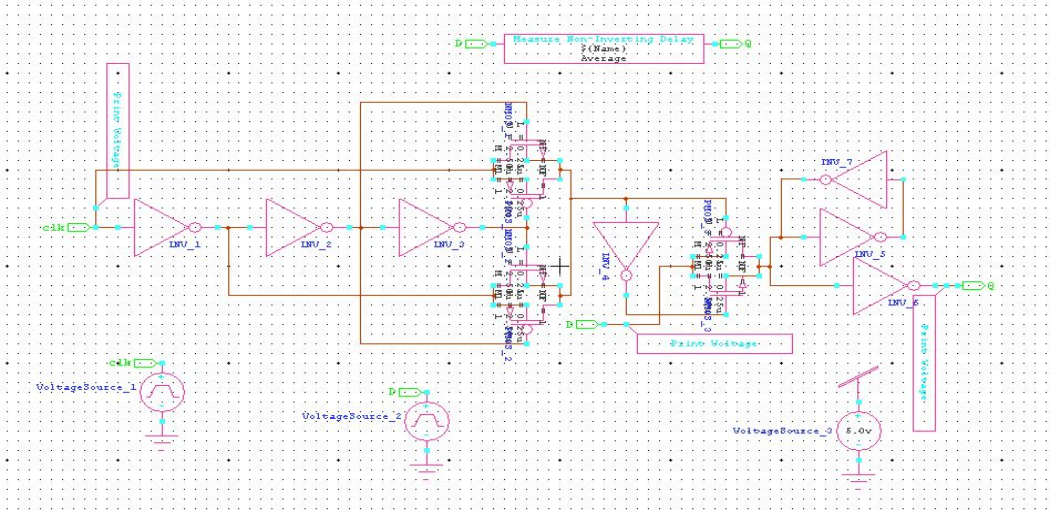

Fig: 6. Schematic of Explicit-pulsed Static Hybrid Flip-Flop.

Sensational ep-DSFF circuit is exhibited in Fig. [6], design be expressed by about an "explicit dual edge-triggered" pulse generator along with a simple great level triggered Flip-Flop circuit [19]. This pulse generator recycled in previously circuit can be local to each flop or shared among multiple flops. Considering the entire latch is not duplicated and area is relatively small, due to its explicit pulse generator, it increases the clock activity element and dynamic clock power consumption. Furthermore, the two transmission gates used in the pulse generator have a current contention problem, during clock transition. As well as the exposed input diffusion of impressive transmission gate at the input makes ep-DSFF affected to noise [20].

B. C-DDR FLIP-FLOP

Our advanced design technique is placed on splitting expressive sequential two latch structure used in a standard D flip-flop. i.e., "C-element based Dual Data Rate Flip-Flip" just as expressed in Fig. [8]. The outputs of expressive two latches continue when given to facing two inputs of the classic C-element [21], whichever past virtue of its operation, influences the present or require data until both effective inputs given to it inclined equal smart value. Already that two inputs given to the C-element to be equal at that time it acts as a simple inverter. The elemental operation and truth table of the C -element is presented in Table 1.

TABLE I. C-Element Truth Table

DATA INPUT	CLOCK INPUT	OUTPUT
0	0	1
1	1	0
0	1	Previous value
1	0	Previous value

Required Data input is given in parallel to both high level triggered and low level triggered latches. Hence allowing previously new Flip-Flop to be capture any transitions in determined input data during the entire clock period. After all the C-element stores the require data until both the latch outputs become equal, at the same time it includes both the storage and edge triggering attributes of a flip-flop, hence eliminated the require for any clock pulse generator is used in existing dual edge trigger Flip-Flops. In addition to that new C-DDR Flip-Flop has the same capacitive load on the clock network as a standard D flip-flop.

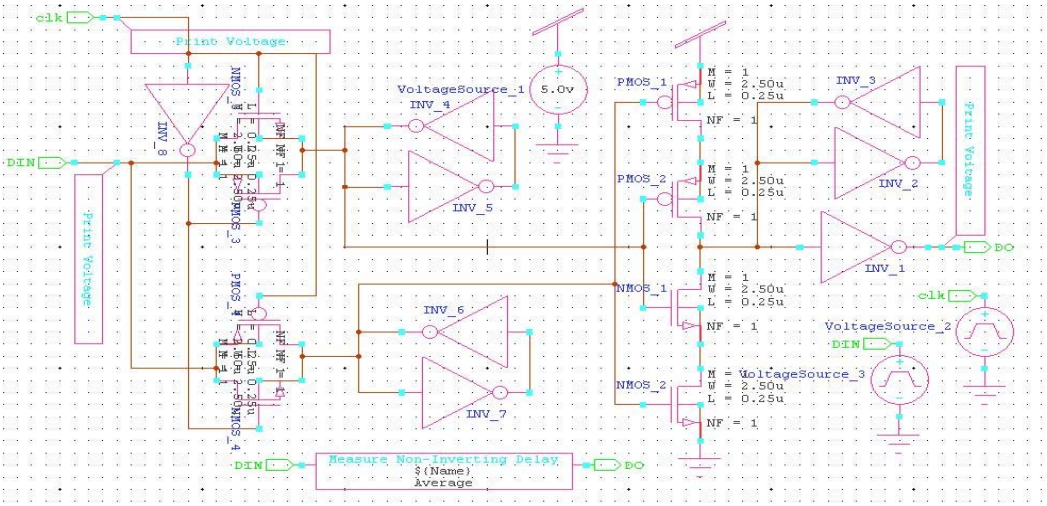

Fig: 7. Schematic of C-element based Dual Data Rate Flip-Flip.

First we keeps the output state of the C-element, like if there is an enormous leakage current passing through the C -element during the period when both the pull-up path and pull-down path of the C –element are push off. Again we keep second keeper also takes care of any charge sharing problem in order that might occur in case of the next stage is not isolated by static logic. In which the output buffer is used to prevent charge sharing problem at the output node of the C-element. In addition similar to ep-DSFF design is expressed in new C-DDR FF also has the exposed input dissipation of the transmission gate at the input, whichever overcome with an inverter at the data input. The expressive design of new C -DDRFF has also potentially better Single Event Upset (SEU) freedom than ep-DSFF.

IV. SIMULATION RESULTS

The TANNER SPICE simulations on Dual Data Rate Flip-Flop, ep-DSFFand more Flip Flops are performed using thePredictive Transistor Model (PTM_45_HK) in a 45nm metal gate high K dielectric CMOS technology, with the supply voltage of 0.5V. The designs were enhance for a 5 MHz clock frequency and data switching activity equal to 0.5. Because transistor sizing was upgrade using a constant procedure with the equitable of perform high speed and low power. Table II and III display the count of the transistors calculation of all considered Flip-Flops. Correlated and plotting graphs between the Power Vs VDD is expressed in Fig. [8], Delay Vs Frequency is also expressed in Fig. [10], the Dual Data Rate (DDR) Flip-Flop utilizes 30% fewer capacity/power, including 14% lower C-Q delay.

TABLE II. COMPARISON OF DIFFERENT FLIP-FLOP DESIGNS

Flip-Flop Design	HSDMHLFF	MHLFF	ep-DCOFF	CDFF	SCCERFF
Number of Transistors	21	19	28	30	17
D to Q-Delay	-1.21659e-004	-3.043e-001	-1.7495e-004	2.2495e-001	4.1760e-002
Average Power	3.4250e-002	3.0749e-001	3.1358e-001	3.0062e-002	2.9861e-002
Maximum Frequency	5MHZ	5MHZ	5MHZ	5MHZ	5MHZ
Raise Time	4.0000e-009	4.0000e-009	4.0000e-009	4.0000e-009	4.0000e-009
Fall Time	3.0000e-009	3.6503 e-007	7.6086 e-010	3.0953 e-001	2.1056 e-007

TABLE III. COMPARISON OF DIFFERENT DUAL DATA RATE FLIP-FLOP DESIGNS

Flip-Flop Design	ep-DSFF	C-DDRFF
Number of Transistors	20	24
D to Q-Delay	2.2086e-002	1.6973e-004
Average Power	3.5826e-002	2.5430e-002
Maximum Frequency	5MHZ	5MHZ
Raise Time	4.0000e-009	4.0000e-009
Fall Time	3.0500 e-010	4.3281 e-009

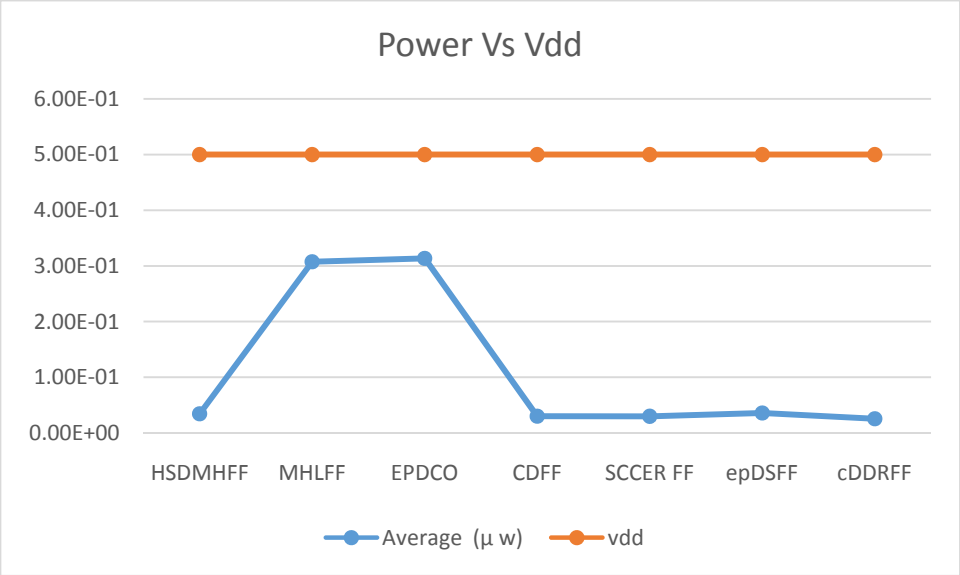

Fig: 8.Performance of Power dissipation VDD.

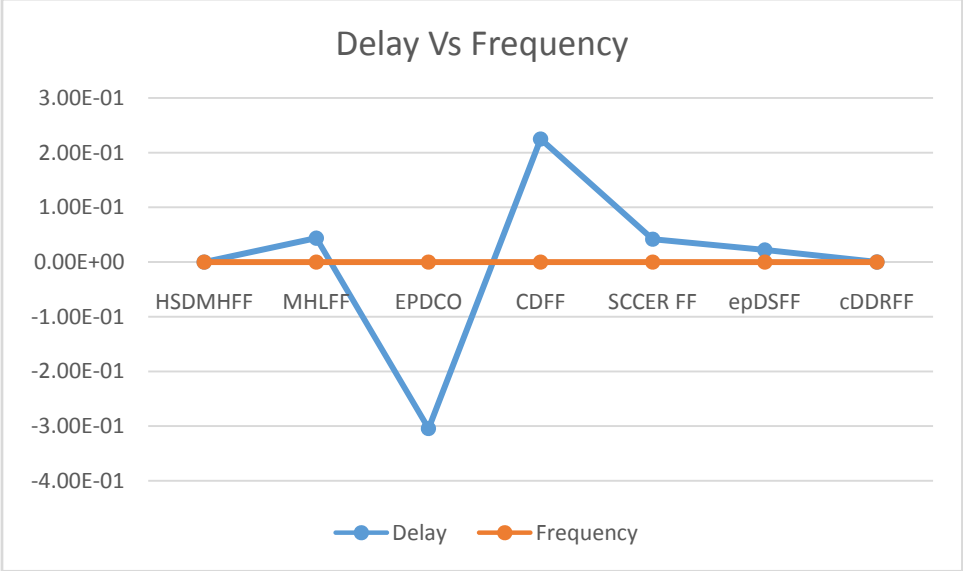

Fig: 9.Performance of Delay versus frequency.

V. CONCLUSION

In this paper, an advanced Implicit Pulse Triggered Flip-Flops obtain granted, and that is a hybrid pulsedtype Flip-Flops. Hence Capable only four clocked transistors whichever results in important power saving. Impressive key idea to be using of a C-element as long asthat two input signals obtain to provide along input data and common node of two series pass transistors. According, the every correct value of output was obtained and controlled by anelementary/simple latch. All required Flip-Flops were designed in 45 nm technology, and experimental results exposed so that the average power consumption in 30% data activity and that required delays are also 15% and 10%, respectively. Contemporaryof all process intersections, it includepreferable (PDP) Power Delay Product saving.

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