

# ZigBee Based Wireless Data Transmission with LDPC codes using FPGA

M.Ushaswini Chowdary<sup>\*1</sup>, B.Murali Krishna<sup>2</sup>, K.S.N.Murthy<sup>3</sup>, G.L.Madhumati<sup>4</sup>, Habibulla Khan<sup>5</sup>

<sup>\*1</sup>PG Student Department of ECE , K.L.University Green fields-522502,AP,India  
ushaswinichowdary.6@gmail.com

<sup>2</sup>Assistant Professor Department of ECE , K.L.University Green fields-522502, AP,India  
muralikrishna@kluniversity.in

<sup>3,5</sup> Professor Department of ECE, K.L.University Green fields-522502, AP,India.

<sup>4</sup> Professor & H.O.D Department of ECE, DIET, AP, India

**ABSTRACT**-Due to advancements in wireless communication, data transmission through noisy channel demands some efficient coding techniques. A Low Density Parity Check (LDPC) code performs dependable exchange of data over a noisy channel through long distances. LDPC code is basically a linear forward error correcting code. Error detection and correction in the decoder without any additional circuitry is the key component. In this paper 3 bit LDPC code encoder and decoder is designed in Verilog HDL synthesized in Xilinx and implemented on Spartan3E FPGA. ZigBee is interfaced with FPGA to transmit data in wireless between transmitter and receiver through media.

**Key Words** :-LDPC code, ZigBee, Spartan3E FPGA, Error detection and correction.

## I. INTRODUCTION

In coding theory with increased applications in computer science and telecommunications, error detection and correction techniques allows dependable data transfer over uncertain channels.LDPC code is one of the linear error correcting codes that transmits data over a noisy channel. LDPC codes consumes more hardware complexity compared to conventional error detecting and correcting codes. Turbo codes came into existence to replace these LDPC codes. Later in 1990's with the invention of parity check matrix by two scientists Mackay & Neal, LDPC code is considered to be efficient to Turbo codes in terms of high code rate and error floor. LDPC codes gained an immense popularity due to the error correcting capability nature and parallel decoding procedure in the decoder. These codes have a number of real life applications such as magnetic storage, 10 GB Ethernet, and high-throughput wireless local area network.

LDPC code stands for Low Density Parity Check code is a linear block code and also a forward error correcting code. The name low density indicates the number of 1's in the parity check matrix.If the 1's in the parity check matrix follows certain rules such as  $W_c \ll m$  and  $W_r \ll n$  , where  $W_c$  represents the column weight,  $W_r$  represents the row weight ,m represents number of rows and n represents number of columns [2],it is the case of regular LDPC codes where as no rules are followed in irregular LDPC codes. In regular parity check matrix the number of 1's in rows and columns will be the same satisfying the condition mentioned and in case of irregular parity check matrix the number of 1's in the rows and columns will not be the same [3]. Once the number of 1's in the parity check matrix is constant then the complexity in the decoder increases with only increase in the code word length.

## II. LDPC Encoder – Decoder

The encoding and decoding of the message vector using LDPC code requires two matrices, one is the parity check matrix (H) and the other is the generator matrix (G).Parity check matrix is used in decoding section where as generator matrix is used at encoding section. The matrices not only help in encoding and decoding procedures but also in the detection and correction of errors during data transmission. The number of rows in parity check matrix indicates the check nodes and number of columns indicates the variable nodes in the Tanner graph which is a pictorial representation of working of LDPC code. The block diagram shown in fig 1 consists of an encoder and a decoder connected through a channel. The information or the data to be transmitted is given as the data input which will be encoded in the LDPC encoder and the data will be sent to the decoder through a noisy channel due to

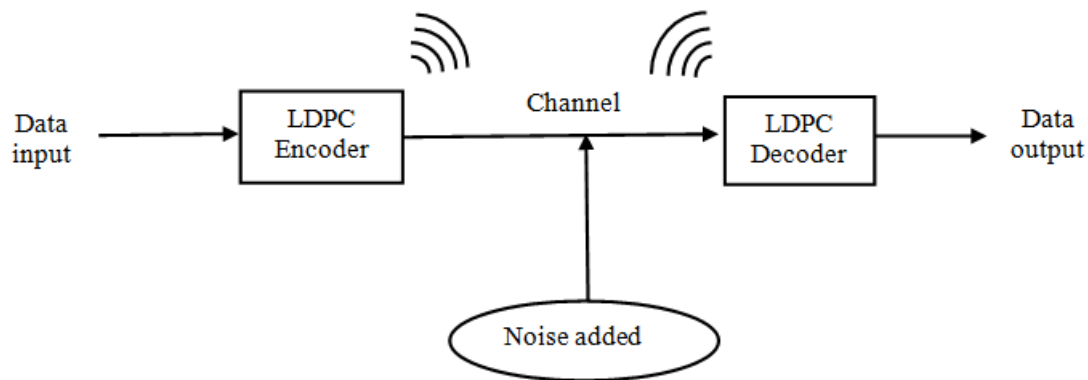


Fig1: LDPC System Architecture

which the encoded message is tampered. The decoder has to correct the encoded output which is an error (noise added in channel during transmission) due to the noisy channel.

The representation of an LDPC code starts with the representation of a parity check matrix with dimensions  $n \times m$  for a (8, 4) code which is shown in fig 2. The parity check matrix defined is a regular parity check matrix (H-Matrix) as it satisfies the conditions  $W_c \ll m$  and  $W_r \ll n$ .

$$H = \begin{pmatrix} 0 & 1 & 0 & 1 & 1 & 0 & 0 & 1 \\ 1 & 1 & 1 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 1 & 1 & 1 \\ 1 & 0 & 0 & 1 & 1 & 0 & 1 & 0 \end{pmatrix}$$

Fig 2: H Matrix

The parity check matrix can also be represented in terms of the Tanner graph as shown in fig 3. The Tanner graph is a graphical representation of a parity check matrix which is the key component in defining the LDPC codes. Here  $R_1, R_2, R_3, R_4$  indicates the rows of a parity check matrix called as check nodes and  $C_1, C_2, C_3, C_4, C_5, C_6, C_7, C_8$  represent the columns called as variable nodes. The degree of check nodes and variable nodes are random corresponding to the parity check matrix and is not advisable for linear programming decoding[5]. The representation of an H-matrix is generally in the form

$$H = [A \mid I_{n-k}] \longrightarrow (1)$$

As the H-matrix and the Generator matrix (G-Matrix) are inter related the G-matrix representation is in the form

$$G = [I_k \mid A^T] \longrightarrow (2)$$

Where A is  $(n-k) \times k$  matrix and  $I_{n-k}$  is an identity matrix of size n-k. The generator matrix thus obtained will be used in the encoding of information. The order of the parity check matrix is  $M \times N$ , where N is the code word length and  $M = N - K$  where K is the length of the information bit. The generator matrix G is obtained in such a way that it will be orthogonal to the parity check matrix,

$$G * H^T = 0 \longrightarrow (3)$$

The Tanner graph representation shown in fig 3 is a clear representation of LDPC codes which can explain the encoding as well as decoding process.

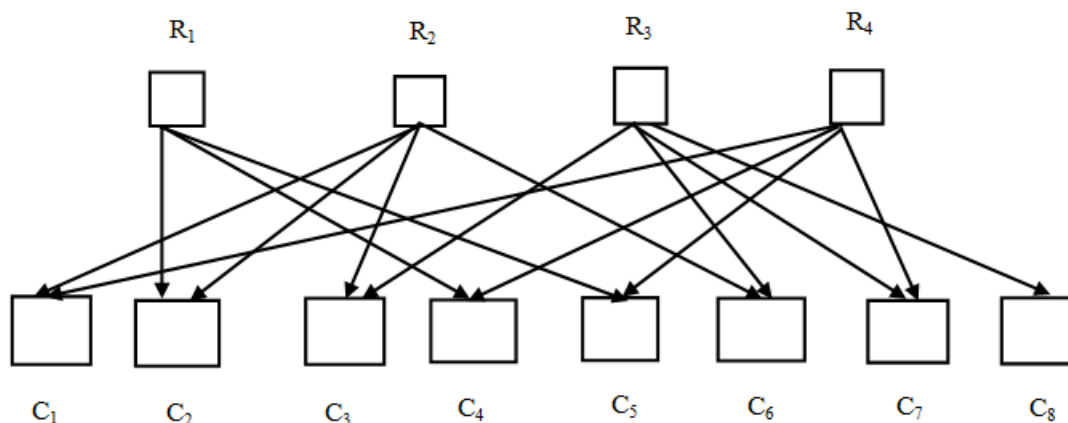


Fig 3: Tanner graph representation of the (8,4) parity check Matrix

### III. LDPC Algorithm

The information bit that is to be transmitted is  $U$  of size  $K$ . In the encoder a code word  $C$  will be obtained as output

$$C=UG \longrightarrow (4)$$

In this algorithm  $G$  is the generator matrix. The condition to be satisfied for the generated code word to be valid is

$$HC^T=0 \longrightarrow (5)$$

$H$  represents the parity check matrix. If the condition is not satisfied, it implies the presence of error in the code word generated and it needs to be corrected accordingly. A vector is used for the correction of such errors known as Syndrome and this method of error correction is known as Bit Flipping method. The syndrome vector is given by

$$S=HY^T \longrightarrow (6)$$

$Y$  is the invalid code word. The syndrome determines the row that is not a zero in  $Y$  and the corresponding correction will be done in the decoder. If the size of the parity check matrix taken is small, the error floor may be low or it is close to zero or it may be zero.

### IV. LDPC Architecture

#### A. LDPC Encoder

The LDPC encoder uses a generator matrix for the encoding of the information bit to generate a valid code word. Both the generator matrix and parity check matrix are co-related to each other as the parity check matrix indirectly defines the generator matrix.

$$H = \begin{pmatrix} 1 & 1 & 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 & 1 \\ 1 & 0 & 0 & 1 & 1 & 1 \end{pmatrix}$$

Fig 4: Irregular H-matrix

For a given parity check matrix, a generator matrix is obtained from H-Matrix using Gaussian elimination method. The parity check matrix initially taken is an irregular matrix and each one of the column represents one of the bit in the resulting code word and each one of the row represent a parity check constraint. The parity matrix of the irregular form is shown in fig 4. The standard form of parity check matrix will be derived from the initial irregular parity check matrix taken and is in the form  $H = [A | I_{n-k}]$ .

$$H = \begin{pmatrix} 1 & 1 & 1 & 1 & 0 & 0 \\ 0 & 1 & 1 & 0 & 1 & 0 \\ 1 & 1 & 0 & 0 & 0 & 1 \end{pmatrix}$$

Fig 5: Standard H-matrix

The Generator matrix will be obtained from the the irregular matrix by applying elementary transformations (swapping of two rows, adding of one row with the other using modulo two etc). The Generator matrix of the standard form  $G = [I_k | A^T]$  is shown in fig 6.

$$G = \begin{pmatrix} 1 & 0 & 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 1 & 1 \\ 0 & 0 & 1 & 1 & 1 & 0 \end{pmatrix}$$

Fig 6: Generator matrix

The resulting code word for the original information bit U is obtained by multiplying U with the generator matrix G that is C=UG. The block diagram that describes the encoding procedure is shown in fig 7.  $G_{(0,1,\dots,m-1)0,\dots,15}$  are the XOR operations performed by the encoder on the input information data, each row performs an XOR operation on the corresponding bit of information data and the resultant code word will be of the size 2K.

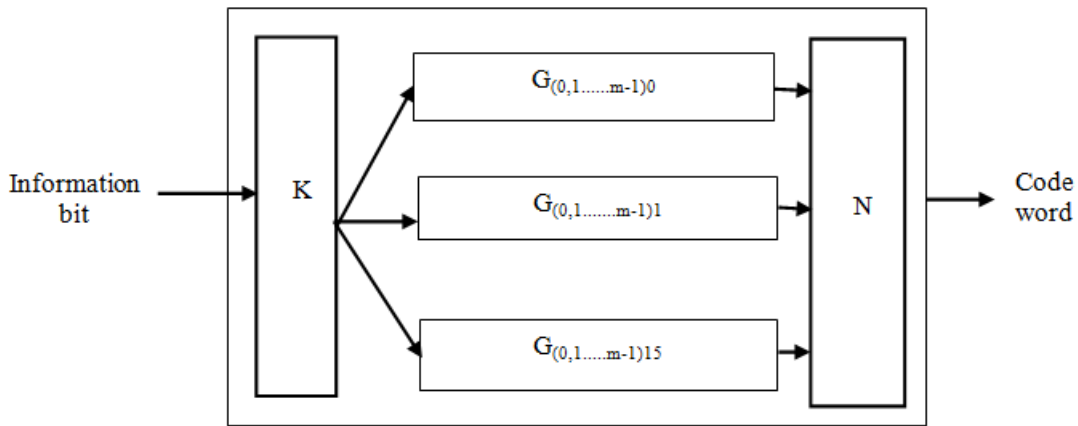


Fig 7 : LDPC Encoder

For a given 3 bit information data, the process of encoding based on the above block diagram is shown in fig 8. The information bit which is  $U=[110]$  is multiplied with generator matrix to obtain the code word.

$$\begin{pmatrix} 1 & 1 & 0 \end{pmatrix} \begin{pmatrix} 1 & 0 & 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 1 & 1 \\ 0 & 0 & 1 & 1 & 1 & 0 \end{pmatrix} = \begin{pmatrix} 1 & 1 & 0 & 0 & 1 & 0 \end{pmatrix}$$

Fig 8: Code Word Generation

On multiplying a 3 bit input information data with a corresponding sized generator matrix the resulting code word will be of size 2K i.e 6 bit code word.

**B. Channel**

The channel plays a major role in the transmission of data in wireless communication. When the encoded signals are transmitted through a channel, they get affected by the noise in the channel. The noise in the channel is considered as the additive white noise which is the basic type of noise added to the information when passing through the channel. It is uniform throughout the band of frequency.

**C. LDPC decoder**

LDPC decoder design follows joint design approach with parity check matrix divided into blocks with each block equal to zero or identity matrix with permutations done [6]-[10]. Among different techniques available for LDPC decoding hard decision decoding and soft decision decoding techniques are widely used. There are many algorithms used to decode the LDPC codes. The types of techniques to be used are based on complexities for different types of codes. Hard decision decoding starts with the parity check done by the check nodes to find the error based on odd or even parity. The message data is transmitted to the check nodes from the variable nodes, the check nodes verify whether the parity is satisfied based on number of 1's. If the parity is satisfied it re-sends the same message to the message node or else it flips the bits in the received data stream, to satisfy the parity and sends the new message back to the message nodes. Bit flipping algorithm is an example for the hard decision decoding technique. An alternative technique for the hard decision decoding is the soft decision decoding. Sum product algorithm is an example for soft decision decoding.

**a) Bit Flipping Algorithm**

This paper proposes a 3 bit LDPC code decoder designed using hard decision decoding technique with bit flipping algorithm. The input data is passed along the edges of a Tanner graph. The check node receives a message from the corresponding variable nodes representing the bit to be 1 or 0 based on parity. Each of the

check nodes receives the similar message from the variable nodes. All the check nodes verifies the data received from the variable nodes is according to the parity. The result will be zero if the parity equations are satisfied else it indicates the presence of error. The bit will be flipped and sent back to the respective variable node. Similarly each variable node receives number of bits. The variable node verifies and using the majority check operation, corrects the bit among all other bits received. If the result of majority check is zero then the bit will be the initial bit ,else the bit will be flipped. The process will be cycled until all the parity equations are satisfied and a valid code word is obtained as a result. The bit flipping algorithm has two advantages. One with the detection of valid code word the loop will be halted. Another with detection of code word can be known in advance.

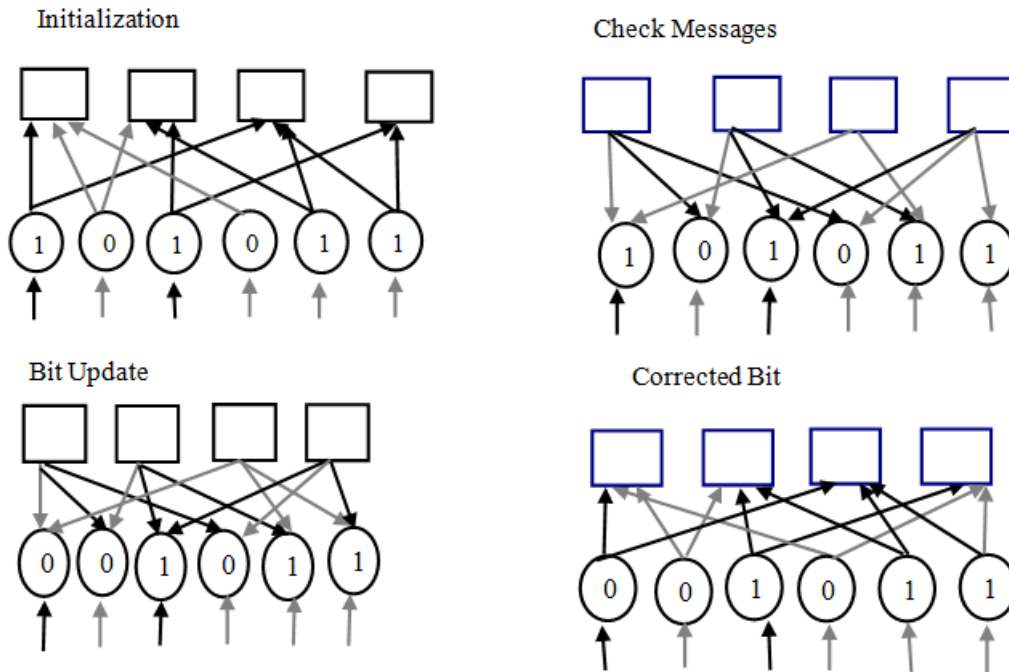


Fig 9: Bit Flipping Representation

The verification of code word for validity can be done using syndrome  $(S=HY^T)$ . Y be the decoded code word. If the syndrome is zero then the decoded code word will be the same as the encoded code word as shown in fig 9. If the result is non zero the code word decoded is not a valid code word.

$$S=HY^T = \begin{pmatrix} 1 & 1 & 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 & 1 \\ 1 & 0 & 0 & 1 & 1 & 0 \end{pmatrix} \begin{pmatrix} 1 \\ 1 \\ 0 \\ 0 \\ 1 \\ 0 \end{pmatrix} = \begin{pmatrix} 0 \\ 0 \\ 0 \end{pmatrix}$$

Fig 10 : Syndrome Calculation

The non zero vector in the syndrome indicates the error in the corresponding row of the decoded code word (Y). The parity equations will be verified and necessary bit flipping will be done to correct the respective bit. The process will be repeated until a valid code word is obtained as a result.

**V. Results**

The information bit 101 is encoded to form a code word 101011 and the same message is decoded with syndrome vector zero representing zero error and the same information bit is obtained as result which shown in fig11.

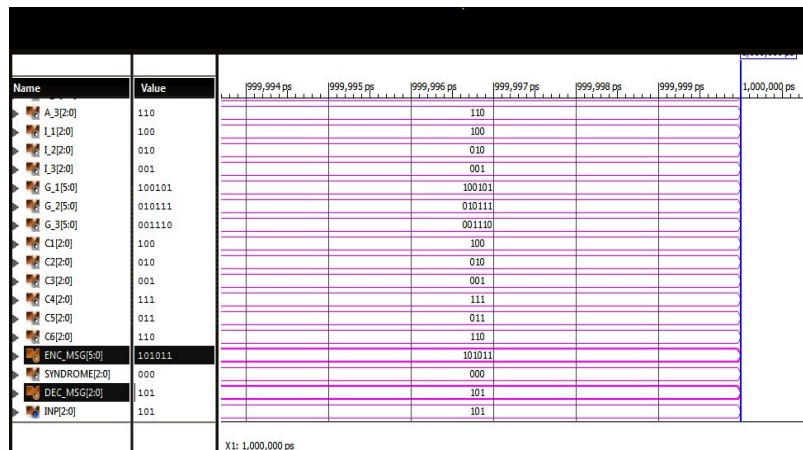


Fig 11: Encoding and decoding with Zero error



Fig 12: Encoding and decoding with error

Fig 12 shows the encoding and decoding results with non zero syndrome vector. The input information bit 111 is encoded to obtain a code word 111100. The encoded message on transmitting it to a decoder has an error in third bit position represented by err\_enc msg. The error will be corrected by the algorithm in the decoder and the correct encoded bit is obtained as a result in crtd\_msg. The final result 111 is obtained as the decoded output with both error detection and correction.



Fig 13: Zigbee interfacing of LDPC code

The LDPC code on simulating with the verilog HDL is interfaced with a Zigbee network to verify the data transmission. Fig 13 shows the data transmission with error detection and correction. E in the figure indicates the presence of error and the error is corrected. The data is transmitted with error detection and correction and the input data is obtained as the final output.

Table I: Device Utilization Summary

<b>DEVICE UTILISATION SUMMARY</b>			
<b>LOGIC UTILISATION</b>	<b>USED</b>	<b>AVAILABLE</b>	<b>UTILISATION</b>
Number of Slice Latches	7	9312	1%
Number of 4 input LUT's	13	9312	1%
Number of occupied Slices	7	4656	1%
Number of Slices containing only relative logic	7	7	100%
Number of Slices containing unrelated logic	0	7	0%
Total Number of 4 input LUT's	13	9312	1%
Number of Bonded IOB's	157	232	67%
IOB Latches	2		
Number of BUFGMUX's	1	24	4%
Average Fan out of Non Clock Nets	3.82		

The device utilization summary indicates the resources used by the LDPC code in encoding, decoding, error detection and correction within the resources available.

## VI. Conclusion

This paper presents a 3 bit LDPC codes. Encoder is designed with generator matrix and decoder with Bit-flipping technique. LDPC codes is implemented in Xilinx using Verilog HDL, simulated in ISIM. Design is targeted and verified on Spartan 3E FPGA. ZigBee Module is interfaced with FPGA for low cost, low power short range data transmission. 3 Bit LDPC codes is considered in view of FPGA and ZigBee GPIO's. It can be implemented for high bit rates like 16, 32 bit and 64 bit.

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## Author Profile

Muppalla Ushaswini Chowdary is pursuing M. Tech VLSI Design in K L University. Her research interests include FPGA Implementation, Low Power VLSI and Testing for VLSI Circuits.

B.Murali Krishna is working as Assistant Professor in K L University. His research interest focuses on FPGA implementation, Partial Reconfiguration, and Testing of VLSI circuits.

K.S.N.Murthy is working as professor in K L University. His research interest focuses on MEMS, Electronic Instrumentation

Dr. G.L.Madhumati presently working as Professor & Head, Department of the ECE at Dhanekula Institute of Engineering & Technology. Her research interested areas includes FPGA Implementation, Low Power VLSI.

Dr. Habibullah khan presently working as Professor & Dean (SA), Department of the ECE at K L University. His research interested areas includes Antenna system designing, microwave engineering, Electromagnetic and RF system designing.