Implementation of Video-Processing and Control on a Zynq Soc Platform

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***Abstract*— This paper represents a hardware and software co-design for real-time video processing module which is a vital part of a smart camera system [1-3]. Video surveillance is the main application of this work. As part of implementation required peripherals, the platform contains a Zynq board device and the OV7670 camera module. In order to develop the required hardware and software co-design in an integrated fashion, Xilinx VIVADO 15.2 and SDK 15.2 is used. To implement the real-time motion picture capture and display functionality of the camera module, OV7670 camera and a VGA monitor have been interfaced with the Zynq platform. This interfacing uses p mod connectors and VGA connector on the Zynq board. The programmable logic is done using the VHDL coding. The application software, written in C language, runs on top of a hardware platform which is opted as standalone in the SDK and uses the provided application programmer interface (API) by the hardware platform. From the device utilization summary, we can observe that, with the proposed hardware and software co-design based video acquisition module, are sufficient for implementing any reasonably complex video processing application in real-time.**

Keyword - Hardware Software Co-Design, Zynq-7000SoC, Embedded Video Processing.

I. INTRODUCTION

Due to the progression of the programmable logic devices has motivated the availability of an increasing set of low-cost development boards such as Zed Board, based on Avnet Zynq-7000 family of devices, which are a combination of the hardware and the software. The overall input/output capability is on a single silicon Integrated circuit. For Development of different application domains in the embedded system we use this kind of devices as the basic elements which gives the advantages like versatility, increased computational speed and opportunity to connect to sensors, actuators or input/output peripherals.

The application introduced recently reveals the necessity to capture and process the image sequences. There are different stages of video processing such as capturing the image from the outer sensor writing it to the memory, data processing of the memory information, visualization of the results to establish processing options for user interaction with control application.

Basically, there are two alternatives for development of video processing systems on the reconfigurable platforms. In that software approach consists of software instruction execution in an embedded processor system. In this high computational capability achieved as many development libraries available for optimized efficient execution [4-5].

On the other hand, algorithms based on hardware acceleration which allows the processor capability outperforming by using custom-designed electronic components for the implementation of specific tasks. In some previous works this approach related to hardware implementation of video processing has been followed .For standalone applications only these systems are mainly conceived. In this context, the work in [3] elucidates the implementation of an RTL Mixture-of-Gaussian background subtraction algorithm, mainly aimed at obtaining an embedded application for full-HD image resolution.

The Integration of general purpose processor system and specific hardware modules supported by an operating system combines the advantages provided by both approaches. In this sense, implementation of hardware software co-design accession includes a graphical operating system for execution of the processing application and to ease the connection of low cost cameras .however these proposals have draw backs in terms of frame rate, system integrity and efficiency based on features available in embedded platform.

The aim of this work is to present a cost efficient and versatile development platform for video processing algorithms. It eases the joint integration of software and hardware components in embedded systems application. Live video from a camera is the input to the platform and through interfaces connected to the system user inputs are given. Integration within the embedded system includes user handling capability.

Integration with in the embedded systems include user handling capability of a software program interface to select the type of processing to be done for the input video as well as real-time showing the processed results, providing the processing performance obtained in terms of frame rate per second for different set of image resolutions. In the embedded platform it makes possible for the development and debugging of software application. System can be connected via Internet application. System can be connected via Internet giving the possibility to interact as the network mode.

The structure of the paper is as follows section-II describes the base configuration of development platform by general design and implementation characteristics. Section III enumerates the procedure of enhancing the picture resolution by software application on the hardware platform. Section IV deals with the simulation results, Design summary like number of LUT's used etc., efficiency.

II. PLATFORM FOR VIDEO PROCESSING

A. Zynq Processing system

The data flow interconnection for the overall video processing system is shown in the following Fig.1.It is based on the Zed Board development board, equipped with the reconfigurable device from the Zynq-7000 family. Zynq system on chip (SoC) integrates an ARM Cortex-A9 dual core based processor system with a Xilinx 7-series FPGA fabric.

Hardware platform configuration for Zynq device can be described as the intercommunication between two different portions of electronic circuits between the two different portions of the electronic circuits. The upper basic portion, called the processing system (PS), is mainly formed by the ARM cores, I/O peripherals, clock system generators, memory interfaces and master/slave ports with AXI interface.

AXI is a standardized IP interface protocol based on the Advanced Micro-controller Bus Architecture (AMBA 4) specification. These interfaces provide a common IP interface protocol framework for building a system. Before any custom IP integrator, the IP must be packaged. To reduce the barrier of entry into the Vivado design tools chain, Vivado provides a simple way to package the IP. For custom AXI IP, Vivado can automatically infer the AXI interfaces when the IP port names as AXI4 specifications.

Zed Board consists of the Dual-core ARM Cortex-A9 Based Application Processor Unit (APU) which is having the capability 2.5DMIPS/MHz per CPU, up to 1GHz CPU frequency, coherent multiprocessor support, three watchdog timers, one global timer, and two triple-timer counters. A cache which has 32 KB level 1 4-way set-associative instruction and data caches, 512 KB 8-way set-associative level 2 cache, byte parity support. On Chip Memory consists of on-chip boot ROM, 256 KB 8-way set-associative level 2 cache, byte-parity support.

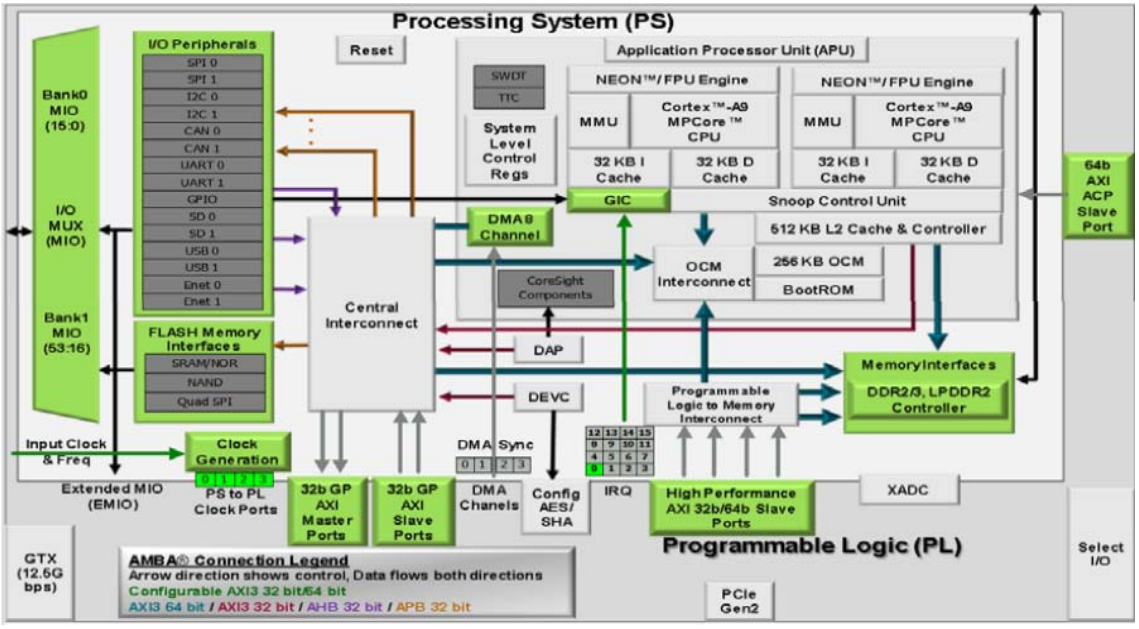

Fig. 1. Re-customize IP Dialog Box

External Memory Interfaces are multi protocol dynamic memory controller,16-bit or 32-bit interfaces to DDR3,DDR3L,DDR2,LPDDR2 memories, ECC support in 16-bit mode,1GB of address space using single rank of 8,16,32 bit wide memories.8-channel DMA controller has memory-to-memory, memory-to-peripheral, peripheral-to-memory and scatter-gather transaction support. I/O peripherals and Interfaces has Two 10/100/1000 tri-speed Ethernet MAC peripherals with IEEE std 802.3 and IEEE std 1588 ,scatter-gather DMA capability,

GMII,RGMII and SGMII interfaces, Two SD/SDIO 2.0/MMC3.31 complaint controllers. Interconnect has High band width connectivity within PS and between PS and PL ARM AMBA AXI based.

B. OV7670 Camera module

CMOS image sensor the OV7670 camera chip is a low voltage that provides the full functionality of a single chip image processor and VGA camera in a small footprint package. It provides full-frame, sub-sampled or windowed 8-bit images in a large range of formats, controlled through the serial camera control bus (SCCB) interface. Camera has an image capability up to 30 frames per second (fps) in VGA with user control over image quality, formatting and output data transfer.

All image processing functions, including exposure control, gamma, white balance, color saturation, hue control, and more, are also programmable through SCCB interface. In addition, they use proprietary sensor technology to improve image quality by reducing and eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, blooming, etc., to produce a fully stable, clean color image.

The features of this camera module is that for low-light operation it has High sensitivity, low operating voltage for embedded portable applications with I^2C standard SCCB interface compatible. It supports VGA, CIF and resolutions lower than CIF for RGB, YUV and YCbCr formats. For sampling it is using variopixel method, automatic image control functions Automatic Exposure Control, Automatic White Balance, Automatic Black-Level calibration, Automatic Band filter. Supports scaling, supports LED and flash strobe mode.

OV7670-VL2A is a color, lead-free 24 pin CSP2 package. The camera module consists of the Image sensor array, analog signal processor, A/D Converters, Test pattern Generator, Digital signal processor, Image Scaler, Timing Generator, Digital signal Video port, SCCB Interface, LED and Strobe flash control output.

The image array of the image sensor array has 656 x 488 pixels for a total of 320,128 pixels of which 640 x 480 pixels are active. Timing generator controls frame generation and array control, generation and distribution of timing signals internally, timing of frame rate, Automatic Exposure control (AEC).This camera chip progressively scans the array in which rows are sequentially read and transferred out to the analog processing block (APB). Frame rate timing can be adjusted by clock pre-scalar, Dummy Pixel Adjustment, Dummy row adjustment. Analog signal processor controls automatic gain control, Automatic white balance. An A/D converter has the functionality Digital Black-Level Calibration (BLC), Optional U/V channel delay Additional A/D range controls.

The features of the test pattern generator are the 8-bar color bar pattern, fade-to-gray color bar pattern, shift "1" in output pin. Digital signal processor controls interpolation from Raw data to RGB and some image quality control by Edge enhancement, color space converter, RGB matrix to eliminate color cross talk, hue and saturation control, White/black pixel correction, De-noise, Lens shading correction. Programmable gamma control, Transfer 10-bit data to 8-bit.Image scalar controls all output and data formatting required prior to sending the image out. This block scales YUV/RGB output from VGA to CIF and almost any size under CIF.LED and Strobe Flash Control Output has a strobe mode that allows it to work with an external flash and LED

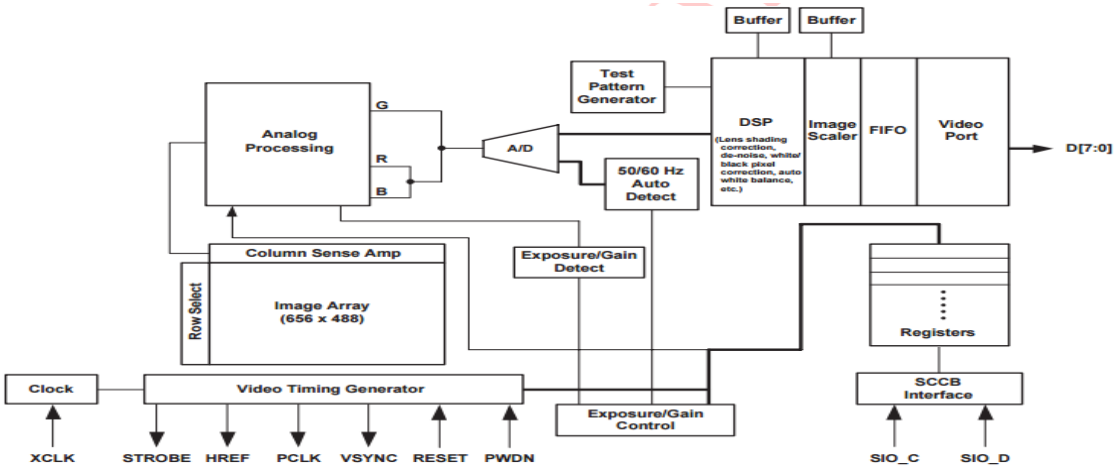

Fig. 2. Functional diagram of the OV7670 camera module

III. PROCEDURE TO GENERATE THE HARDWARE AND SOFTWARE PLATFORMS

Zed Board is particularly used for the applications where programmable logic as well as programmable software is needed to enhance the output. For the software running we need a hardware platform to run on top of it. Hardware platform is generated using the programmable logic. In Vivado we have to generate the VHDL code which consists of the interfacing between the zed Board and the OV7670 camera module. From this

programmable logic we will create the IP block and added to the IP catalog. Then the block diagram has to be created with programmable logic IP and the Zynq processing unit.

For interfacing we use the AXI interfacing is used so that the speed of data transfer is more compared to normal one. The wrapper bit file is generated using that block diagram .The output is observed using the Integrated Logic Analyzer (ILA).For the bit file generation the ILA should be removed. Then the hardware is launched to support the SDK. The camera module is having the different modules like VGA Generator, Capture logic, Frame buffer, controller clock. While interfacing we had used the core IP blocks like clock generator, BRAM controller.

There is a version problems occurred as the BRAM controller IP of older version is having less number of bit length to overcome this problem we had used the Xilinx VIVADO 2015.2.Otherwise the output will not produced properly due to the loss of the data. The BRAM controller bit capacity changes due to different types and version of the Xilinx tools like ISE, vivado different versions. In SDK the hardware platform is first selected with the board support package which supports the program dumping in to the board. Along with the C program coding the test peripherals, memory Tests, Zynq FSBL for boot loading functionality, and increasing capability of the number of peripherals interfaced without any errors.

The programming can be done via the LAN or the Ethernet connection .The IP address is same to the all Zed Boards. Via the SD card or temporary transfer of the file in to the card can be implemented. For the transfer of the file and execution of the file directly from the SD card the bin file should be created. Using the BOOTGEN we can create the boot.bin file which can be executed on the board directly by loading in to the SD card directly. Generally the program is executed in the SDK after the program is dumped in to the Zed Board then by using the minicom the output can be verified or checked. The C code is executed by running the program on the hardware platform.

By using the LAN connection the program can be executed by identifying the port to which it is connected. Then the SD card is mounted and the program is executed properly. Once it is completed to this the command from external camera is sent so that the live video output which can be modified in terms of the resolution, frames per second etc..,

IV. RESULTS

The real-Time video in RGB analog format has been captured from the OV7670 camera module. The captured video has been converted into frames and buffered using the C programming in the SDK .The stored frames have been converted into VGA resolution of 640X480 and displayed on the VGA monitor. The proposed embedded architecture for the video acquisition module is a predecessor to any image and video processing application which uses smart camera. In the design we stream the video frames on an individual basis, buffer the frames in the external memory SD card. By using the Zed Board the utilization percentage of the blocks is increased more and both the programmable logic and programmable software can be done.

The following are the Zed Board and OV7670 camera interfacing setup and the output observed before running C code and after running a C code.

Fig 3 displays the complete set up design how Zed Board is connected to the PC and the programming procedure. Fig 4 specifies the connection interface between the camera and the Zed Board using the pmod connectors, LAN connection, USB-UART connection to the PC etc., Fig 5 specifies the output after implementation of C program on the hardware platform in SDK for improvement of the resolution.

Fig. 3. Complete set up of the design

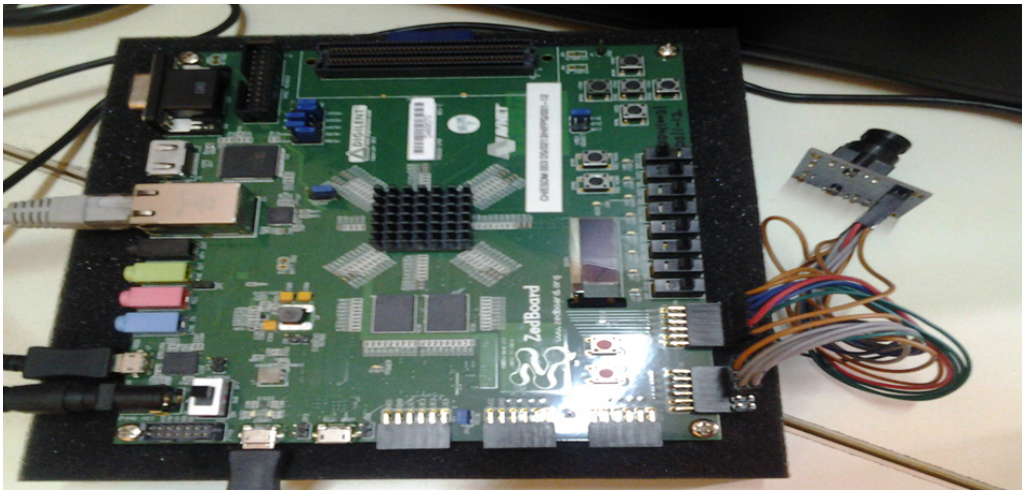

Fig. 4. Interfacing Zed Board with the OV7670 Camera module

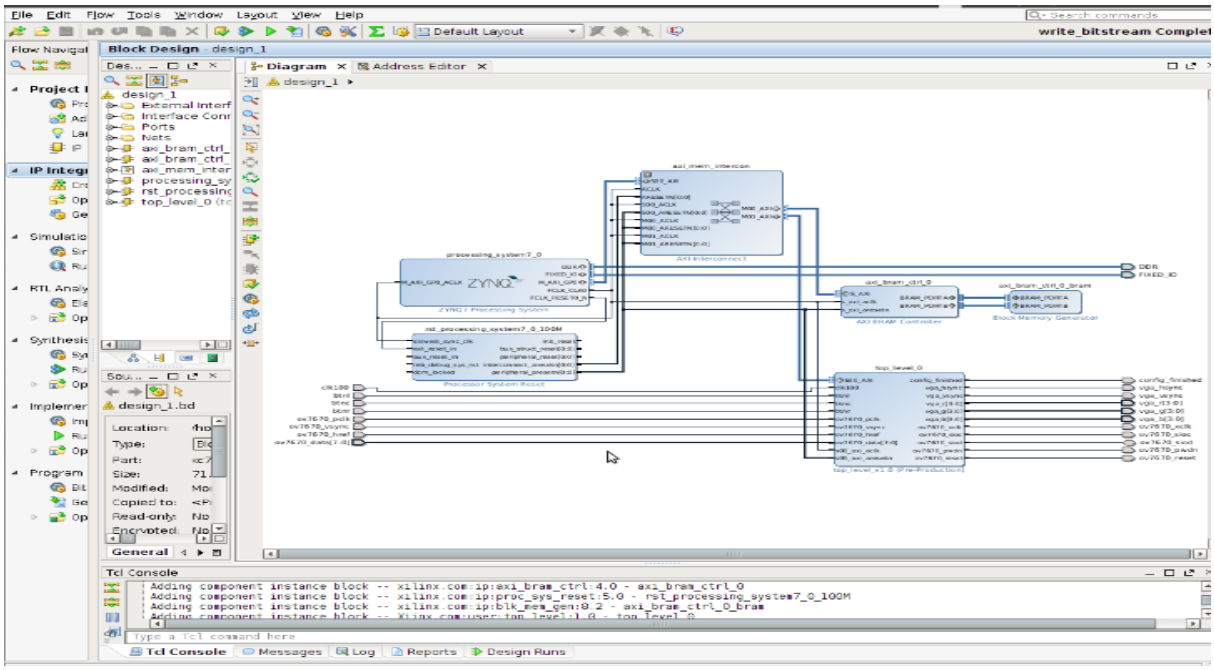

Fig. 5. Block Diagram generated to generate Hardware platform

Fig. 6. Output of the camera module

V. CONCLUSION

Interfacing Zed Board with the camera module OV7670 is done with the vivado for programmable logic and it is launched into SDK for the programmable software is run on top of that. The bin file is generated to run the program from the SD card directly via JTAG-USB connection or the Ethernet connection. The boot.bin file is created using the zynq FSBL so that the program can be runned at any time without the need of running from the SDK every time. This interfacing can be used as the CCTV footage. To this the external commands can be given by web camera interfacing and can be used for the applications human computer interfacing, eye detection, face detection through HCI.

ACKNOWLEDGMENT

This module is implemented as a part of project “Human computer interfacing, face and eye detection using the smart camera” in the organization. Signals can be sent from the camera to the CCTV camera so that the observation of the footage will be easier than the keyboard accessing for zoom in and zoom out .This project can be developed more using the OpenCV applications.

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