Design of Static Flip-Flops for Low-Power Digital Sequential Circuits

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Abstract— In this paper, we correlated various Master and slave flip-flops i.e., single edge triggered flip-flops. The low-power flip-flops have place utmost necessary elements all the range of the constructing static or successive circuits. We accomplish the comparison for their performance, Delay, Rise time, Fall Time and Power dissipation. Because Power confide in the number of transistors in the circuits, so we are comparing and calculating the number of transistors of the each flip-flops. Analysis of a static/sequential circuits is done by Linear Feed Back Shift Register (LFSR) using 45nm Technology with 5MHZ frequencies and their performance analysis.

Keywords— Flip-Flop, Edge Triggering, low power, Average power, Rise time, Fall Time and Frequency.

I. INTRODUCTION

Flip-flops and latches are affecting elemental repertory particle recycled largely in all different variety of digital circuits. The present technology digital designs utilize in-depth pipelining techniques also multiplied flip-flops easy modules like as shift register files. [1]. A large allocation regarding effective clock power have place recycled into pick up the particular successive elements. By reduction the clock power of latches and flip-flops, the entire chip power can be reduced. Flip-flops appears new different Structures, parallel as D- flip-flops, T-flip-flops and JK-flip-flops, of these D-Flip flop is the better standard one.

A regular Single Edge Triggered flip-flop data each of two powerful falling edge either powerful rising edge of the clock period. Powerful single edge triggered latches continue regularly configured as flip-flop outline, i.e., the sequential structures seeing two flip-flops in cascade [2].

II. PROPOSED DESIGNED STATIC FLIP-FLOPS.

A. CS^2 Flip-Flop

In luminous of this history, we here in propose a circuit shared static flip-flop (CS^2FF) is intensely low power digital circuits with the require number of transistors. Effective CS^2FF need only 24 transistors. This circuit consisting of only five NOR gates and two Inverters shown in Fig. [1]. These Inverters are used to generate the control signals of clock bar (CLKB) and first clock (CLK1) from quick clock of CLK. Here ‘NOR1’, ‘NOR2’ and ‘NOR3’ gates are master section flip-flop, while ‘NOR3’, ‘NOR4’ and ‘NOR5’ gates are slave section flip-flop. In this flip-flop design ‘NOR3’ is common of both master and slave flip-flops, along with it is used to access the data transferring master flip-flop to slave flip-flop. This circuit operation can be interpreted by testing the diagram as succeed. Historic master flip-flop operates using a positive first clock (CLK1) edge of the control signal. When the input data, first clock (CK1), and clock bar (CKB) are ‘D0’ is LOW and HIGH subsequently, ‘NOR1’ gate work as an Inverter and dramatic output of ‘NOR3’ is reset to logic ‘low’. Along these ‘NOR2’gate as well as works as an inverter and that affecting output of ‘NOR2’ data ‘QM’ transfers to ‘D0’. Again when the first clock (CK1) and clock bar (CKB) become logic levels high and low conditions resultantly, at the same time output of ‘NOR1’ remain reset to low logic level. Accordingly ‘NOR2’ and ‘NOR3’ are the master flip-flops and their data is held at ‘MFB’ in the process of ‘D0B’. Until historic slave flip-flop operates applying a negative edge of the clock signal. Meanwhile clock (CLK) and clock bar (CKB) are the logic levels high and low conditions resultantly. At a time output of ‘NOR4’ is clear to logic level low and ‘NOR5’ gate works in the act of an inverter. As a result of MFB data is transmitted to output of Q as ‘D0’.

Again at clock (CLK) and clock bar (CKB) become logic levels low and high consequently, effective output of ‘NOR3’ is clear to low logic level. Since ‘NOR4’ and ‘NOR5’ take away the slave flip-flop, including the data is controlled by Q in the process of ‘D0’. The present custom designing of CS^2FF determine in the process of a master and slave flip-flop among a small number of transistors [3].

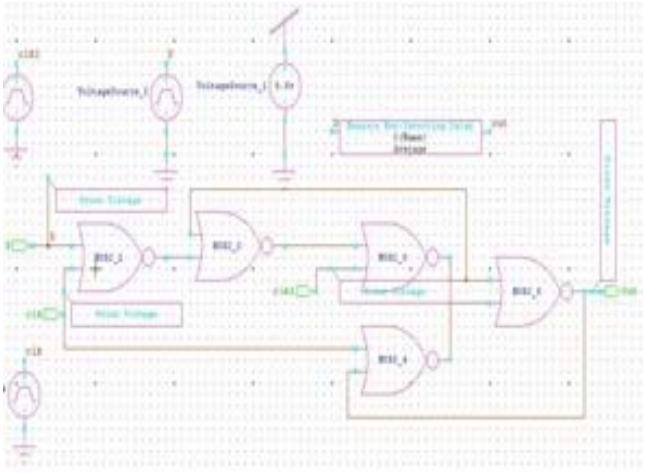

Fig. 1. Schematic of CS^2 Flip-Flop.

B. C^2MOS Flip-Flop

C^2MOS flip-flop proposed by that consists of an unsteady C^2MOS feedback of the flip-flop at the outputs. The clocked inverter D input Clk1 to node N, when the clock is HIGH logic. The feedback path consists of second clocked inverter and first clocked inverter continues the same logic level near to N at the same time clock is LOW logic level. Hence slave flip-flop receives functional logic level and third clocked inverter logic level transfers against to node N to Q output node. When impressive clock is grounded, at that time feedback require fourth clocked inverter and second inverter protects the output Q at logic level.

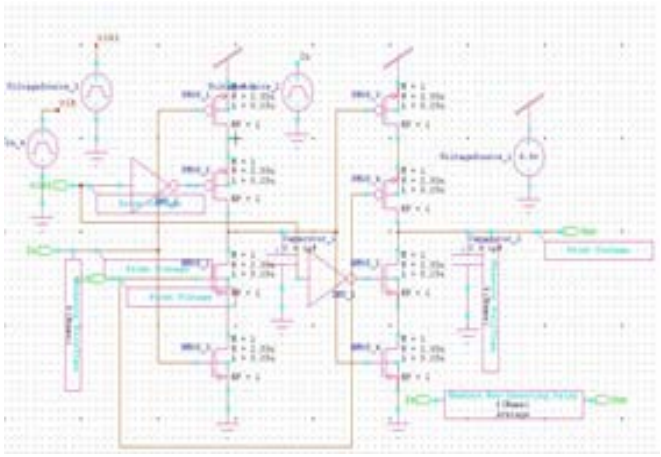

Fig. 2. Schematic of C^2 MOS Flip-Flop.

There is no drop at intermediate circuit nodes. So the circuits is extra fit through noise along high noise confine new ratio into another circuit [2]-[4].

C. Pass Transistor Flip- Flop

Effective pass transistor flip-flop design has shown below fig. [3], the master category of the flip-flop is positive level triggered D flip-flop that shifts input logic level D to N. At the same time clock drives only LOW logic level, the feedback path consisting of PMOS transistor controls more effective logic levels at node N. The slave flip-flop section consisting negative level triggered D flip-Flop that transfers the logic HIGH the feedback path containing of PMOS transistor maintains the Q output logic level, PMOS transistor is recycled in the feedback pass as it advantages to other compact layout than accepting a NMOS transistor.

But due to this output Q logic level is reality continued at the clock is logic HIGH and the clock logic is LOW. At the same time when clock is interrupted, this circuit does not show the static behaviour. By testing of NMOS transistor in that feedback path alternative of PMOS transistor, this limitation can be overcome. Then the circuit will becomes static without increasing the number of transistor. This flip-Flop consist 12 transistors. In histrionic 12 transistor, 4 transistors are effective clocked transistors.

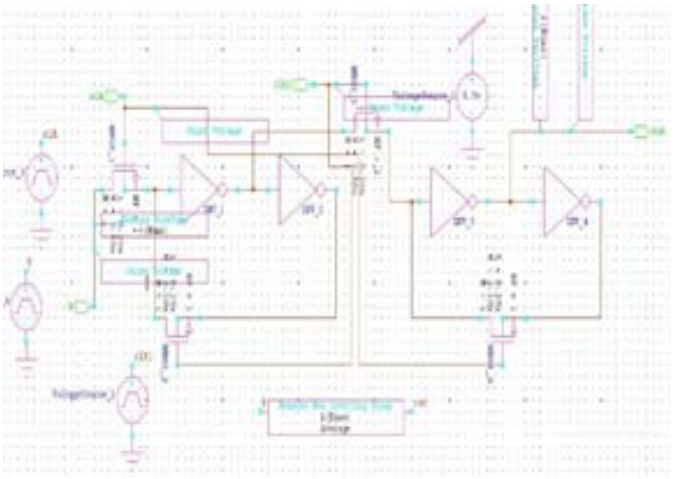

Fig. 3. Schematic of Pass Transistor Flip-Flop.

D. Transmission Gate Flip-Flop

The conventional negative edge triggered Transmission Gate (TG) based flip-flop required two level sensitive latches with 16 MOSFETs that as shown below Fig. [4]. The Master flip-flop is operative supported the positive level from the each clock signal [5]. Effective input D is transferring in to the node N. In case feedback signal control the logic level at the node N at a same time clock activate to the LOW logic level. In addition to impressive slave flip-flop is passes the logic level at node N and negative level clock to output node Q. One more time, the clock logic level is HIGH at that time feedback loop contains the logic level Node Q.

Affecting transmission gate flip-flop speed limit is only two gate delays. The main advantage of the flip-flop is that affect smallest design undertaking. Previously is extensively recycled expected to very less area along with less power consumption. In the low power application speed is not peak transaction used in the Transmission.

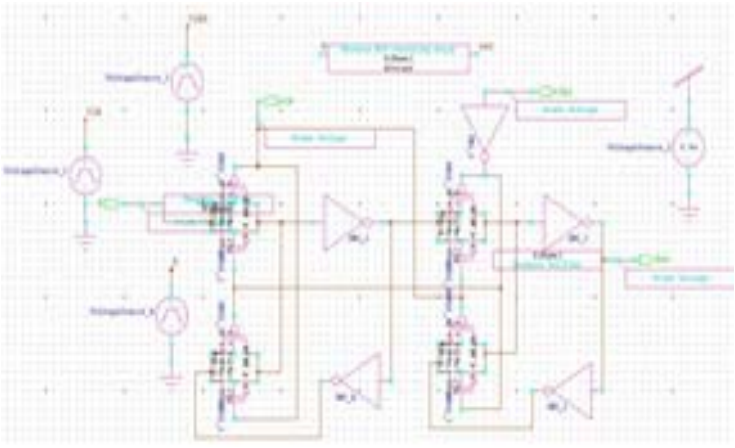

Fig. 4. Schematic of Transmission Gate Flip-Flop.

E. Low area Flip-Flop

The general Transmission gate flip-flop desire approximately huge number of clocked transistor. To decrease affecting clock load of the flip-flop the divide Transmission gate in the comeback loop of both latches can be removed. This low area D flip-flop require the limited quantity of clocked transistors along with transistors as equal to TGFF, even then it require more power as well as delay related to the conventional TGFF. The Basic Circuit of Low-area as show fig [5].

A common access for reduction of occupied place atop of effective traditional D flip-flop survive to eliminate the two comeback transmission gates. Hence the stability of the comeback inverters include to be minimized into weak short-circuit power dissipation overdue to voltage difference [7].

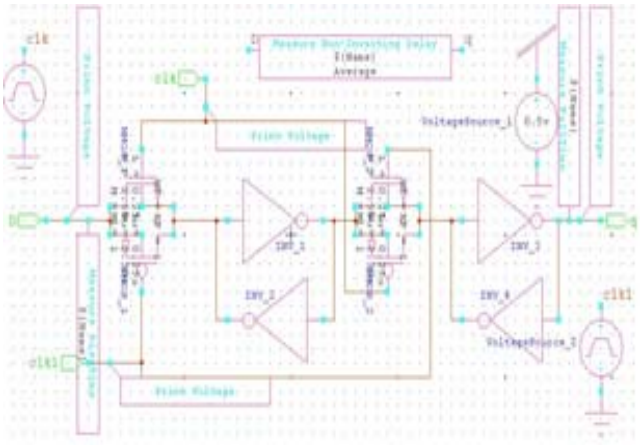

Fig. 5. Schematic of Low area Flip-Flop.

III. LINEAR FEED BACK SHIFT REGISTERS

A. LFSR using Dynamic logic D Flip-Flop

The compact designing of CMOS LFSR dynamic logic consist of D flip-flop. In this system existing the number of active devices can be reduced. In the existing system include the preferable drawback is approach the variation of the voltage between LOW logic level and HIGH logic level at every phase, so in this series every transistor is saturated output at its input, so various appliances are add series in a sense/sanity pathway, a commonly designed gate can be needed to reset the characteristics voltage to the full value. This façade to use drawback of dynamic logic, whichever the frequently used in the process of comparing to the clocked logic. During the time makes fair the separation between these type of constructed and static logic. Normally dynamic logic depends upon the minimum clock rate and speed adequate the output state about every dynamic logic, here gate have being recycled previously it drop output of the capacitance property so main case, the output is no more being strongly induced when during the part of the clock cycle. Dynamic logic is perfectly designed, as shown below fig. [6], at that time dynamic logic might be over double in the process of fast static logic. It handling apart the rapid N-type transistors only, this can be improved transistor development passive or static logic is every slow due to double of power higher thresholds.

Dynamic logic package be strong to with effort, however it can be affecting only one prime when expanded processing speed is needed, even if any manufacturers parallel as Intel include completely static logic to save into power. In a normal dynamic logic gently increases effective number of transistors. So that are shifted on a little bit of given time, whichever increases power consumption by all static CMOS. Here dynamic logic based system as effective power saving techniques that can be designed. In extension, every complain can transmit an arbitrary number of bits and no power consume glitches. Power saved clock gating along with non-parallel techniques are countless more reasonable in dynamic logic. The large scale components regarding dynamic power distraction emerges taken away transient shifting behavior of the each node.

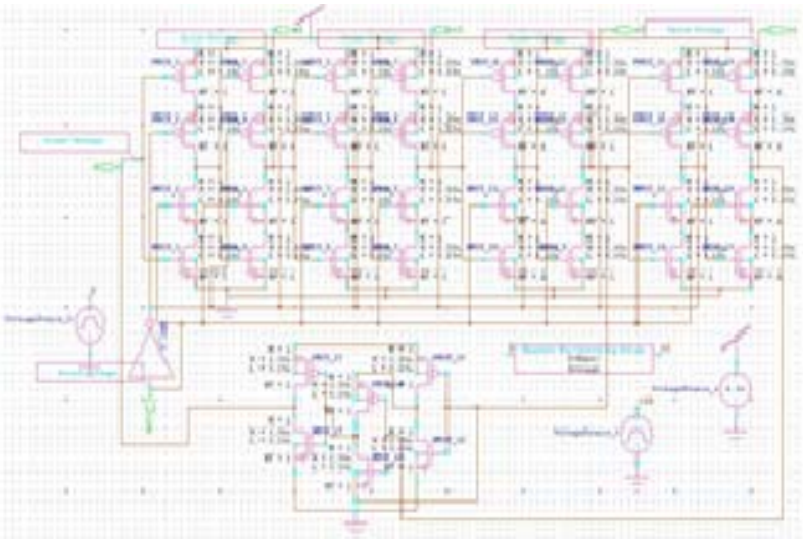

Fig. 6. Schematic of Dynamic logic Flip-Flop

CMOS devices Signal transitions alternating away from the two different logic levels, appearing in sudden charging and discharging of parasitic capacitances up to the minute of the each circuit. Dynamic power dissipation placed reciprocal into the square of effective supply voltage.

B. D Flip-Flop Design using Pass Transistor

Effective ultimate solid designing of single edge trigger flip-flop is placed on pass transistors and inverters as shown in Fig [7], [9]. The two tie-up inverters are in the memory state at clock is =0, at the same time PMOS transistor is on. Here alternative two tie-up inverters are right grip action in different way, and the clear function is secure by directly connecting to the ground of the master flip-flop and slave flip-flops through NMOS devices.

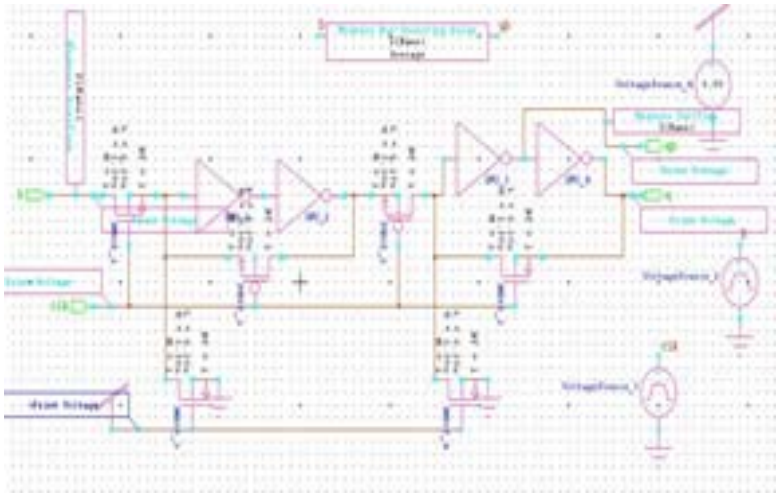

Fig: 7. Schematic of D-Flip-Flop using Pass Transistor.

C. D Flip-Flop Design using Transmission Gate

Emotional designing of single edge trigger flip-flop is placed on TG (Transmission Gate) and inverters, as shown fig. [8], [9]. At that time negative edge input of the clock, T2 transistor and T3 transistor are OFF and T1 transistor and T4 transistor are ON. Throughout that time the slave flip-flop maintained the tie-up through the transistor T4 and two inverters I3 and I4. Hence the earlier triggered value from input to D is received in slave Flip Flop. At the same time T3 is off and master flip-flop next state but slave flip-flop is not passed. Towards that positive clock edge T2 transistor and T3 transistor are swing ON and new flip-flop value passes to slave flip-flop complete the tie-up of T2 transistor and I1 and I2 inverters. Although we reset the circuit at that time master flip-flop and slave flip-flop chains are picked down to ground.

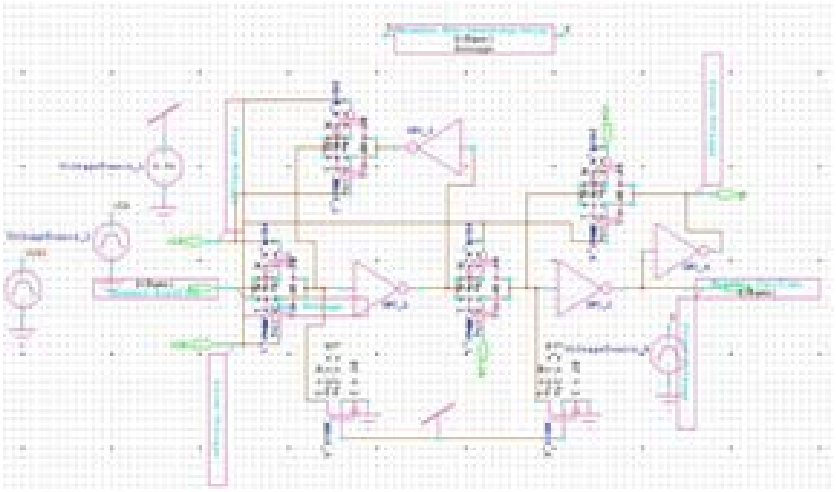

Fig. 8. Schematic of D-Flip-Flop using Transmission Gate.

IV. SIMULAION RESULTS

In this section, the achievement of expected CS^2FF was designed by using Tanner EDA with a set of 0.45-µm CMOS Technology along a Supply voltage 0.5v. For comparison, we also evaluated C^2MOS- FF, PTFF, and TGFF. Again we doing comparison of Low area FF, LFSR-DL FF, LFSR-PT FF and LFSR-TG FF. The time average power dissipation was characterized held down the status of 5-MHZ Clock frequency and 25°C temperature. Because power calculate on the number of transistors in the circuits, so we related the transistor result of separate flip-flops. Table I and II display the transistors calculation of all discussed Flip-Flops. Comparing and Plotting graphs between the Power Vs VDD Fig. [9], Delay Vs Frequency Fig. [10] and Power Vs Frequency Fig. [11], the low area DFF dissipate 20% extra total and 27% slower correlated to the TGFF.

TABLE I. COMPARISON OF DIFFERENT FLIP-FLOP DESIGNS

Flip-Flop Design	CS^2 Flip-Flop	C^2MOS	Transmission gate Flip-Flop	Pass Transistor Flip-Flop	Low Power area Flip-Flop
No. of Transistors (ns)	24	08	16	12	12
Rise Time (ns)	4.0000e-010	4.0000e-010	4.0000e-010	4.0000e-010	-2.0063e-007
Fall Time (ns)	6.2167e-010	2.0156e-007	3.6053e-010	7.8960e-010	3.5341e-010
D to Q delay (ns)	1.4659e-009	4.9360e-008	-5.0245e-008	-4.9525e-008	-1.4935e-007
Average Power (Watts)	4.296889e-002	2.072542e-001	1.075466e-001	5.618604e-002	3.557484e-002

TABLE II. COMPARISON OF DIFFERENT LFSR FLIP-FLOP DESIGNS

Flip-Flop Design	LFSR-Dynamic Logic Gate	LFSR-Pass-transistor Gate	LFSR- Transmission Gate
No. of Transistors	40	14	18
Raise Time (ns)	4.0000e-010	4.0000e-010	4.0000e-010
Fall Time (ns)	4.8938e-010	-1.0077e-007	1.0013e-009
D to Q delay (ns)	4.9270e-008	-5.0218e-008	-5.0447e-008
Average Power (Watts)	1.545689e-001	4.293220e-002	6.994824e-002

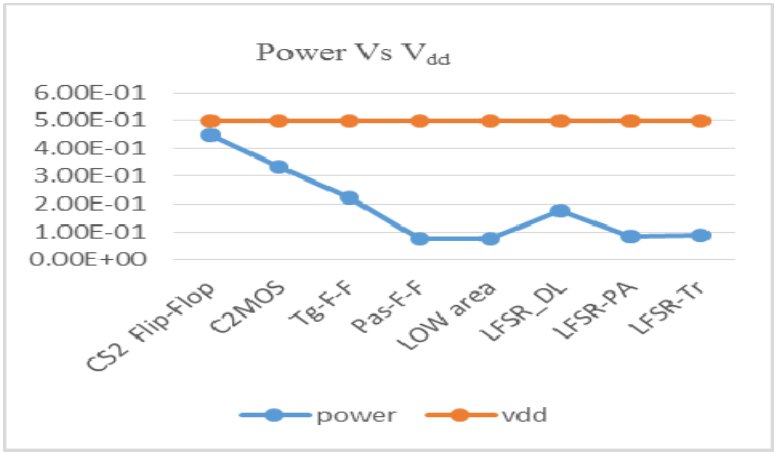

Fig: 9. Performance of Power dissipation V_{DD}.

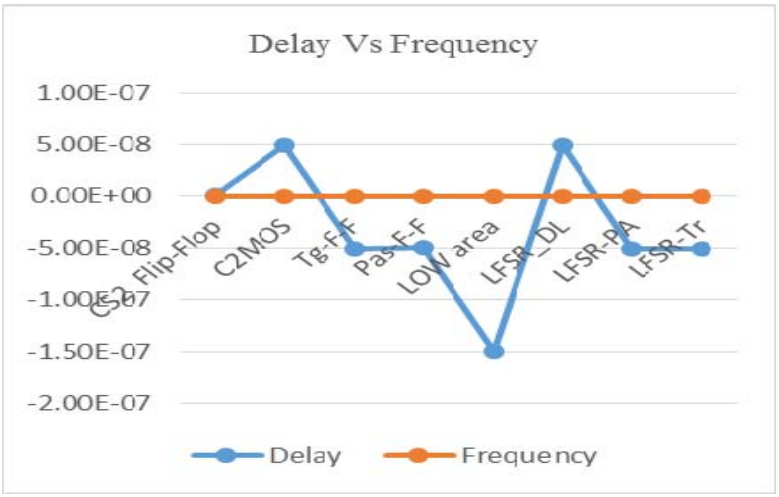

Fig: 10. Performance of Delay versus frequency.

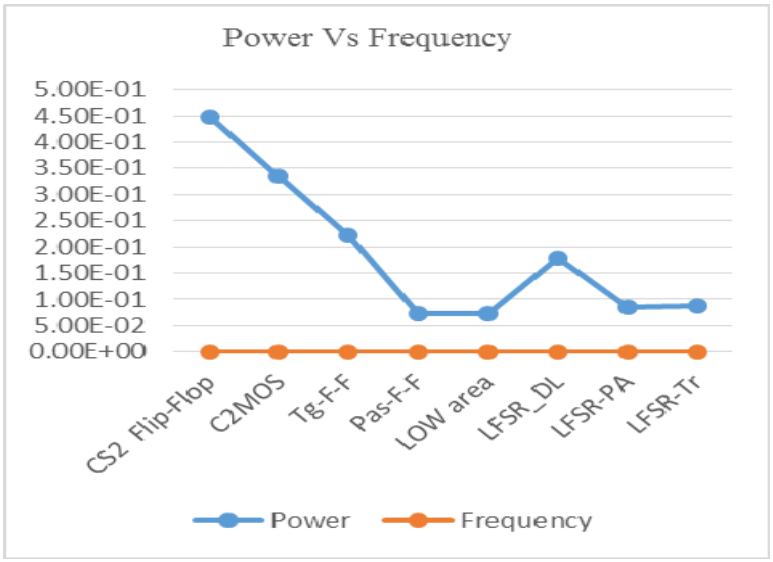

Fig: 10. Performance of Power dissipation versus frequency.

V. CONCLUSION

In this paper, we did a parallel analysis of different Master slave flip-flips as long as intensely low-power VLSI digital circuits. Here we include expressive LFSR Flip-Flop designed with less number of transistors having very fewer power consumption. These effective Flip-Flops are simulated as 45nm technology adopting Tanner EDA Tool. Sensational estimation of three shift registers are shown in Table II. With all these results LFSR-PT speed performance, power and delay are better than LFSR-DL and LFSR-TG.

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