Dual mode logic buffers for VLSI interconnects

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Abstract—Buffer insertion is a mechanism widely used to increase the performance of VLSI digital circuits. Buffer insertion has a strong impact on reliability in terms of delay and power dissipation of synchronous systems, since the clock distribution system requires reduced or controlled clock skew, being the buffer insertion and buffer sizing becomes an important aspect. Buffer insertion has also been used to reduce the noise generation, especially in heavy loaded nets, since the inclusion of buffer helps to desynchronize signal transitions.

Keyword-Buffer insertion, CMOS inverter, Dual mode logic

I. INTRODUCTION

Due to advancement of technology power consumption and delay are the major attentions in designing VLSI circuits. Scaling the devices leads to more power dissipation, operating the devices below the threshold also leads to further increase in power dissipation. Designing a circuit to operate at low power has been a major challenge in ICs. Since the device consumes some delay and power dissipation in processing a signal, the wire too consumes power dissipation. So, our main aim is to reduce the power dissipation and delay due to the wires. Since the lengthy wire consumes more delay due to high resistance which varies linearly to the length, here the wires are divided into many segments by inserting the buffers. The buffers can divide the long wires into smaller section so that the signal can be processed quickly.

CMOS inverter is the series combination of nmos and pmos acts as a most efficient device which can be used to pass the signal between the source and driver. A new method has been proposed to reduce the expected delay and end delay by using buffer inserting techniques and choosing the best size and place to insert the buffer [2]

A new algorithm has been found for the optimal noise avoidance and for simultaneous delay and noise optimization [4]. Low voltage dual mode logic family allows the designer [1] to switch between static and dynamic modes of operation and achieve higher performance in terms of power. An optimized CNTFET driver has been proposed by [6] which can effectively drive the CNT interconnects compared to the normal CMOS drivers. So in all the works done here shows to improve the delay and power dissipation by means of a new algorithm, by CMOS driver utilization and dual mode logic has been excellent in terms of performance for sub threshold circuits.

In this paper we have analyzed the performance of RLC interconnects at Local, intermediate and global level as discussed earlier [10] .For the first time we have used the dual mode logic as drivers and buffers in VLSI interconnects and made a comparison with CMOS drivers as buffers and drivers. We found that Dual mode logic can perform better than normal CMOS devices, as drivers or buffers especially at sub threshold conditions.

II. DUAL MODE LOGIC

A. Dual mode logic operation and structure

Dual mode logic gate [1] consists of a static CMOS gate and an additional transistor whose gate is connected to the clock signal and its output is connected to the output of the static CMOS transistor

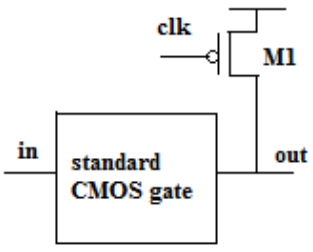

Fig.1 DML gate [1]

Here a PMOS transistor is connected to the output of static CMOS. The output obtained is an inverter in which the PMOS acts as an additional precharge transistor to boost the signal so that delay and power dissipation may get reduced. Apart for normal CMOS inverter the power dissipation in this case might be lesser.

III. COMPARISON OF DUAL MODE LOGIC AND CMOS INVERTER AS DRIVERS

A. Super threshold region

The performance of drivers at super threshold, moderate sub threshold and deep sub threshold has been analysed. Here the table.1 shows the performance of CMOS inverter and dual mode logic as drivers in super threshold region i.e Vdd=1V [9] to pass the signal from driver to load, when the length of the interconnect increases, the delay increases for both the cases, but the power dissipation is less for Dual mode logic based driver at global interconnects level.

Table.1 Delay and power dissipation at super threshold region

Length (um)	**CMOS inverter**		**Dual mode logic**	
	Delay (ns)	**Power dissipation (nw)**	**Delay (ns)**	**Power dissipation (nw)**
400	1	158.8	1.2	200
800	1.2	109.71	1.2	117.43
1200	1.4	83.8	1.4	16.47

At the local and intermediate interconnect level the performance of CMOS inverter is better compared to dual mode logic

B. Moderate sub threshold region

The performance of drivers at moderate sub threshold region i.e Vdd=0.5V [9] from Table.2 shows that when the length of the interconnect increases in dual mode logic, but the power dissipation almost remains same for both cases.

Table.2 Delay and power dissipation at moderate sub threshold region

Length(um)	**CMOS inverter**		**Dual mode logic**	
	Delay	**Power dissipation (nw)**	**Delay**	**Power dissipation (nw)**
400	1.2ns	26.09	1.2ns	30.41
800	0.01us	16.95	1.2ns	17.43
1200	0.02us	11.63	0.05us	11.24

The performance of CMOS inverter is better in terms of delay at moderate sub threshold region for intermediate and global interconnects.

C. Deep sub threshold region

The performance of drivers in deep sub threshold region at Vdd=0.1V [9] from Table.3 shows that there is reduction in delay at global interconnect level for dual mode logic and there is a slight increase of power dissipation at global level

Table.3 delay and power dissipation in Deep sub threshold region

Length(um)	**CMOS inverter**		**Dual mode logic**	
	Delay (us)	**Power dissipation (pw)**	**Delay (us)**	**Power dissipation (pw)**
400	0.03	211.13	0.04	237.76
800	0.05	162.94	0.05	162.9
1200	0.2	110.63	0.1	113.51

The performance of all these shows that delay is slightly lesser for dual mode logic compared to CMOS inverter in all the case and the power dissipation is lesser in case of super threshold and moderate sub threshold and slightly higher in deep sub threshold. This shows that the performance of dual logic is better compared to CMOS inverter.

IV. COMPARISON OF DUAL MODE LOGIC AND CMOS INVERTER AS BUFFERS

The performances of CMOS inverters and Dual mode logic as buffers has been analyzed here

Table.4 delay and power dissipation of buffers in Super threshold region

Length(um)	CMOS inverter		Dual mode logic	
	Delay (ns)	Power dissipation (nw)	Delay (ns)	Power dissipation (nw)
400	1.1	288.772	1	254.59
800	1.2	172.247	1.2	190.52
1200	0.05us	141.609	0.05us	138.22

Table.5 delay and power dissipation of buffers in moderate Sub threshold region

Length(um)	CMOS inverter		Dual mode logic	
	Delay	Power dissipation (nw)	Delay	Power dissipation (nw)
400	1.2ns	38.676	1.3ns	46.16
800	0.01us	26.158	0.01us	24.77
1200	0.01us	20.49	0.01us	19.61

Table.6 delay and power dissipation of buffers in Deep Sub threshold region

Length(um)	CMOS inverter		Dual mode logic	
	Delay (us)	Power dissipation (pw)	Delay (us)	Power dissipation (pw)
400	0.01	404.99	0.02	402.5
800	0.06	232.722	0.02	213.87
1200	0.04	181.91	0.05	174.82

Table.4 shows the performances at super threshold region (Vdd=1V), here the delay of both the devices remains the same and has a reduced power dissipation for any lengths in case of dual mode logic.

Table.5 shows the performance at moderate sub threshold region (Vdd=0.5V), here the delay remains the same for both cases and there is an improvement in reduction of power dissipation, when the length of the interconnect increases for both cases.

Table.6 shows the performance at deep subthershold region (Vdd=0.1V), here the delay remains the same and the power dissipation getting reduced for all the length of the interconnects. In all the cases same number of buffers has been used for both the logics.

V CONCLUSION

The performance of Dual mode logic devices shows that when they are used as drivers their performance in terms of power dissipation is slightly lesser with the same delay compared to CMOS inverters as drivers, when Dual mode logic is used as buffers in almost all the three threshold regions the performance of Dual mode logic is better than CMOS inverters, so, Dual mode logic can be used as buffers in VLSI circuits in all the operating conditions of the interconnect. .

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