

# DESIGN AND ANALYSIS OF ADDER CIRCUITS USING LEAR SLEEP TECHNIQUE IN CMOS TECHNOLOGIES

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**Abstract**— Due to millions of integration of components and shrinking process technology, nowadays leakage power tends to play a major role in total power consumption. In this paper various existing leakage power reduction techniques such as full sleep, sleepy stack, dual sleep, sleepy keeper and dual stack are analysed and two new techniques are proposed to reduce the leakage power in digital circuits by generating transistor grating technology. The digital circuits such as half adder and Full adder are designed using the proposed techniques in 32nm, 22nm and 16nm CMOS technologies and their performances are analysed.

**Keywords**— Power dissipation, leakage power reduction techniques, LEAR Sleep techniques, CMOS design.

## I. INTRODUCTION

Increase in the number of transistors speed results in high performance in the current generation processors. The performance improvements have been supplements by an increase in the power dissipation. A high power dissipation system increases the cost of cooling and reduces the system reliability. The advantages of using the combination of low-power components in conjunction with low-power design techniques are more valuable now than ever before. Power consumption due to the leakage has joined the switching activity as a primary power management concern. There are many techniques that have been developed in the past decade to address the continuous power reduction requirements of most of the high performance. With downward scaling of technology, the static power consumption is becoming more dominant. The power reduction must be achieved without trading-off the performance which makes it harder to reduce leakage during normal operation [10]. There are several techniques for reducing the leakage power in *sleep* or *standby* mode. There are several VLSI techniques to reduce the leakage power [1]. Each technique provides an efficient way to reduce the leakage power, but disadvantages of each technique overcomes the application of each technique [8,12]. This paper mainly emphasized on reducing the count of transistors using different low power techniques, which ultimately reduces the power dissipation.

## II. EXISTING METHODOLOGY

Leakage power of CMOS transistors depends on the gate length and oxide thickness [4]. The supply voltage is decreased which leads to the performance degradation, to decrease the dynamic power. Various leakage power reduction techniques have been developed to reduce both dynamic and leakage power. Each technique provides an efficient way to reduce the leakage power, but disadvantages of each technique overcomes the application of each technique. The various leakage power reduction techniques are, full sleep, sleepy stack, sleepy keeper Dual sleep and Dual stack.

### 1. LIMITATIONS OVER THE EXISTING METHODOLOGY

#### A. FULL SLEEP Technique

Full sleep Technique is a self State-destructive technique which cuts off either pull-up or pull-down or both the networks from the supply voltage or ground by using the sleep transistors. Isolating the logic networks, this technique dramatically reduces the leakage power during sleep mode. However, the area and delay of the circuit are increased due to additional sleep transistors. During the sleep mode, due to the floating values in the pull-up and pull-down networks state will be lost. These state values impact the wakeup time and energy significantly due to the requirement to recharge the transistors which lost their state during sleep mode.

### B. SLEEPY STACK technique

In this technique, every transistors in the network are duplicated with both the transistors which the bears half of the original transistor width [4,6]. When both transistors are turned off duplicated transistors causes a slight reverse bias voltage between the gate and source. Because of the sub-threshold current the transistor is exponentially depends on its gate bias and it obtains substantial current reduction. It overcomes the limitation with the sleep technique by retaining its original state but it takes more wakeup time.

### C. SLEEPY KEEPER Technique

This technique consists of the sleep transistors where is NMOS connected to Vdd and PMOS to the Gnd. This creates the virtual power and ground rails in the digital circuit, which affects the switching speed when the circuit is in active mode [9]. The identification of the idle regions of the circuit the sleep signal needs an additional hardware which are capable of predicting the circuit states accurately, increasing the area requirement of the circuit. This additional circuit consumes more power throughout the circuit operation continuously.

## III. PROPOSED METHODOLOGY

By analysing the performance of the existing system, three new leakage power reduction techniques are proposed to reduce the leakage power better than the existing techniques. In the proposed technique the concept of the LECTOR technique and the sleep transistor techniques are used. Though these two new techniques are used to reduce leakage power in both active and sleep modes. The proposed techniques are,

- LEAR Sleepy Technique,
- LEAR Sleeper Technique.

### A. LEAR SLEEPY TECHNIQUE:

In the proposed lear sleepy technique two self-controlled transistors are designed in between the pull up and pull down network. In this where the sleep transistor S connected to the VDD and sleep bar s' is connected to the ground as shown in Fig1. During the standby mode the sleep transistors are turned off and introduce a large resistance in the conduction path. Hence, the leakage power is reduced in the circuit. By cutting off the power source, technique can be used to reduce the leakage power effectively in both sleep and active mode.

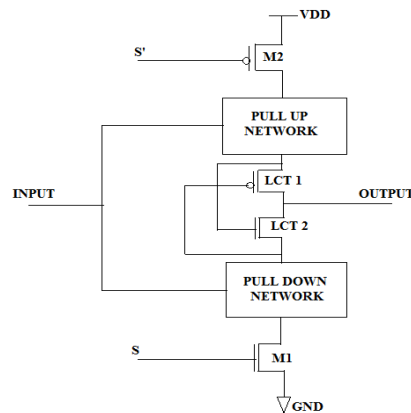


Fig 1 LEAR SLEEPY TECHNIQUE

### B. LEAR SLEEPER TECHNIQUE

An additional pMOS transistor is placed in parallel to the pull-down sleep transistor as the only source of GND to the pull-down network and an additional nMOS transistor is placed in parallel to the pull-up network connects the VDD. Then the two self-controlled transistor called the lector transistors are connected in between the pull up and pull down network as shown in Fig 2. This arrangement of transistor ensures that one of the LCTs always operates in its near cut-off region. By combining the transistors the leakage power will be reduced in both the sleep and active mode.

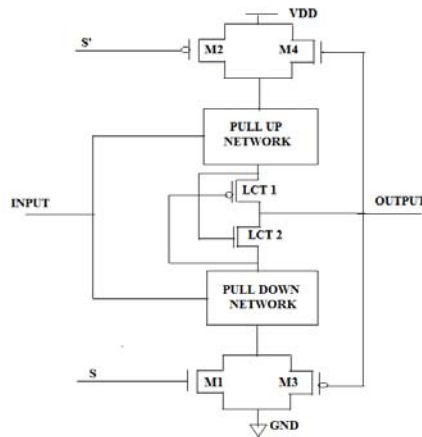


Fig 2 Lear sleeper technique

#### IV. SIMULATION RESULTS

To evaluate the performance of the digital circuits such as half adder and full adder which are designed in this paper using 32nm CMOS technology. All simulations are carried out using HSPICE simulation tool. The simulated waveform of half adder, full adder and multiplexer circuits using proposed techniques are shown from Fig 3 to Fig 6.

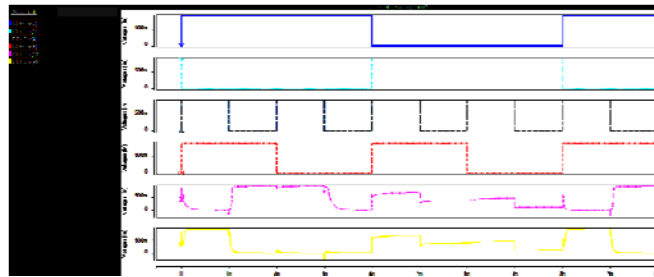


Fig 3 Transient analysis of half adder using proposed learsleepy technique

Fig 3 describes the transient analysis of half adder. In this analysis v(2), v(3) represents the sleep signals, v(4), v(5) represents the input signals and v(16), v(19) represents the output signals.

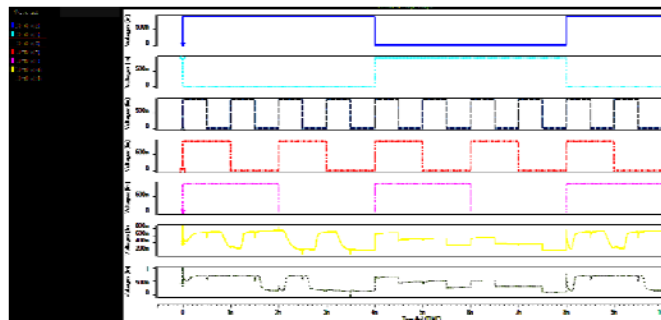


Fig 4 Transient analysis of full adder using proposed learsleepy technique

Fig 4 describes the transient analysis of full adder. In this analysis v(42), v(40) represents the sleep signals, v(2), v(3), v(6) represents the input signals and v(31), v(39) represents the output signals.

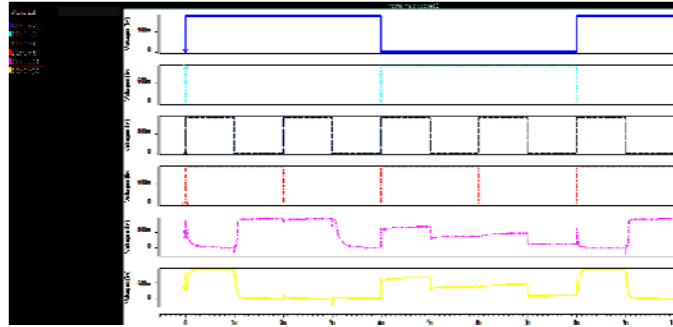


Fig 5 Transient analysis of half adder using proposed learner technique

Fig 5 describes the transient analysis of half adder. In this analysis v(2), v(3) represents the sleep signals, v(4), v(5) represents the input signals and v(16), v(19) represents the output signals.

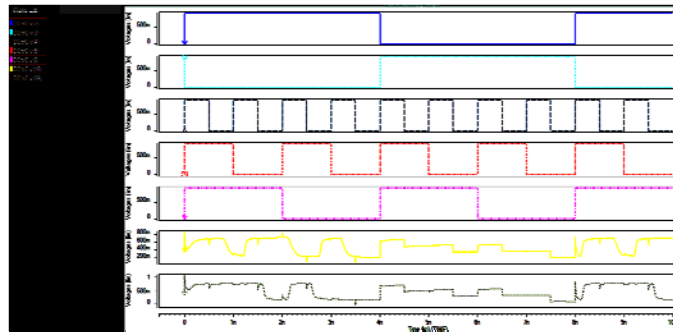


Fig 6 Transient analysis of full adder using proposed learner technique

Fig 6 describes the transient analysis of full adder. In this analysis v(42), v(40) represents the sleep signals, v(2), v(3), v(6) represents the input signals and v(31), v(39) represents the output signals.

**V. PERFORMANCE ANALYSIS**

The average power and leakage power of half adder and full adder circuits using proposed techniques are obtained and analysed.

Table 1 POWER ANALYSIS OF HALF ADDER USING 32nm CMOS TECHNOLOGY

DESIGN	Average power (W)	leakage power (W)
CONVENTIONAL DESIGN	$9.53 \times 10^{-06}$	$1.63 \times 10^{-06}$
LEAR SLEEPY	$1.40 \times 10^{-07}$	$333.78 \times 10^{-12}$
LEAR SLEEPER	$3.59 \times 10^{-07}$	$433.79 \times 10^{-12}$

Table 1 describes the power analysis of half adder circuit for conventional and proposed techniques using 32nm CMOS technology.

Table 2 POWER ANALYSIS OF FULL ADDER USING 32nm CMOS TECHNOLOGY

DESIGN	Average power (W)	leakage power (W)
CONVENTIONAL DESIGN	$8.49 \times 10^{-07}$	$23.419 \times 10^{-09}$
LEAR SLEEPY	$1.233 \times 10^{-07}$	$333.35 \times 10^{-12}$

Table 2 describes the power analysis of Full adder circuit for conventional and proposed techniques using 32nm CMOS technology.

Table 3 POWER ANALYSIS OF HALF ADDER USING 22nm CMOS TECHNOLOGY

DESIGN	Average power (W)	leakage power (W)
CONV DESIGN	$6.404 \times 10^{-06}$	$1.636 \times 10^{-06}$
LEAR SLEEPY	$1.544 \times 10^{-06}$	$144.29 \times 10^{-09}$
LEAR SLEEPER	$1.101 \times 10^{-06}$	$1.001 \times 10^{-09}$

Table 3 describes the power analysis of half adder circuit for conventional and proposed techniques using 22nm CMOS technology.

Table 4 POWER ANALYSIS OF FULL ADDER USING 22nm CMOS TECHNOLOGY

DESIGN	Average power (W)	leakage power (W)
CONV DESIGN	$6.632 \times 10^{-07}$	$101.95 \times 10^{-09}$
LEAR SLEEPY	$6.633 \times 10^{-07}$	$750.2 \times 10^{-12}$

Table 4 describes the power analysis of Full adder circuit for conventional and proposed techniques using 22nm CMOS technology.

Table 5 POWER ANALYSIS OF HALF ADDER USING 16nm CMOS TECHNOLOGY

DESIGN	Average power (W)	leakage power (W)
CONV DESIGN	$4.092 \times 10^{-06}$	$135.17 \times 10^{-09}$
LEAR SLEEPY	$3.334 \times 10^{-07}$	$1.474 \times 10^{-09}$
LEAR SLEEPER	$1.215 \times 10^{-07}$	$2.139 \times 10^{-09}$

Table 5 describes the power analysis of half adder circuit for conventional and proposed techniques using 16nm CMOS technology.

Table 6 POWER ANALYSIS OF FULL ADDER USING 16nm CMOS TECHNOLOGY

DESIGN	Average power (W)	leakage power (W)
CONV DESIGN	$5.442 \times 10^{-07}$	$295.75 \times 10^{-09}$
LEAR SLEEPY	$4.517 \times 10^{-07}$	$2.063 \times 10^{-09}$

Table 6 describes the power analysis of Full adder circuit for conventional and proposed techniques using 16nm CMOS technology.

## CONCLUSION

In this paper, the half adder and full adder circuits are designed using the proposed leakage power reduction techniques such as Lear Sleepy and Lear Sleeper techniques in 32nm, 22nm and 16nm CMOS technologies to reduce the leakage power in both active and sleep mode. The leakage power dissipated by the half adder, full adder circuits are reduced up to 80% when compared with the conventional and existing design in CMOS technologies.

## REFERENCES

- [1] Asif Jahangir Chowdhury (2012), Leakage Reduction Method for Ultra Low Power VLSI Design for Portable Devices", 2nd International Conference on Power, Control and Embedded Systems.pp.501-506.
- [2] Daya Sagar.CH, Krishna Moorthy.T, (2012) "Design of a Low Power Flip-Flop Using MTCMOS Technique", International Journal of Computer Applications & Information Technology Vol. 1, No.1, July.pp.347-378.
- [3] Dilip. b, Surya PrasAd.p & Bhavani.r.s.g, "Leakage power reduction in cmos circuits using leakage control transistor technique in nanoscale technology".Vol-2 Iss-1, 2012.pp.72-76.
- [4] Hina malviya, SudhaNayar C.M Roy (2013), "A new approach for Leakage Power Reduction Techniques in Deep Submicron Technologies in CMOS circuit for VLSI Applications".
- [5] Hina malviya, Murli Manohar Hinnwar (2013), " Comparison of Various Leakage Power Reduction Techniques for CMOS Circuit Design", International Journal of Engineering Research & Technology (IJERT) Vol. 2 Issue 10, October.
- [6] Ravi.T, Kannan.V "Modeling and performance analysis of ballistic carbon nanotube field effect transistor (CNTFET) "International Conference on Recent Advances in Space Technology Services & Climate change– RSTS&CC 2010, November-2010, pp. 327-331.
- [7] Kalyani.K, dr.sathiskumar.P, drragini.k (2013),"Various low power techniques for CMOS circuits", journal of engineering research and applications pp.330-333.
- [8] Kanika Kaur and Arti Noor (2011) "A review strategies & methodologies for low power VLSI designs", International Journal of Advances in Engineering & Technology.
- [9] Ravi.T, Kannan.V "Effect of N-type cntfet on double edge triggered D flip-flop based PISO shift register" International Conference On Emerging Trends in Science Engineering and Technology: Recent Advancements on Science and Engineering Innovation - INCOSSET 2012, Dec-2012 pp. 344-349.
- [10] Kuldeep Niranjana, Sanjay Srivastava, Jaikaran Singh, Mukesh Tiwari (2012), "Comparative Study: MOSFET and CNTFET and the Effect of Length Modulation", International Journal of Recent Technology and Engineering (IJRTE) ISSN: 2277-3878, Volume-1, Issue-4, October.
- [11] Leela Rani.V, Madhavi Latha.M, SaiRamesh.A (2012), "Galeorstack- A Novel Leakage Reduction Technique for Low Power VLSI Design", International Journal of Computer Applications (0975- 888)Volume 48 –No.8, June 2012.
- [12] Ravi.T, Kannan.V "Design and analysis of N-type CNTFET double edge triggered D flip-flop based SISO shift register" International Conference on Nanoscience, Engineering and Technology, ICONSET 2011, Nov -2011, pp. 724 – 728



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