Delta- Sigma Modulator with Signal Dependant Feedback Gain

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Abstract— Higher order Delta-Sigma Modulator (DSM) is basically an unstable system. The approximate conditions for stability cannot be used for the design of a DSM for industrial applications where risk is involved. The conventional second order, single stage, single bit, unity feedback gain , discrete DSM cannot be used for the normalized full range (-1 to +1) of input signal since the DSM becomes unstable when the modulus of the input signal is above 0.55. The stability is also not guaranteed for amplitude of input signal less than 0.55. In this proposal, the conventional second order DSM is modified with input signal dependant feedback path gain. The proposed DSM is suitable for industrial applications where one needs the digital representation of the analog input signal, during each sampling period. This first configuration of proposed DSM can operate for the full range of input signal without causing instability. In order to improve the SNR of first configuration, it is combined with conventional second order DSM and proposed the second configuration of DSM.

I. INRODUCTION

In the conventional discrete second order DSM [1],[2] and [3] the sampling of input signal and DSM operation is performed by single clock signal with period T_C and is shown in Fig.1. The block D is the delay unit of one clock period (T_C) and the block Q is binary quantizer. In Fig.1, $x(i)$, $x_1(i)$, $x_2(i)$ and $y(i)$ represent the ith sample of input signal, first integrator output, second integrator output and quantizer output respectively. The quantization error signal during ith sampling period is denoted as $e(i)$.
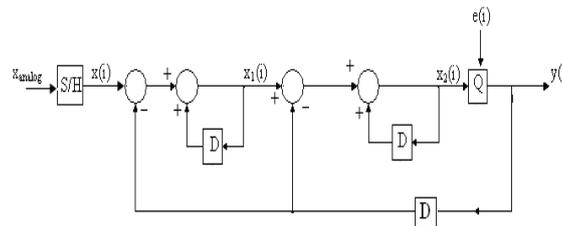

Fig.1 - Conventional Second-Order DSM

The difference equation governing the second-order DSM, is given by,

$$Y(i) = x(i) + e(i) -2e(i\text{-}1) +e(i\text{-}2) \qquad (1)$$

The average value of the digital output during update period T_U ($T_U \gg T_C$) , is equal to the average value of the discrete input signal during the same period. The DSM becomes unstable when the modulus of the input signal is above 0.55.

In [4] is proposed a method for achieving adaptive reduction in the order of the loop filter of usual high-order, single-stage, single-bit DSM in order to improve the stability range and SNR. The resulting DSM recovers from instability, with extended input range when compared to the corresponding conventional DSM but the SNR starts falling down when the input signal amplitude exceeds 0.55.

According to [1] and [5] loop stability is obtained by feed forward coefficients and feedback coefficients and are added to optimize quantization noise response in base band. By using multiple feed forward and feedback features into second order structure, more flexibility is obtained for improving stability and improving dynamic range.

In the research papers [6] and [7] is proposed a single-loop DSM with extended dynamic range. It employs an auxiliary quantizer to process the quantization error of the main quantizer. This simple addition guarantees improved stability over a wider signal input range and also reduces the sensitivity to the front-end DAC nonlinearity.

In [8] is proposed Sturdy MASH (multi-stage noise shaping) DSM which provides reduced sensitivity to circuit non-idealities but not stable for the full range of input signal. The Sturdy MASH becomes unstable when the input signal is around -2dB. In [9] is proposed Mixed order sturdy MASH DSM which also provides better reduced sensitivity to circuit non-idealities but becomes unstable when the input signal is around -3dB.

Pui-Kei Leong *et. al.* in [10] describes the design and implementation of low power Delta-Sigma digital pulse width modulation controller for switching converters which can operate at high frequency. Smaller quantizer with a limiter is used in the digital Delta-Sigma modulator to minimize the area consumption. The resulting SNR after implementation is decreased when the input amplitude is higher than 0.9FS.

Jiaxin Ju *et. al.* in [11] presented a low voltage switching capacitor DSM and focused on the implementation of unity gain and conventional DSM which could reduce the requirement of operational amplifier DC gain and was able to reduce the circuit complexity, power consumption and area. However, the SNR falls when the normalized input signal exceeds -3dB.

In the research paper [12] is proposed single-loop DSM with extended dynamic range which provides spurious free dynamic range of 87.5dB.

In [13] is presented, describing function approach to study the overload of multibit quantizer. For dc signal, when the magnitude of input is greater than 0.8, the DSM becomes unstable. In the present proposal, the proposed DSM can function for the full range of input signal. The input signal can be dc or sine signal.

In [14] is proposed an approach to find the modulator which maintains its performance like stability, SNR etc. against the parasitic effects. The SNR falls when the input is around -3dB. In the present proposal, the SNR never falls after certain range of input signal. The SNR increases steadily for the full range of input signal.

Two configurations of DSMs are proposed (DSM1 and DSM2). In the proposed DSM1, the demodulated signal closely follows the sampled analog input signal for the entire normalized range -1 to +1. The maximum value of the error signal is 0.8mV (0.08%). The SNR never falls after certain range of input signal. The SNR steadily increases and reaches the maximum value at Full scale. In the power spectral density (PSD) the noise level is much below the signal level and so the noise can be easily filtered out from the signal. The second configuration DSM2 is the combination of DSM1 and conventional DSM. In DSM2, the SNR is maximized for the entire range.

II. BLOCK DIAGRAM OF PROPOSED DSM OF CONFIGURATION 1 (DSM1)

The block diagram of the proposed second order DSM1 is shown in Fig.2. The sample and hold circuit S/H1 samples the input signal at a sampling period T_C and is denoted as $(x)_{TC}$. $(x)_{TC}$ is fed to the input of DSM. The S/H2 circuit samples the input signal at a sampling period T_U and is denoted as $(x)_{TU}$. The feedback gain is $n \times (x)_{TU} (n>1)$. In [14] the input signal fed to the DSM is dc being it is sampled at T_U. In this proposal, the input signal is sampled at T_C as in the case of conventional DSM, the operating period of DSM2 is proportional to $(x)_{TU}$ and the DSM circuit is operating at T_C.
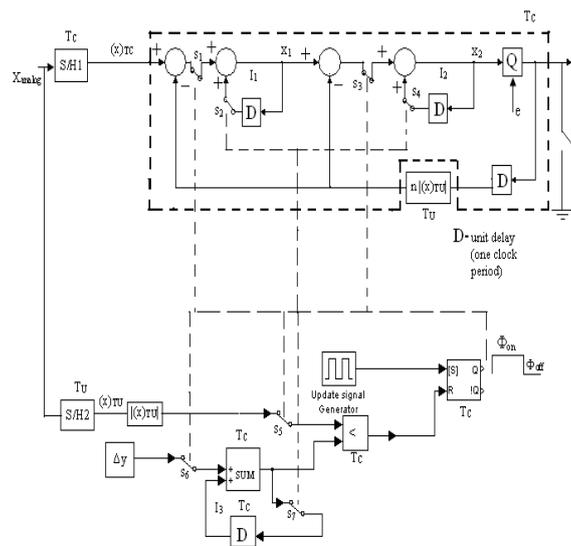

Fig. 2 - Proposed DSM1 with signal dependant feedback gain

During each update period, the bit stream at the output of quantizer gives the digital representation of input signal. The average value of bit stream at the output during each update period is equal to the average value of sampled input signal. The normalized value of y (ny) is equal to the normalized input signal (x/n). In the proposed DSM, the output of first summing unit is equal to $(x)_{TC} - n \times (x)_{TU}$ (if $y(k)=1$) and this quantity is much less than the output of first summing unit in the conventional DSM ($(x)_{TC}-n$). This fact makes the outputs of the integrators much less. The proposed modulator increases the input signal range to full scale. The upper bound of the state variable x_2 never overloads the quantizer and hence the proposed DSM is stable for the complete range of the input signal. The dynamic range, SNR in the higher range and PSD are better than the conventional DSM and DSMs proposed in the referred papers.

A. Relation between Input and Output in the Proposed DSM1

The operating time, T_O of the DSM circuit during each update period is varied proportional to $|(x)_{TU}| = x$ .Therefore,

$$T_O = k \, | \, x \, |$$
(2)

where k is the constant of proportionality. Substituting in equation (2) that when $| \, x \, | = | \, x_{max} \, | = n$, $T_O = T_U$ results in $k = \dfrac{T_U}{n}$. Substituting the value of k in equation (2), gives the value of T_O as;

$$T_O = \frac{| \, x \, | \, T_U}{n}$$
(3)

The average value of the DSM output during T_O (y') is equal to the average value of input samples divided by $n \, |x|$ during T_O. Therefore,

$$y' = \frac{(\sum_1^N x_m)/N}{n \times | \, x \, |}$$
(4)

where N is the number of samples during T_O. By definition, the average value of the output signal during T_O is given by,

$$y' = \frac{N_p \times T_C}{T_O}$$
(5)

where N_P is the net number of pulses at the output. Therefore,

$$\frac{N_p \times T_C}{T_O} = \frac{(\sum_1^N x_m)/N}{n \times | \, x \, |}$$
(6)

Substituting, $T_O = \dfrac{| \, x \, | \, T_U}{n}$ in equation (6), N_P can be given as

$$N_p = \frac{T_U}{T_C} \frac{(\sum_1^N x_m)/N}{n^2}$$
(7)

The average value of output (y) during an update period is given by,

$$y = \frac{N_p T_C}{T_U}$$
(8)

Substituting the value of N_p from equation (7) in equation (8), y is given by,

$$y = \frac{(\sum_1^N x_m)/N}{n^2}$$
(9)

Therefore, the average value of the output is proportional to the average value of input. The normalized value of y (yn) is equal to the normalized value of input which is given by $\dfrac{(\sum_1^N x_m)/N}{n}$ ..

B. Simulation Results of Proposed DSM 1

The simulation results of third order DSM1 for dc signal are shown in Fig.3.The integrator outputs never increase abruptly and hence the DSM is stable for the full range of input signal. The quantizer output is a sequence of pulses of amplitude +1 and -1 and never remains constantly at +1 or -1which proves that the proposed DSM is stable. The error signal for dc input is 0.7µV. The simulation results of third order proposed DSM1for sinusoidal signal is shown in Fig.4. Fig. 4(b) to Fig. 4(e) show the different outputs of proposed for sine signal of normalized peak amplitude 1 and frequency 45Hz which is shown in Fig. 3(a). From Fig.4(b), Fig.4(c) and   Fig. 4(d) it is evident that the integrators output never increase abruptly. The upper bounds of the integrator outputs are well within the safe limits. Fig.4(e) shows the output of the quantizer of proposed DSM. The output is a sequence of pulses of amplitude +1and -1, confirming the stable operation of the circuit. Fig. 4(f) shows the normalized average value of the quantizer output during each sampling period. It can be seen that the demodulated signal closely follows the sampled analog input signal for the entire normalized range -1 to +1. In Fig. 4(g) is shown the error signal (x/n-yn) and the maximum absolute value of the error signal is 0.8mV (0.08%).
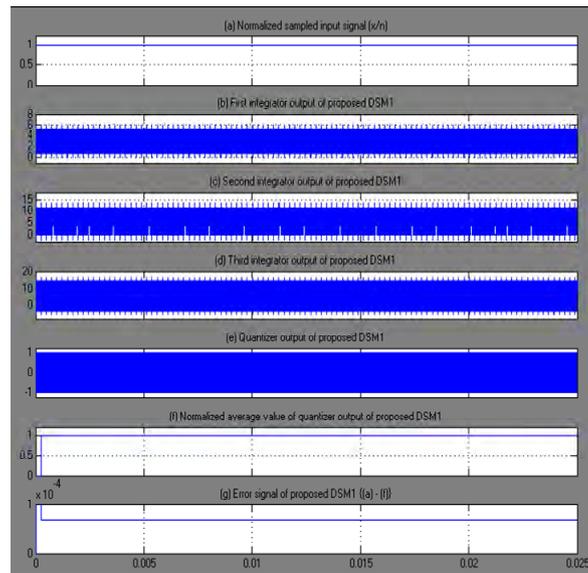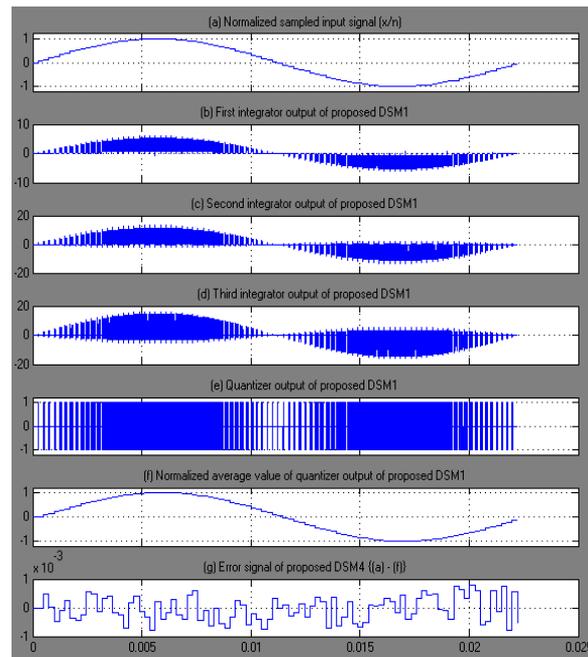

Fig.3 - Outputs of Proposed DSM1 for Sine Signal [Horizontal axis- Time in sec, Vertical axis- Voltage in Volts, T_U=0.2442msec, T_C=0.1µsec, x_{nor} =1 and n=1.5].

Fig.4 - Outputs of Proposed DSM1 for Sine Signal [Horizontal axis- Time in sec, Vertical axis- Voltage in Volts, T_U=0.2442msec, T_C=0.1µsec, x_{norp} =1 and n=1.5].

Fig. 5 compares the SNR of conventional second order DSM and the proposed DSM1. In the proposed DSM, the SNR never falls after certain range of input signal. The SNR increases with different slopes and reaches 75.9dB when x_{norp} is equal to 0dB.The dynamic input range of positive SNR of proposed DSM is 75dB. The maximum SNR of conventional DSM is 71.5 dB when x_{norp} is equal to -7dB and when $x_{norp} > -7$dB, the SNR falls. For $x_{norp} \le -7$dB, the SNR of proposed DSM is little less than the SNR of conventional DSM. For $x_{norp} > -7$dB, the SNR of conventional DSM falls rapidly but the SNR of proposed DSM continues to increase.
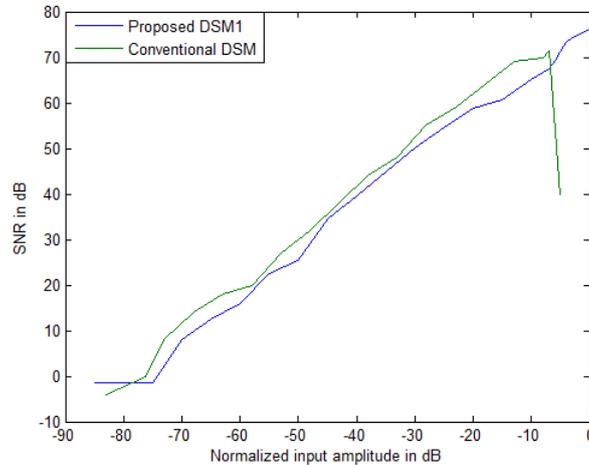

Fig.5 - Comparison of SNR of Proposed DSM1 with Conventional DSM (OSR=64, T_U = 0.2442msec, T_C = 0.1μsec, f_{sig}=45Hz)

The output of proposed DSM is passed through the running average filter. The average is taken for the update period T_U. The PSD is plotted for the output signal from the filter and is shown in Fig.6. The PSD gives the power spectrum of the voltage applied to the load. The PSD is drawn using FFT length of 4096 and with sampling frequency f_U is equal to 4.096 kHz. In the plot of PSD, the signal level is at 25 dB and the noise level is at -60dB. The signal is well separated from the noise.
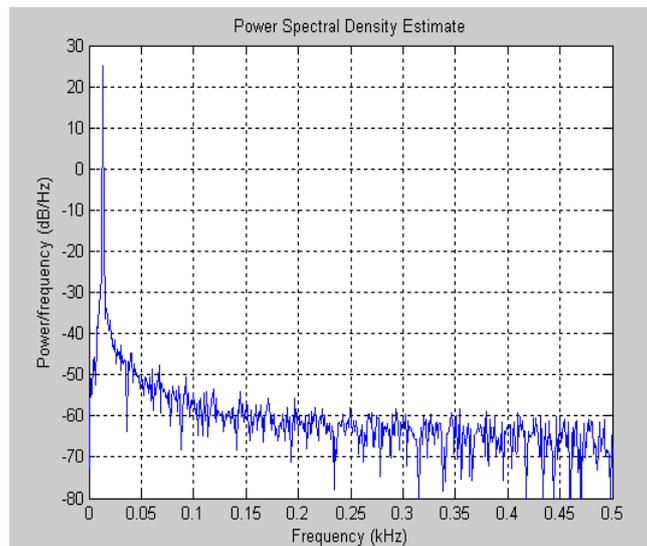

Fig.6 - PSD of proposed DSM1 (x_{norp} = 1).

In the proposed DSM1, the outputs of the subtractor units are kept under control by the feedback of $n|(x)_{TU}|$. This reason makes the DSM stable for the full range of input signal with better SNR and PSD.

III. PROPOSED DSM OF CONFIGURATION 2 (DSM2)

DSM2 is the combination of DSM1 and conventional DSM. When $|x_{nor}| \le 0.55$ (-5dB) it functions as conventional DSM and when $|x_{nor}| > 0.55$ it functions as proposed DSM1. The idea is to maximize the SNR and keep the DSM stable for the complete range.

The block diagram of proposed DSM2 is shown in Fig.7. When $|x_{nor}| \le 0.55$, RS1 flip-flop is set and output Q is in phase Φ_1. During Φ_1, x_{analog} is sampled at T_U and is fed to DSM. During Φ_1, the switch SW1 connects 0V to the input of control circuit, SW2 disables RS2 and SW3 connects the feedback gain n^2 in the feedback circuit. In short, if $|x_{nor}| \le 0.55$, the circuit is operating as DSM1. When $|x_{nor}| > 0.55$, RS1 flip-flop is

reset and output Q is in phase Φ_2. During Φ_2, x_{analog} is sampled at T_U and is fed to DSM. During Φ_2, the switch SW1 connects x_{analog} to S/H2 of control circuit, SW2 enables RS2 and SW3 connects the feedback gain $n|x|$ in the feedback circuit. If $|x_{nor}| > 0.55$, the circuit is operating as DSM2. DSM3 is stable for the full range (x_{nor} varies from -1 to +1). In the lower range ($|x_{nor}| \leq 0.55$) the SNR of DSM3 is better than the SNR of DSM2.
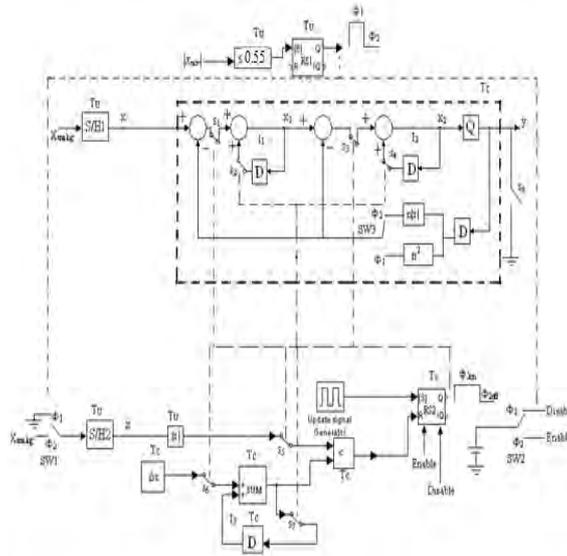

Fig.7 - Proposed DSM combined with conventional DSM.

In DSM2, y is proportional to x in each sampling period. When operating as conventional DSM, the normalized value of y is equal to $ny = n\left(\dfrac{x}{n^2}\right) = \dfrac{x}{n}$ = normalized input. When operating as DSM1, $ny = \dfrac{x}{n}$ as given by equation (9). Therefore, in DSM2 the normalized output is equal to normalized input for the entire range of normalized input signal (-1 to +1). DSM2 is stable for the full range of input signal. Since it is a combination of conventional DSM in the stable range and DSM1, the overall SNR of DSM2 is better than DSM1 and conventional DSM.

The SNR plot of proposed DSM2 is shown in Fig.8. For $|x_{nor}| \leq 0.55$, the SNR plot is same as that of conventional DSM and for $|x_{nor}| > 0.55$, the SNR plot is same as that of proposed DSM1.For the full range, the proposed DSM2 has better SNR compared to proposed DSM1 and conventional DSM.
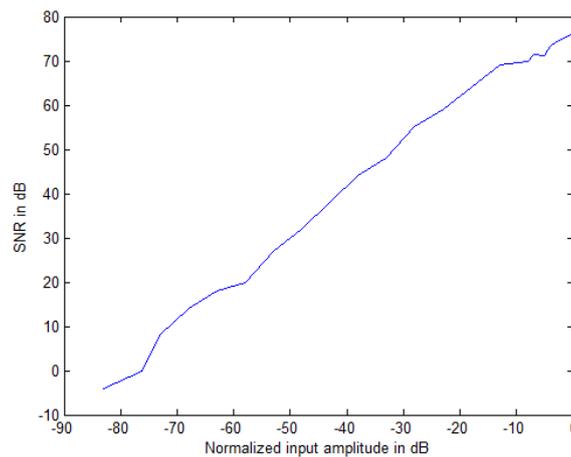

Fig.8 - SNR plot of proposed DSM2

IV. CONCLUSION

The proposed two configurations of DSMs can function for the full range of input signal and remain in stable condition. In the proposed second configuration, the SNR is maximized for the full range of input signal. In the PSD of both the configurations the noise level is well below the signal level.

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