A Transistor Sizing Tool for Optimization of Analog CMOS Circuits: TSOp

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Abstract—Optimization of a circuit by transistor sizing is often a slow, tedious and iterative manual process which relies on designer intuition. It is highly desirable to automate the transistor sizing process towards being able to rapidly design high performance integrated circuit. Presented here is a simple but effective algorithm for automatically optimizing the circuit parameters by exploiting the relationships among the genetic algorithm's coefficient values derived from the analog circuit design variables. Simulation results demonstrate that the proposed algorithm (TSOp) converges to optimal solutions efficiently for the circuits which contain discrete or discontinuous parameters constraints in a large search spaces. The robustness of TSOp has been verified by using a cascaded amplifier assisted inverter and an operational amplifier circuitries based on TSMC 0.25um process technology. Even though with a large number of design variables, TSOp successfully converges to a range of optimum solution for the targeted circuit performance. TSOp achieves optimum solutions and simplifies the design steps in developing an analog circuit, thereby significantly improving the time to market for an integrated circuit chip.

Keyword-Optimization, Transistor sizing, Analog design, CMOS circuit, Genetic algorithm, Pspice

I. INTRODUCTION

Transistor size will influence the speed of circuit, energy consumption, total area of circuit, and the delay constraints. Analog designers are tasked to taking large and small signal models of circuit components, and in order to fulfill certain performance requirements, deducing the components input parameters in accordance to output constraints. For example, given output performance measurements like gain, gm, unity gain bandwidth, wc, phase margin, ǿ, they must correspondingly produce the input MOSFET parameters, e.g. the length, L, and width, W and the input current, I. The process of translating the performance measurements into component parameters is called circuit sizing. In a modern analog design process, designers need to specify between 10 to 100 input parameters in order to achieve up to 20 output performance measurements [1]. Several automated and manual methods for circuit sizing exist in practice[1-4]. The manual method involves a designer using his or her own accumulated knowledge of circuit behavior to iteratively adjust the component parameters such that they satisfy a set of first order transistor models, and then test the accuracy of these models. This manual method is low in productivity and difficult to find an optimum solution for large circuit with more design parameters. For automated method, most of the previous researches use commercial computer aided design (CAD) software which is fast and easy to use [5-7]. However, most of the commercial software are expensive and have less flexibility to add on additional required features in optimization process. This paper introduces a simple but effective algorithm (TSOp) evolved from genetic algorithm (GA) for optimizing the circuit design parameters. PSPICE, one of the oldest and the most famous circuit level simulators [8], provides the design variables. The variables will be encoded in order to be processed by TSOp. The design variables formed as TSOp's coefficient values. The coefficient values will be evolved using techniques inspired by natural evolution, obtaining from GA. The proposed algorithm converges to a range of optimum solution for the targeted circuit performance.

The remainder of this journal is divided into five sections. In Section II, we present the main analog circuit design variables. The methodology of MATLAB in circuit modelling is presented in Section III. The evolution of the proposed TSOp is presented in Section IV. The results and discussions are presented in Section V. Section VI concludes this work.

II. ANALOG CIRCUIT DESIGN VARIABLES

The Complementary Metal-Oxide-Semiconductor (CMOS) Op-Amp is the most versatile and widely used component in analog electronic [2]. It consists of coupled differential amplifiers, providing a high voltage gain, high input impedance, and low output impedance. In the case of evolutionary design of bipolar amplifiers such as bipolar transistor-based circuits, the designer’s creativity is usually applied to the conception of different circuit topologies. For CMOS design, the creativity is used to set the transistor’s sizes of a particular topology, and as a consequence, determines the transistors operating region [5]. This is defined as the cell sizing or transistor sizing.

When cell sizing is performed, each point of the design space consists of the transistors' sizes, biasing current and compensating capacitance of a target circuit topology [5]. By setting the transistors' sizes and biasing currents, the Metal-Oxide-Semiconductor (MOS) transistors operating regions are determined [9]. MOS transistors may operate in strong, weak, and moderate inversion. The strong inversion region, in which voltage between Gate to Source (VGS) and Threshold voltage (VTN) is greater than 0.2 volts, is the most commonly used device in analog design [10]. The weak inversion region, in which VGS – VTN is around 100 mV, is characterized by the low power consumption of the device, is usually employed in micro-power applications. Nonetheless, the use of this operating region also results in the following drawbacks: low speed of the device, increase in its area, and reduction of the load driving capacity. Another way to characterize the weak inversion region is through eq. (1) which is created in [5].

$$I_D < 2nB(U_T)^2 \quad (1)$$

Where ID is the drain current, B is proportional to the transistors' dimensions width per length, W/L , UT is the thermal voltage (26mV at 300K), and n takes values between 1 and 1.5. The moderate inversion region is intermediate between the weak and the strong inversion regions.

III. GENETIC ALGORITHM IN CIRCUIT MODELING

GA is a stochastic combinatorial optimization technique introduced by Dr. J. Holland in 1975 [8]. At the beginning of GA, representations for possible solutions, which are often called chromosomes or individuals must be developed [11]. Chromosomes in a generation are forced to evolve toward better ones in the next generation by three basic GAs operators, reproduction, crossover, and mutation, and the problem-specified fitness function [12]. GA searches the solution space of a function through the use of simulated evolution, i.e. the survival of the fittest strategy. In general, the fittest individual of any population tends to reproduce and survive to the next generation, thus improving successive generations [13-14].

In the field of automated circuit design, GA has been previously used as a standalone method in generating both the topology and components of a circuit. In [15] had shown that, given the number of inputs and outputs of the circuit, sets of available components, and a fitness measurement in terms of performance, GA tended to perform satisfactorily in synthesizing eight different analog circuits. Nevertheless, the computational cost for solving the sizing problem becomes less feasible for more complex circuits such as op-amps, which require more stringent constraints and therefore larger dimension. In order to improve computation speed, researchers in [16] decoupled the circuit synthesis problem into two different stages: topology design, and component parameter selection. The two stages hybrid GA uses evolutionary techniques to choose the topology of the first circuit, and then numerical optimization is used to size the circuit components. Although the hybrid GA exhibits a performance improvement in linear analysis, non-linear analysis continues to consume a significant chunk of computational power in the numerical optimization stages.

IV. THE EVOLUTION OF TSOP

The process of developing TSOp splits into three stages as shown in Fig. 1; they are circuit design, linking circuit information with MATLAB and GA optimization. Usually, GA will generate first population randomly. However, in transistor sizing, the first population is populated with parameters that are known to have a range close to the desired value. One of the most important aspects in choosing a particular chromosome representation is from the amount of knowledge a circuit designer has. This will lead to a quicker convergence in the appropriate range by reducing the search space. Chromosomes will be decoded into a format recognizable by PSPICE for the circuit simulation. The respective output from PSPICE will be evaluated by the fitness function. Hence, as in the general GA, the steps of selection, crossover, mutation, and the re-evaluation of fitness measures are applied iteratively until a good transistor parameter that meets the specification is found [17]. GA will choose the best fitness value which indicates the best pair of transistor parameters. PSPICE always give precise and accurate data analysis for linear and non-linear circuits. With the high accuracy of PSPICE simulation, the result from the developed algorithm will be evaluated faster due to lesser generation needed. The developed algorithm provides a generic solution which can be applied in different design environment and does not constraint in one particular circuit design or technology.

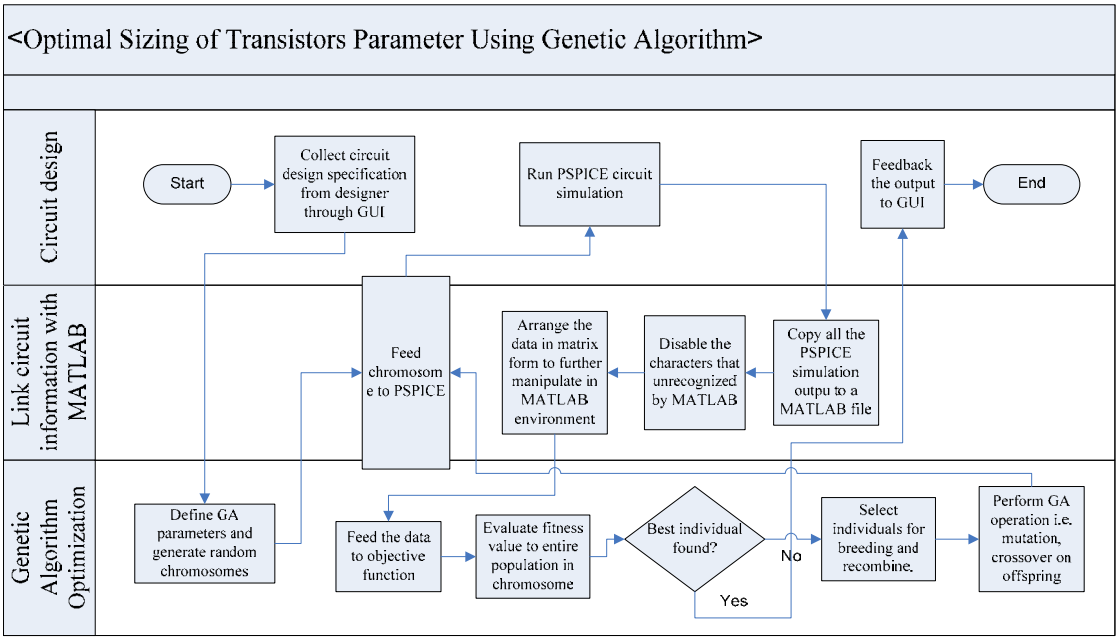

Fig. 1: Flow chart of proposed design strategy of TSOp

A. *Design of Data Handling between PSPICE and MATLAB*

The data handling interface will be developed in order to call PSPICE to simulate the circuit written in netlist. A temporary m-file will be created to copy the data through looping technique from PSPICE simulation output. MATLAB will recognize all the necessary character in the log file and fit the corresponding data in matrix form. The data will be kept according to the MATLAB format so that it can be manipulated later in GA environment.

B. *Chromosome Setup*

One of the important aspects of GA is the choice of how to encode a solution. In this case, the transistor parameter will be represented as a chromosome. The encoding can directly affect the ability of the iterative process to converge on an appropriate solution. GA will process information of component values such as resistor values and transistor sizes. So the values or parameters of a transistor can be fitted into a chromosome as shown in Fig. 2. Each gene represented one of the transistor parameter and had two fields: width and length of transistor which will be multiply with micro meter, µm. Finally, output current, Iout will be inserted in to the chromosome as the last variable.

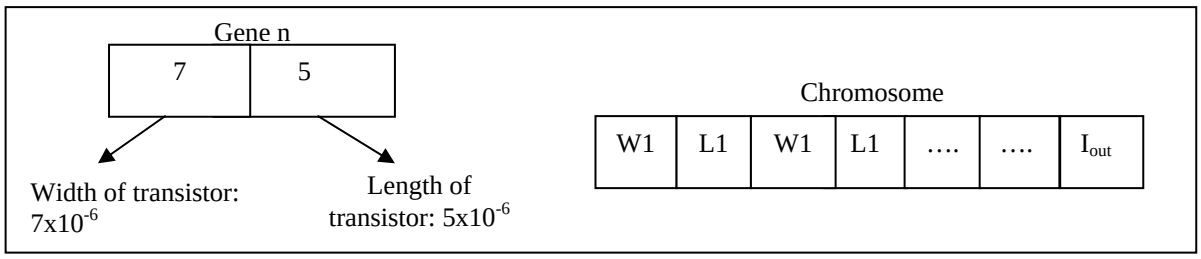

Fig. 2: Encoding for a transistor width as 7µm and length as 5µm and using binary encoding technique.

C. *Fitness function to measure the output performance*

Eq. 2 is used in [15] as the fitness function to evaluate output variable. From this fitness value, the optimized value from the corresponding parameters can be determined. In this paper, the maximum output current of the circuit will be the parameters of optimization.

$$f(x) = \frac{f(xi)}{\overline{F(x)}} + 1 \qquad (2)$$

Where

f(xi) is the output value of one chromosome

$\overline{F(x)}$ is the summation of chromosomes in the whole population

1 is a constant and is used to ensure the fitness value is always positive

D. GA Optimization

The developed algorithm starts with a number of eight chromosomes and has a maximum generation of 50. Generation gap is set to 1.0 to ensure that the same amount of chromosomes will be created when GA proceeds to the next generation. The technology used is TSMC 0.25um process where transistor parameters changes from 0.25µm to 3.0µm. For each iteration, eight sets of random chromosomes will be created. The initial value of transistor parameters will be generated randomly within range of 0.1µm to 2.5µm as defined in population creation.

The chromosomes will be decoded and handled to PSPICE. PSPICE will simulate the circuit according to the input provided and generate an output. Output current, ID will be encoded into the chromosome again to perform genetic evolution. The chromosome will be evaluated by objective function.

After that, data created will be iterated to perform selection, recombination and mutation. The fitness value of each iteration will be plotted until reach the maximum of the simulation.

V. RESULTS AND DISCUSSIONS

In this section, the GA optimization system will be applied to two practical analog circuit sizing problems. The purpose of these examples is to test the ability of the system handle large search spaces in electronics circuit.

A. Cascaded Amplifier Assisted Inverter

The cascaded amplifier assisted inverter is shown in Fig. 3. Output of the inverter is amplified using cascaded amplifier setup that is transistors M3 and M4. Output current at resistor, R2 will be taken as output and analyzed in GA. Fig. 4 shows the effect of ID and VGS by using different sets of the transistor parameters. Varying the transistor parameters will vary the Id and eventually lead to a change to the switching time of the circuit.

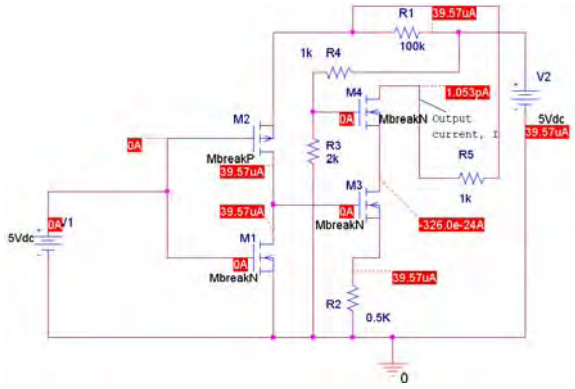

Fig. 3: A cascaded amplifier assisted inverter with four transistors and eight design variables

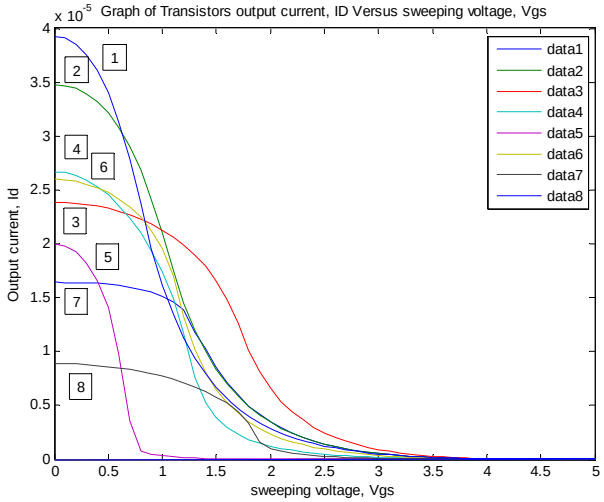

Fig. 4: Effect of circuit performance in term of output current by using different sets of parameters

The developed algorithm has analyzed eight set of chromosomes with nine variables each per iteration. Eight new born chromosomes from genetic evolution process have reinserted into PSPICE to generate the output results. Then, the fitness function is re-analyzed and the best fitness value is plotted. This process continues for

50 generations. The results are displayed in Fig. 5. The last generation of chromosome is listed in Table 1. The best chromosome with the fitness value of 1.1794 generated the output current of 1.634 µA.

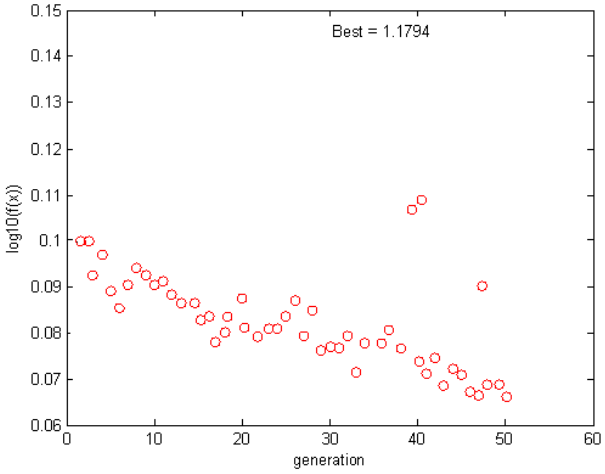

Fig. 5: Convergence of TSOp based on fitness values for the cascaded amplifier assisted inverter with nine design variables

Table 1. Eight optimized design parameters in the form of chromosome sets in last iteration

Chromo-some set	MbreakN1		MbreakN2		MbreakN3		MbreakP		Output current	Fitness value
	L_1/µm	W_1/µm	L_2/µm	W_2/µm	L_3/µm	W_3/µm	L_4/µm	W_4/µm	I_D/µm	ObjV
1	3.2055	3.2874	3.3324	1.4827	3.1131	1.5949	0.5030	1.3952	1.5920	1.1747
2	3.2055	3.2874	3.3590	1.2736	3.1131	1.5957	0.5021	1.6060	1.5860	1.1741
3	0.6555	3.2874	3.3324	1.4827	3.1131	1.5949	0.5030	0.1033	0.5980	1.0656
4	3.2061	3.2874	3.3590	1.4837	3.1136	1.5949	0.5030	0.1033	1.6340	1.1794
5	3.2055	3.2874	3.3324	1.4827	3.1131	1.5949	0.5030	0.1033	0.7228	1.0793
6	3.2055	3.2874	3.3590	1.2736	3.1131	1.5957	0.5021	1.6060	0.7228	1.0793
7	3.2071	3.5000	3.3324	1.4827	2.6881	1.5949	0.5030	0.1033	1.5320	1.1682
8	3.2071	3.5000	3.3324	1.2736	3.1131	1.6082	0.1000	1.3940	0.7228	1.0793

B. Operational Amplifier

The developed algorithm also tested in operational amplifier (op-amp) which consists of four stages of circuit. They are input stage, an intermediate stage, a level-shifting stage and output stage as shown on Fig. 6. The input stage of an op-amp is usually a pair of matched transistors configured as a dual-input differential amplifier. This balanced output is fed into another dual-input unbalance differential amplifier that serves as the intermediate stage. The output of this intermediate stage is taken from just one of the transistors and single-ended, therefore it is not balanced. The output of this input stage is taken from across the outputs of the paired transistors. The output of the op-amp is measured at resistor, R_13. Due to the mirror transistor pair, the dimension of transistor M1 is equal to M2 and dimension of transistor M3 is equal to M4. Mirror pair has equal dimension to produce balance current at the emitter. Thus, in mirror pair circuit, the number of transistors to optimize can be reduced to half.

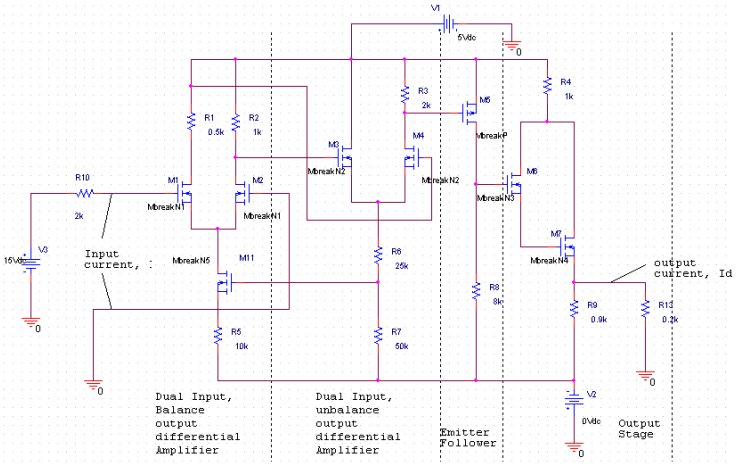

Fig. 6: An op-amp circuit with eight transistors and twelve design variables

The result of GA optimization is displayed in Fig. 7. It is observed that these eight MOSFET in the op-amp circuit were optimized after 50 generation. At the last generation, the best fitness value is 1.032 as shown by first and fourth chromosome in Table 2 with the value of 5.21 nA output current.

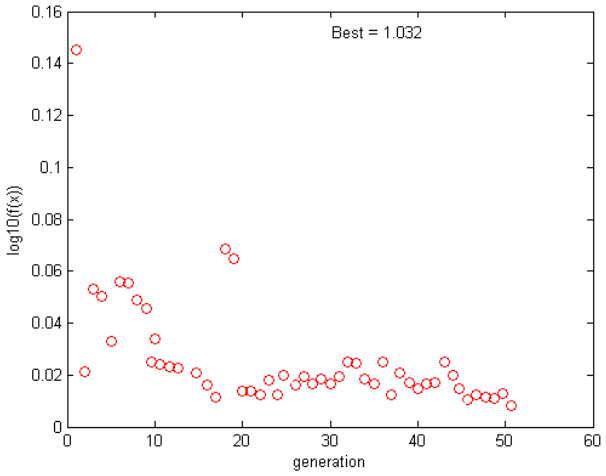

Fig. 7: Convergence of TSOp for the operational amplifier circuit with twelve design variables

Table 2: Twelve optimized design parameters in the form of chromosome sets in last iteration

Chromo-some set	MbreakP1		MbreakP2		MbreakP3		MbreakP4		MbreakP5		MbreakP6		Output current	Fitness value
	L_1/µm	W_1/µm	L_2/µm	W_2/µm	L_3/µm	W_3/µm	L_4/µm	W_4/µm	L_5/µm	W_5/µm	L_6/µm	W_6/µm	$I_{(R13)}$/µm	ObjV
1	0.1000	2.3597	1.0239	1.2256	0.7396	1.1719	0.1000	3.0000	1.3613	2.6735	1.5991	2.2822	5.21E-09	1.0320
2	1.5636	2.1009	0.3348	2.7162	2.3873	0.6485	0.3976	2.9975	0.1000	0.4205	0.8594	1.5491	1.24E-09	1.0056
3	1.5636	2.1009	0.3348	2.7162	2.3873	0.6485	0.3976	2.9975	0.1000	0.4205	0.8594	1.5491	3.67E-09	1.0226
4	1.5636	2.1009	0.3348	2.7162	2.3873	0.6485	0.3976	2.9975	0.1000	0.4205	0.8594	2.2822	5.21E-09	1.0320
5	0.1683	1.6347	0.6557	0.8630	0.7396	1.1705	0.3976	2.9975	2.4824	2.6760	1.5991	2.2822	1.24E-09	1.0056
6	0.1000	2.3597	1.0239	1.2256	0.7396	1.1719	0.1000	3.0000	1.3613	2.6735	1.5991	2.2822	1.45E-09	1.0057
7	0.1000	2.3597	1.0239	1.2256	0.7396	1.1719	0.1000	3.0000	1.3613	2.6735	1.5991	1.5491	5.17E-09	1.0318
8	0.1000	2.3597	1.0239	1.2256	0.7396	1.1719	0.1000	3.0000	1.3613	2.6735	1.5991	2.2822	1.24E-09	1.0056

VI. CONCLUSION

For optimal sizing the analog circuitry, we have presented an automated algorithm (TSOp) which has fast convergence speed and accuracy than existing method which mostly based on empirical knowledge. The developed TSOp provides a generic solution which can be applied in different design environment and does not constraint in one particular circuit design or technology. Moreover, it can be easily tailored to solve more complex circuits by changing the design parameters and fitness function. The effectiveness of the developed algorithm has also been verified by using a cascaded amplifier assisted inverter and an operational amplifier that consist of eight and twelve design variables. The results show that the optimal design parameters have successfully been converged in a short iteration time. The proposed design strategy significantly simplifies the analog design steps and achieves optimum design parameters. The reduction in design complexity is important for alleviating analog circuit design bottleneck, achieving better time to market.

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