

Analysis of Leakage Current and DC Injection in Transformerless PV Inverter Topologies

Anjali Varghese C^{#1}, Karpagam M^{*2}, Alwarsamy T^{#3}

[#] Research Scholar, Anna University, Chennai

[#] Liaison Officer, DOTE, Chennai
India

¹ anjuvicy@gmail.com

³ talwarsamy@gmail.com

^{*} Associate Professor, Hindusthan College of Engineering and Technology
Coimbatore, India

² karpagam.sathish@gmail.com

Abstract—Considering low efficiencies of solar panels, the reliability and efficiency of power electronic interface has to be ensured. Transformerless PV inverters increases the efficiency by nearly 2% and decreases cost by 25%. With no galvanic isolation comes the problem of dc injection and ground leakage current which pauses serious problems to core saturation of distribution transformers, cable corrosion, Power quality and EMI problems and has to be limited as per IEEE standards. This paper gives an analysis of leakage current flowing through the parasitic capacitance and also the DC injection in the output of the inverter. Analysis is done for various values of parasitic capacitance. Five different H-Bridge derived topologies and PWM techniques are evaluated on the basis of leakage current and DC injection.

Keyword-DC injection, Common Mode Voltage, Differential Mode Voltage, Parasitic Capacitance, Leakage current.

I. INTRODUCTION

Avoiding transformers while connecting PV inverters to grid has gained much popularity due to its increased efficiency (nearly by 2%) and decreased cost (nearly by 25%). Transformers used for isolation could either be line frequency transformers which increase the bulkiness of the system while high frequency transformers require more than one power stage and increase system complexity.

However, transformerless inverters have a serious drawback of ground leakage current which flows between the PV array and the ground through the parasitic capacitance that exists between PV cell and its frame. When the frame is grounded the parasitic capacitance exists between the PV array and ground. The common mode voltage fluctuations across this capacitance cause ground leakage current flow which initiates problems of EMI, personnel safety, power quality issues and system losses. Large ground leakage currents are formed when parasitic capacitance AC side filter inductors and grid form a resonant circuit.

To minimize the leakage current, the maintenance of constant common mode voltage is primarily required. Common mode voltage largely depends on topology of the inverter and PWM techniques.

Full bridge configuration with bipolar PWM has constant common mode voltage but with a reduced efficiency and large output current ripple. Full bridge with unipolar PWM has many advantages of increased efficiency and three level output. There are other full bridge derived structures like H5 and HERIC topologies which use additional switches for DC and AC decoupling respectively. Decoupling switches enable the disconnection of PV panel from the grid during freewheeling modes. This helps in limiting the DC link voltage ripple.

The galvanic connection between the PV system and the utility also causes DC current injection from PV system to the utility. This DC injection, according to Blewitt et al can be classified as common mode and differential mode DC current injection. Common mode DC injection is established due to the parasitic capacitance that is formed between the PV array and ground. This in turn produces ground leakage current between inverter output and DC stage. A finite DC component is thereby injected to the inverter output through this connection. Ground leakage current can be prevented by maintaining the common mode voltage constant. This can also be prevented by using various topologies and pulse width modulation (PWM) techniques. Differential mode DC injection is produced due to the asymmetrical operation of inverter switches and also due to offset errors produced by sensors and transducers. Also a differential mode voltage component is generated

within common mode component which is discussed in section II and can be avoided using equal value filter inductors. DC injection can be eliminated by using series capacitors, DC link sensors and particular topologies using DC decoupling during freewheeling modes in inverter operation[1]-[7].

The organisation of the paper is as follows: Section II contains modelling of common mode voltage . Section III gives the analysis of the five different H-Bridge derived topologies. Section IV gives the comparison and experimental analysis and Section V summarizes the conclusion obtained from the experiments.

II. COMMON MODE VOLTAGE MODEL

The galvanic connection between PV inverter and the grid pauses the problem of leakage current and DC injection. This section models the equivalent common mode voltage considering both differential mode and common mode voltage.

Fig. 1 shows the model of single phase inverter connected to the output of PV array through a DC link capacitor. L_R and L_Y are line inductors respectively and L_g is the inductor on the grid side. Parasitic capacitance can exist between PV panel and frame, represented as C_{PV} , between line and ground, as C_{LG} and between transformer windings, C_W .

Ground leakage current flows from the output of PV through C_{PV} to the ground. Since grid is also grounded, leakage current flows to the grid. For PV inverters with galvanic isolation , the stray capacitance between transformer windings offer impedance to DC current and therefore the DC injection is not much influenced by topology or PWM technique used in inverters. But in transformerless inverters since winding capacitance is absent the topology as well as modulation strategies can be effectively modified to eliminate DC injection.

The common mode voltage existing between R and Y terminals of the line is obtained where V_{CM_RY} and V_{DM_RY} are the common mode and differential mode voltage between lines R and Y respectively. V_{RN} and V_{YN} are the output voltages of the inverter with respect to the negative terminal N of the DC bus reference. V_{CM_RY} and V_{DM_RY} are defined as

$$V_{CM_RY} = \frac{V_{RN} + V_{YN}}{2} \tag{1}$$

$$V_{DM_RY} = V_{RN} - V_{YN} \tag{2}$$

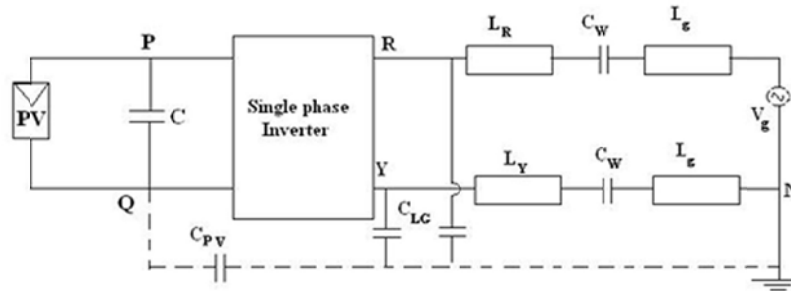


Fig 1. Common Mode Voltage Model

V_{CM_EFF} is the combination of common mode voltage between lines and the common mode voltage produced by the differential mode voltage which is influenced by the filter inductance imbalances depicted as V_{ry} .

Effective common mode voltage can be defined as

$$V_{CM_EFF} = V_{CM_RY} + V_{ry} \tag{3}$$

$$V_{ry} = \frac{V_{DM_RY}}{2} \frac{L_Y - L_R}{L_Y + L_R} \tag{4}$$

This voltage can be made zero if $L_R=L_Y$. The inverter has been designed with equal output inductors. In this paper, the DC injection measured and shown is the total DC injection in the output of the inverter[8]-[11].

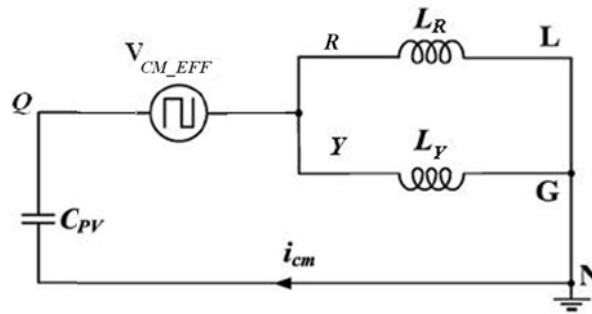


Fig 2. Model of Effective Common Mode

III. ANALYSIS OF TOPOLOGIES

This section gives an analysis of leakage current flowing through the parasitic capacitance and also the DC injection in the output of the inverter. Five different H-Bridge derived topologies and PWM techniques are evaluated on the basis of leakage current and DC injection. Transformerless inverters based on H-Bridge are chosen for their less complexity in analysis and modelling [12]-[14].

- i) H-Bridge with Bipolar Pulse Width Modulation (PWM)
- ii) H-Bridge with Unipolar Pulse Width Modulation
- iii) H-Bridge with Hybrid Pulse Width Modulation
- iv) H-Bridge Topology with DC Bypass (one Switch)
- v) H-Bridge Topology with DC Bypass (two switches)

- i) H-Bridge with Bipolar Pulse Width Modulation

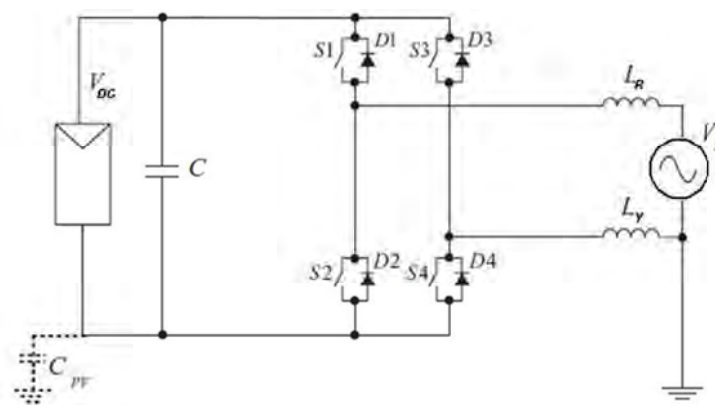


Fig 3. H-Bridge inverter Topology

S1 and S3 are switched by comparing sinusoidal signal with triangular carrier signal and S2 and S4 are switched complementarily. There is no zero output voltage state in this configuration. The filtering requirements are high in bipolar PWM. The output voltage is bipolar in nature, ($+V_{DC}$ to $-V_{DC}$ to $+V_{DC}$), and so core losses are high. Efficiency is low due to reactive power transfer between L_R , L_Y with C_{PV} .

- ii) H-Bridge with Unipolar PWM

Two legs are switched by comparing high frequency with sinusoidal and mirrored sinusoidal references. Two zero output voltage states are possible when S1, S3 = ON and S2, S4 = ON. Since the switching ripple has double the switching frequency, the filtering requirements are lowered. The output voltage is unipolar in

nature.(0 to $+V_{DC}$ to 0 to $-V_{DC}$ to 0). Losses are reduced during zero voltage states and therefore efficiency is higher than bipolar.

iii) H-Bridge with Hybrid PWM

One leg is switched at low grid frequency and the other leg is switched at high PWM frequency. Two zero output voltage states are possible: $S1, S2 = ON$ and $S3, S4 = ON$. Efficiency is high as in unipolar. The switching ripple in the current follows switching frequency and hence filtering requirements are higher.

iv) H-Bridge with DC Bypass (one Switch)

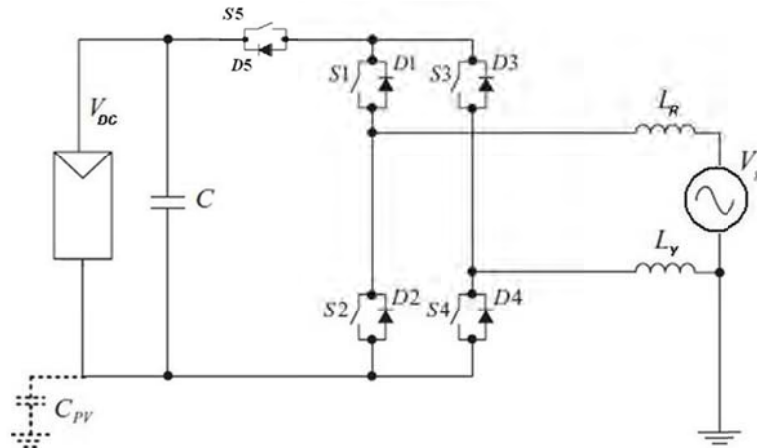


Fig 4. H-Bridge with DC Bypass (one Switch)

The H – bridge switches in this topology follow a unipolar switching pattern. Switch S5 is turned off during the freewheeling mode of the inverter. Two zero output voltage states are possible: $S1, S2 = ON$ and $S3, S4 = ON$. Efficiency is high as in unipolar. The switching ripple in the current follows switching frequency and hence filtering requirements are higher. This modulation can be used only for two quadrant operation.

v) H-Bridge with DC Bypass (Two Switches)

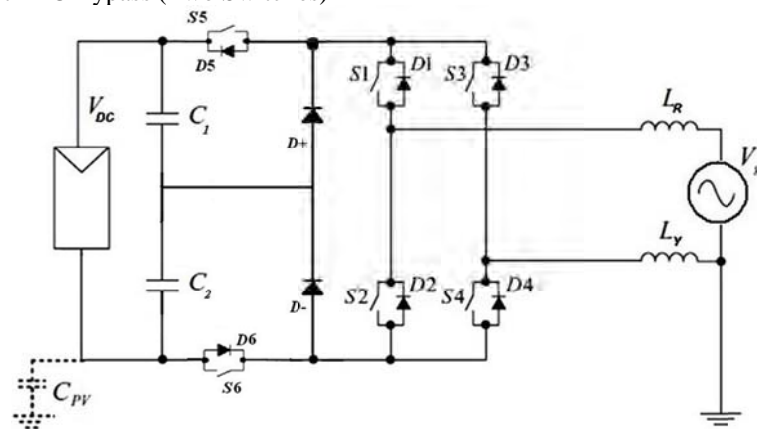


Fig 5. H-Bridge with DC Bypass (Two Switches)

The H-Bridge switches in this topology follow a unipolar switching pattern. S5 and S6 (DC Bypass switches) are turned off during zero output voltage states. The efficiency is lower than unipolar has higher filtering requirements.

IV. COMPARISON OF RESULTS

To analyze and compare the leakage current of output for the various topologies, simulations were performed in MATLAB/Simulink. Two filter inductors are placed in the line and neutral of the output as shown. Analysis is done by varying the parasitic capacitance CPV over a range of 1μF to 10μF and studying the FFT analysis and fundamental value of leakage current. Analysis of the inverter output current with varying values of

parasitic capacitance has been done. Also the analysis of effect of output inductor imbalance on DC injection has been observed. Further the effect of series capacitance connected in the output of inverter on the DC injection values has also been investigated.

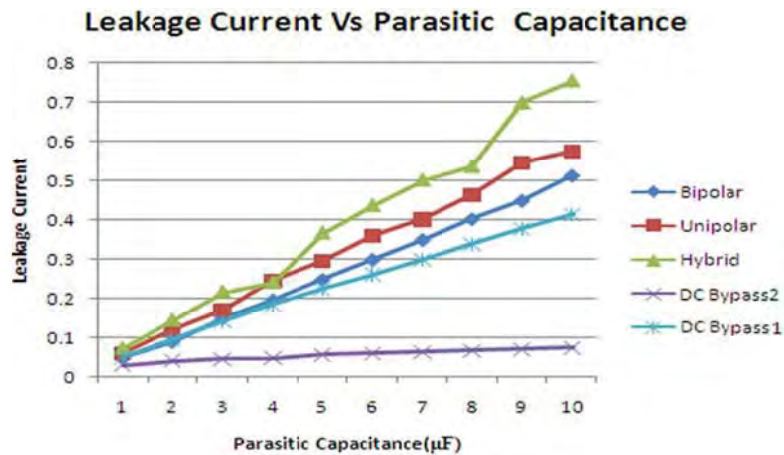


Fig 6. Leakage Current Vs Parasitic capacitance

Fig 6 shows the effect of varying parasitic capacitance on the leakage current for different topologies. This chapter evaluates 5 topologies on the basis of leakage current and shows that hybrid switched inverter has the highest leakage current and the topologies with DC bypass has lesser leakage current values. In all the topologies, the leakage current increases with increased with increasing values of parasitic capacitance.

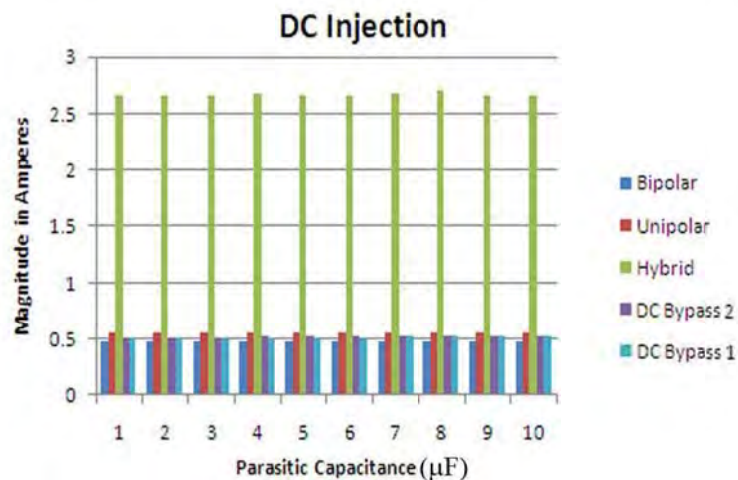


Fig 7. Comparison of DC Injection values for various topologies with varying parasitic capacitance

Fig 7 shows the effect of various topologies on DC injection with varying parasitic capacitance. It can be seen that the value of DC does not much depend on the value of parasitic capacitance but it rather depends on the PWM technique and circuit topology. As can be seen, the DC injection value is maximum for hybrid PWM topology and least for bipolar topology. The Unipolar topology has more DC injection than H-Bridge with single switch DC Bypass and H-Bridge with double switch DC Bypass topologies.

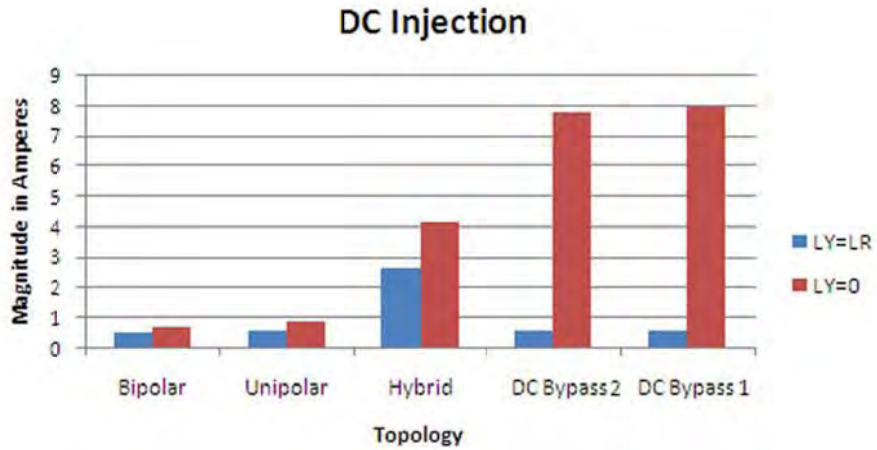


Fig 8. Comparison of DC Injection values for various topologies with varying output inductor values.

Another interesting feature can be seen in fig 8. The effect of varying the output inductors can be observed for the 5 topologies. When there is no imbalance that is when $L_Y = L_R$, the DC injection values are lesser. But when there is imbalance in the output inductor values, the DC injection has substantially increased for all the topologies. So it can be clearly stated that DC injection depends on the common mode effective voltage.

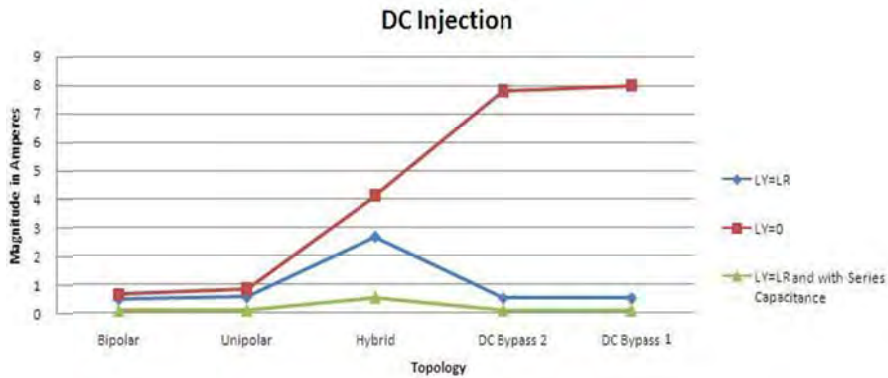


Fig 9. Comparison of DC Injection values for various topologies with varying output inductor values and output series capacitance.

When series capacitance is added to the different topologies, as seen in fig 9 the DC injection values have considerably dropped. It can be observed that DC injection values does not much depend on the value of parasitic capacitance. The value of injected DC definitely depends on the effective common mode voltage which can be adjusted by the balance of output inductors.

TABLE I
Comparison of Topologies

Topology	Parameters				
	Leakage Current	DC Injection	Common Mode voltage V_{CM}	Effective Common Mode Voltage V_{CM_EFF}	
				$L_Y=L_R$	$L_Y=0$
H-Bridge with Bipolar PWM	Low	Low	$V_{DC}/2$	$V_{DC}/2$	$0, V_{DC}/2$
H-Bridge with Unipolar PWM	High	High	$0, V_{DC}/2$	$0, V_{DC}/2$	$0, V_{DC}$
H-Bridge with Hybrid PWM	Highest	Highest	$0, V_{DC}/2$	$0, V_{DC}/2$	$0, V_{DC}/2, V_{DC}$
H-Bridge with DC Bypass (one Switch)	Low	Low	$V_{DC}/2$	$V_{DC}/2$	$0, V_{DC}/2, V_{DC}$
H-Bridge with DC Bypass (two Switches)	Lowest	Lowest	$V_{DC}/2$	$V_{DC}/2$	$0, V_{DC}/2, V_{DC}$

V. CONCLUSION

This work evaluates five different transformerless topologies on the basis of leakage current and DC injection. It can be seen from the analysis that DC decoupling of the inverter during freewheeling tends to reduce the leakage current as well as DC injection. Moreover DC injection can be reduced by using equal values of output inductors which indicates the dependence of DC component on the common mode voltage values. Among the H-Bridge derived transformerless topologies, DC decoupling is suggested for use in grid connected PV systems. Table I summarizes the result of analysis and shows that variation in common mode voltage accounts for high leakage current values and also imbalance in output inductors causes wide variations in effective common mode voltage.

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