Noise Reduction of Fractional Source in Cryogenic Current Comparator Bridge

C. Jassadajin [#1], C. Kurupakorn [#2], N. Khumthukthit [#3], A. Pruksanubal [*4]

[#] Electrical Metrology Department, National Institute of Metrology (Thailand)
3/4-5 Moo 3, Klong 5, Klong Luang, Pathumthani 12120 THAILAND
[1] chaiwat@nimt.or.th
[2] chatchaval@nimt.or.th
[3] natenapit@nimt.or.th
[*] Department of Electrical Engineering, King Mongkut's University of Technology North Bangkok
1518 Phiboonsongkram Road, Bangsue, Bangkok 10800 THAILAND
[4] pruksanubal@yahoo.com

***Abstract*— In this work, a resistance measurement is done at both high accuracy and precision using Cryogenic Current Comparator (CCC) bridge system [1]. A CCC bridge circuit consists of three parts: coil, current source and detector parts. There are electronic components in the current source of the system. They generate thermal noise in the measurement system. This paper shows the noise reduction in a fractional source of CCC Bridge which is a ramp generator. The bridge receives the voltage signal, which is supplied to a CCC coil to achieve the magnetic flux balance condition inside the superconductor shield, from a null detector. By analysing the noise of the circuit in the fractional part and improving the circuit, it can minimize the noise to obtain a better output of the fractional source for improved accurate and more stability. Finally, the noise can be reduced for a designed bandwidth, a unity noise gain and minimized input resistance in the circuit.**

Keyword-Noise reduction, Fractional source, Noise model, Resistance measurement, Ramp generator

I. INTRODUCTION

The fractional source of CCC bridge can be designed for low output noise, that is important for a CCC system performance. In the fractional circuit, the noise performance is important because it takes a current from the output of fractional source to calculate the results of resistance measurement during the bridge balance condition. The most important part of fractional source is the ramp generator. By using a basic of integrated circuit, the noise is modelled and analysed for more accuracy and stability of output of fractional source.

II. CCC BRIDGE SYSTEM

The CCC bridge [2] for resistance measurement is shown in Fig. 1. First part, the coils consist of primary coil (N_p), secondary coil (N_s) and fractional coil (N_f). These coils also include the superconductor shield. Second part, the current sources consist of primary source (S_p), secondary source (S_s) and fractional source (S_f). These sources are for supplying currents to the coils. Third part is the detector part, which consists of SQUID for detecting flux in superconductor shield and Null detector for detecting the voltage drop between primary side and secondary side.

When the bridge is in the balance condition, a zero flux occurs in the CCC,

$$N_p \bullet I_p = N_s \bullet I_s + N_f \bullet I_f \tag{1}$$

The Null detector is also balance,

$$R_p \bullet I_p = R_s \bullet I_s \tag{2}$$

Then

$$\frac{R_p}{R_s} = \frac{N_p}{N_s} \bullet \left[1 - \frac{N_s \bullet V_f}{N_p \bullet R_f \bullet I_p} \right] \tag{3}$$

where N_p is the turn number of primary coil, N_s the turn number of secondary one and N_f the turn number of fractional one. The fractional resistance (R_f) is fixed to be 10 kΩ and primary current (I_p) is also a fixed value and generated from a high stability primary current source. For voltage across fractional resistor (V_f) [3], it can be measured by using digital multimeter. According to Eq. 3, V_f depends on the fractional source and it must be accurate and stable. If V_f is changed, it affects the resistance ratio.

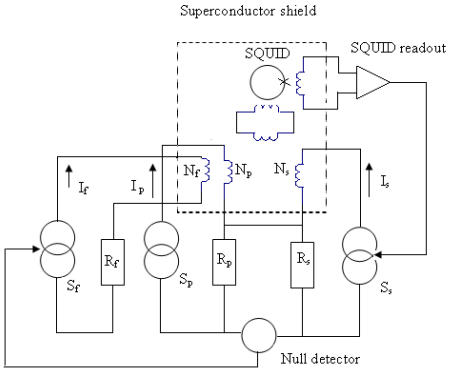

Fig. 1. Simplified schematic circuit of the CCC Bridge

In general, the fractional source (S_f) is a ramp generator [4], as shown in Fig. 2. This application of the integrator generates a ramp voltage. The input of fractional source receives the voltage signal from an analogue output of the null detector and supplies the current output passed through the fractional resistor. The voltage drop on this resistor can be measured by a digital multimeter, which must to maintain the null balance condition.

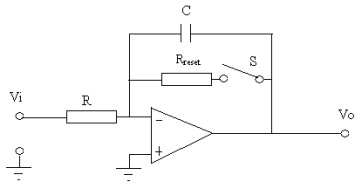

Fig. 2. Circuit of fractional source

III. NOISE MODEL

A noise voltage [5], [6] called thermal noise is generated when the thermal energy causes free electrons to move randomly in a resistive material. This noise is presented in all circuit elements containing resistance. The noise is independent of the composition of the resistance. The thermal noise in a resistor can be modelled as voltage or current. As the voltage model, it is placed in series with an otherwise noiseless resistor, while as the current model, it is placed in a parallel with an otherwise noiseless resistor, as shown in Fig. 3 (a) and (b).

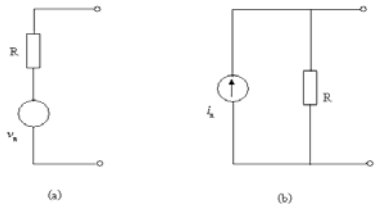

Fig. 3. (a) Voltage noise model, (b) Current noise model

The rms value of voltage (thermal) noise and current (thermal) noise can be calculated by using Nyquist's relation,

$$v_n = \sqrt{4kTR\Delta f} \tag{4}$$

and

$$i_n = \sqrt{\frac{4kT\Delta f}{R}} \tag{5}$$

where v_n is the voltage noise in volts (rms), i_n the current noise in amps (rms), k Boltzmann's constant (1.38×10^{-23} j/K), T absolute temperature (K), R the resistance in ohms and Δf is the effective noise bandwidth in Hertz.

The term 4kTR and 4kT/R are voltage and current power densities having units of V^2/Hz and A^2/Hz.

The noise in operational amplifiers (Op-amp) is generated by semiconductor shield and resistors. The op-amp used in analysis is assumed to be ideal having infinite input and zero output impedance. The equivalent circuit of op-amp noise model is shown in Fig. 4. For the standard model of an op-amp, three noise sources: v_n the amplifier noise voltage, i_{np} the non-inverting input current noise and i_{nn} the inverting input current noise are taken into account.

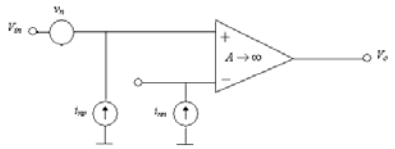

Fig. 4. Noise model for Op Amp

A. The Noise model analysis

In this case, the equivalent circuit with the op-amp integrated circuit for noise analysis [7], [8] can be shown in Fig. 5.

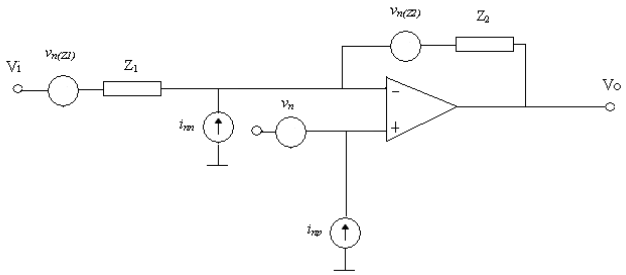

Fig. 5. Noise model for circuit of fractional source

The noise contribution of each source can be calculated by using the superposition principle. The amplifiers are not ideal in this analysis:

$$v_o = A_v \bullet v_a \tag{6}$$

$$\beta = \frac{Z_1}{Z_1 + Z_2} \tag{7}$$

$$\alpha = 1 - \beta = \frac{Z_2}{Z_1 + Z_2} \tag{8}$$

$$A_{vcl(inv)} = \frac{-\alpha A_v}{1 + \beta A_v} \tag{9}$$

$$A_{vcl(non)} = \frac{1}{\beta} \tag{10}$$

where v_o is op-amp output voltage, v_a the voltage between inverting and non-inverting inputs, A_v the op-amp open loop gain and the feedback factor (α ,β) for closed loop non-inverting gain ($A_{vcl(non)}$) and closed loop inverting gain ($A_{vcl(inv)}$).

B. Noise contribution due to Z_1

The noise contribution due to Z_1 can be calculated by using the equivalent circuit shown in Fig. 6.

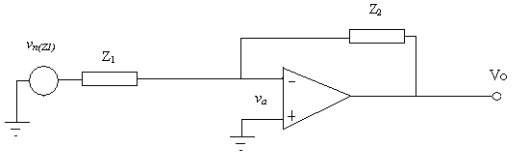

Fig. 6. Noise model for noise contribution due to Z_1

Applying KCL at the inverting input node of the op-amp:

$$\frac{v_{n(Z1)} + v_a}{Z_1} + \frac{v_{o(Z1)} + v_a}{Z_2} = 0$$

(11)

$$\frac{v_{n(Z1)}}{Z_1}+v_{o(Z1)}\left[\frac{1}{Z_2}+\frac{1}{A_vZ_1}+\frac{1}{A_vZ_2}\right]=0 \quad (12)$$

$$v_{o(Z1)}\left[\frac{1}{Z_2}+\frac{1}{A_vZ_1}+\frac{1}{A_vZ_2}\right]=-\frac{v_{n(Z1)}}{Z_1} \quad (13)$$

$$v_{o(Z1)}=-v_{n(Z1)}\frac{A_vZ_2}{A_vZ_1+Z_2+Z_1} \quad (14)$$

$$v_{o(Z1)}=-v_{n(z1)}\frac{\alpha A_v}{1+\beta A_v} \quad (15)$$

where $v_{n(Z1)}$ is the thermal noise due to Z_1 and $v_{o(Z1)}$ the output voltage resulting from the thermal noise due to Z_1.

The noise voltage due to Z_1, the closed loop gain for an inverting Op Amp configuration, this reduces to:

$$v_{o(Z1)}=v_{n(z1)}A_{vcl(inv)} \quad (16)$$

The non-inverting closed loop gain ($A_{vcl(non)}$) is referred to the "noise gain" that is a common factor for the noise to the input:

$$v_{o(Z1)}=-v_{n(z1)}\alpha A_{vcl(non)} \quad (17)$$

For ideal op-amp,

$$v_{o(Z1)}=-\sqrt{4kTZ_1\Delta f}\,\frac{\alpha}{\beta} \quad (18)$$

C. Noise contribution due to Z_2

The noise contribution due to Z_2 can be calculated by using the equivalent circuit shown in Fig. 7.

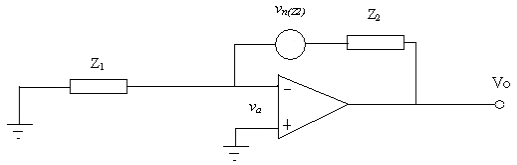

Fig. 7. Noise contribution due to Z_2

Applying KCL at the inverting input node of the op-amp:

$$\frac{v_a}{Z_1}+\frac{v_{o(Z2)}-v_{o(Z2)}+v_a}{Z_2}=0 \quad (19)$$

$$\frac{-v_{n(Z2)}}{Z_2}+v_{o(Z2)}\left[\frac{1}{Z_2}+\frac{1}{A_vZ_1}+\frac{1}{A_vZ_2}\right]=0 \quad (20)$$

$$v_{o(Z2)}=\frac{v_{n(Z2)}}{Z_2}\left[1/(\frac{1}{Z_2}+\frac{1}{A_vZ_1}+\frac{1}{A_vZ_2})\right]=0 \quad (21)$$

$$v_{o(Z2)}=v_{n(Z2)}\left[\frac{A_vZ_1}{A_vZ_1+Z_2+Z_1}\right] \quad (22)$$

$$v_{o(Z2)}=v_{n(Z2)}\left[\frac{\beta A_v}{1+\beta A_v}\right] \quad (23)$$

$$v_{o(Z2)}=v_{n(Z2)}\beta A_{vcl(non)} \quad (24)$$

In case of an ideal op-amp,

$$v_{o(Z2)}=\sqrt{4kTZ_2\Delta f} \quad (25)$$

D. Noise contribution due to v_n

The noise contribution due to v_n can be calculated by using the equivalent circuit shown in Fig. 8.

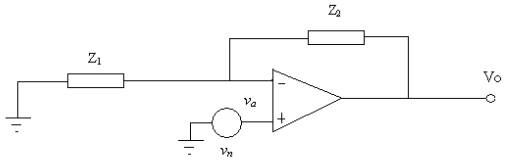

Fig. 8. Noise contribution due to v_n

The v_n is typically given in datasheet as a noise density, while the noise bandwidth is included in the representation of the noise voltage source. Apply KCL at the inverting input node of the op-amp:

$$-v_n\sqrt{\Delta f}\left[\frac{1}{Z_1}+\frac{1}{Z_2}\right]+v_{o(vn)}\left[\frac{1}{Z_2}+\frac{1}{A_v Z_1}+\frac{1}{A_v Z_2}\right]=0 \tag{26}$$

$$v_{o(vn)}=v_n\sqrt{\Delta f}\left[(\frac{1}{Z_1}+\frac{1}{Z_2})/(\frac{1}{Z_2}+\frac{1}{A_v Z_1}+\frac{1}{A_v Z_2})\right] \tag{27}$$

$$v_{o(vn)}=v_n\sqrt{\Delta f}\left[\frac{A_v(Z_2+Z_1)}{A_v Z_1+(Z_2+Z_1)}\right] \tag{28}$$

$$v_{o(vn)}=v_n\sqrt{\Delta f}\left[\frac{A_v}{1+\beta A_v}\right] \tag{29}$$

$$v_{o(vn)}=v_n\sqrt{\Delta f}\,A_{vcl(non)} \tag{30}$$

In case of an ideal op-amp,

$$v_{o(vn)}=v_n\sqrt{\Delta f}\,\frac{1}{\beta} \tag{31}$$

E. Noise contribution due to i_{nn}

The noise contribution due to i_{nn} can be calculated by using the equivalent circuit shown in Fig. 9.

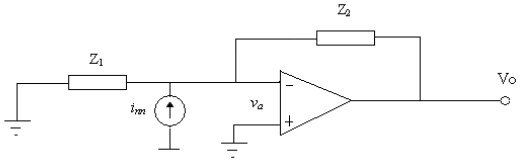

Fig. 9. Noise contribution due to i_{nn}

The i_{nn} is typically given in datasheet as a noise density; the noise bandwidth is included in the representation of the noise current source. Apply KCL at the inverting input node of the op-amp:

$$\frac{v_a}{Z_1}+\frac{v_{o(inn)}+v_a}{Z_2}-i_{nn}\sqrt{\Delta f}=0 \tag{32}$$

$$v_{o(inn)}\left[\frac{1}{Z_2}+\frac{1}{A_v Z_1}+\frac{1}{A_v Z_2}\right]=i_{nn}\sqrt{\Delta f} \tag{33}$$

$$v_{o(inn)}=i_{nn}\sqrt{\Delta f}\left[1/\left(\frac{1}{Z_2}+\frac{1}{A_v Z_1}+\frac{1}{A_v Z_2}\right)\right] \tag{34}$$

$$v_{o(inn)}=i_{nn}\sqrt{\Delta f}\left[\frac{A_v Z_1 Z_2}{A_v Z_1+Z_1+Z_2}\right] \tag{35}$$

$$v_{o(inn)}=i_{nn}\sqrt{\Delta f}\,(\frac{Z_1 Z_2}{Z_1+Z_2})A_{vcl(non)} \tag{36}$$

In case of an ideal op-amp,

$$v_{o(inn)}=i_{nn}\sqrt{\Delta f}\,Z_2 \tag{37}$$

F. Noise contribution due to i_{np}

The circuit for calculation the noise contribution due to i_{np} is shown in Fig. 10. It can be determined by inspection $v_{o(inp)} = 0$ because there is no resistance value of the noise current source to develop a voltage across.

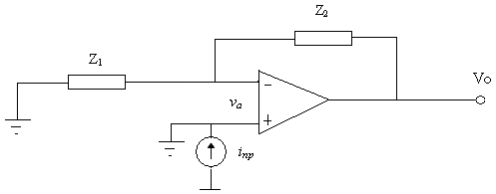

Fig. 10. Noise contribution due to i_{np}

G. Total noise

The total noise [9] can be determined by the noise contribution of each source divided by the noise gain ($A_{vcl(non)}$) to refer to the noise of the input and to figure out the noise bandwidth which are combined by the root sum square. The result of the total noise input voltage ($v_{n(in)}$) is given in the equation below.

$$v_{n(in)} = \sqrt{\Delta f}\sqrt{4kTZ_1\left[\frac{Z_2}{Z_1+Z_2}\right]^2 + 4kTZ_2\left[\frac{Z_1}{Z_1+Z_2}\right]^2 + v_n^{\,2} + i_{nn}^{\,2}\left[\frac{Z_1Z_2}{Z_1+Z_2}\right]^2} \tag{38}$$

In integrated circuit, Z_1 is R whereas Z_2 is C. Therefore the noise contribution due to Z_2 is zero since the thermal noise is generated only in the resistor components. The total noise input voltage of the integrated circuit is given in Eq. 39.

$$v_{n(in)} / \sqrt{\Delta f} = \sqrt{4kTR\left[\frac{(1/2\pi fC)}{R+(1/2\pi fC)}\right]^2 + v_n^{\,2} + i_{nn}^{\,2}\left[\frac{R(1/2\pi fC)}{R+(1/2\pi fC)}\right]^2} \tag{39}$$

The total noise output voltage ($v_{n(out)}$) can be evaluated by multiplying Eq. 39 with the noise gain in the closed loop bandwidth. For the noise bandwidth (Δf), the frequency bandwidth (*fBW*) of the op-amp can be used to determine the noise bandwidth, while the gain bandwidth product (*GBWP*) specification can be found in the op-amp data sheets. Then the noise bandwidth can be obtained by

$$\Delta f = \frac{\pi}{2} fBW = \frac{\pi}{2}\frac{GBWP}{A_{vcl(non)}} \tag{40}$$

where $A_{vcl(non)}$ is the noise gain.

IV. Calculation and Improvement

A. Noise calculation

According to the design of the integrated circuit in this work, R is 1 MΩ, C is 10 µF (integration constant = 10 s), ambient temperature is 296.15 K, while the op-amp specification is depended on the voltage noise density and the input bias current noise density such as at 100 Hz (referring to data sheet [10]), they are 8 nV/√Hz and 1.6 fA/√Hz, respectively. These can be determined as $v_{n(in)}$ and $v_{n(out)}$ in Table I.

TABLE I
Noise calculation

Noise source	Noise contribution
noise voltage due to R	20.4 pV/√Hz
noise voltage due to v_n	8 nV/√Hz
noise voltage due to i_{nn}	2.5 pV/ √Hz
Total noise input voltage, $v_{n(in)}$	8.0 nV/√Hz
Total noise output voltage, $v_{n(out)}$ at Δf=1	8.0 nV_{RMS}

When adjusting the R value of the circuit from 1 Ω to 10 MΩ at the values of C 10 µF, 1 µF and 0.1 µF, the results of the input noise voltage, output noise voltage and noise gain can be calculated and shown in Table II.

TABLE II
Results of noise calculation when the values of R and C are changed

R (Ω)	C= 10 μF			C= 1 μF			C= 0.1 μF		
	$V_{n(in)}$ (nV/√Hz)	noise gain	$V_{n(out)}$ (nV/√Hz)	$V_{n(in)}$ (nV/√Hz)	noise gain	$V_{n(out)}$ (nV/√Hz)	$V_{n(in)}$ (nV/√Hz)	noise gain	$V_{n(out)}$ (nV/√Hz)
1	8.001	160.24	1 282	8.001	1593.4	12 750	8.001	15924.6	127 400
10	8.009	16.92	135.5	8.010	160.0	1 282	8.010	1593.4	12 760
100	8.038	2.59	20.82	8.090	16.9	136.7	8.100	160.2	1 298
1 k	8.019	1.16	9.294	8.380	2.6	21.70	8.850	16.9	149.6
10 k	8.003	1.02	8.123	8.190	1.2	9.492	11.20	2.6	29.01
100 k	8.000	1.00	8.013	8.030	1.0	8.158	9.740	1.2	11.29
1 M	8.000	1.00	8.001	8.003	1.0	8.016	8.247	1.0	8.378
10 M	8.000	1.00	8.000	8.000	1.0	8.002	8.026	1.0	8.039

B. Improvement of the noise voltage of fractional source output voltage

According to the results in Table 2, the input noise voltages are depended on the value of R and the output noise voltages are depended on the noise gain, which is the relation between R and C. This fractional circuit can decrease the noise voltage by minimizing resistance value and the noise gain of circuit becomes about 1. For the circuit as shown in Fig. 2, RC of circuit has been set to be 1(ω=1) for control the bandwidth and noise gain of the circuit. After that the input voltage of 0.1 V is supplied and the voltage across 10 kΩ resistor is measured by using the nano-voltmeter. In general, the noise is a random signal which is composed of uncertainties. The test circuit has the varieties of the adjusted R which introduces the normalized output voltages. In order to compare the time and voltage, they have to be compare in the same axis. This is because it is possible to make clearer to check the deviation voltage as well as the calculation. The test results can be shown in Fig. 11.

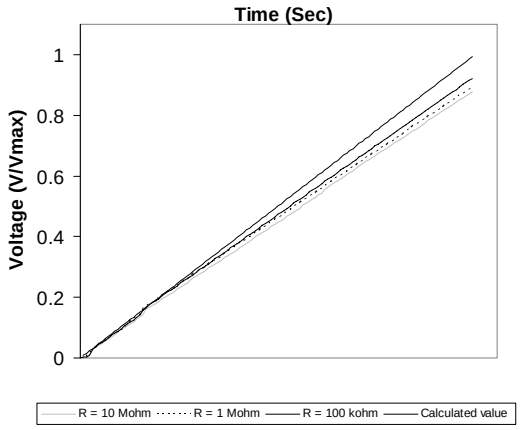

Fig. 11. The output voltage of fractional source

Fig. 11 shows the normalized output voltage when the noise gain of the circuit is controlled to be approximately 1. When the comparison the output voltages of the fractional circuit has been done with each R value, the output voltage is quite closed to the calculated value while R of the circuit is 100 kΩ as shown in table 2. The output noise voltage is smallest when it is compared between each R of circuit at RC = 1.

V. Conclusion

This paper presents the noise reduction of output voltage of the fractional source. Generally, the thermal noise can be reduced by minimizing the resistor value, the temperature and the frequency bandwidth. For this case, the fractional source is the integrated circuit which is operated under the fixed temperature condition.

According to the analysis and results of this circuit, it has been found that the noise of circuit affects to the output voltage source, which can be improved. Moreover, the noise of circuit can be reduced by decreasing the R value in circuit when the noise gain is controlled to be 1 because the noise gain affects the output voltage noise and limits the bandwidth for controlling the noise of circuit. This circuit analysis can be applied in future work to other electronic designs in order to minimize the noise in system.

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