

# FPGA Implementation of Modified Secured Web Server

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**Abstract-- Demand for High speed portable networks impels compulsory optimization in various aspects. A common web server is to act as a central control point which responds to the user request, and employing a high sophisticated computer for this purpose is not obligatory. This Paper focuses on a portable low power automated web server in a FPGA platform by accomplish the Network on chip concept. This web server has the capability to adapt multipurpose operation, a client can share the web content not only the HTML files but also can control a device operated in a remote place through this web server. In accession a modified Elliptic curve cryptographic architecture is implemented to fortify the communication of server to client system. The ECC is coalition with Montgomery multiplication for certain advantage like minimum register usage.**

**Keyword - Montgomery Multiplication, Reconfigurable, Elliptic Curve Cryptography**

## I. INTRODUCTION

The hackneyed purpose of the web server is to share the suitable complete information among the users in secured manner. The secured information sharing is corroborating with the use of Elliptic curve cryptography (ECC)[9]. The ECC is chosen because the high security obtained with less key length.

The FPGA web server is endowed in secured manner using ECC and embrace Montgomery arithmetic method in ECC to reduce the no of logical elements, worse case time and power consumption.

The HTML web pages are collected in external Static Dynamic (SD) card in encrypted format using ECC security method. A web browser interface will be developed either .NET or JAVA script. An Ethernet interface will be developed using VHDL language for the interaction of Altera NIOS II trainer FPGA kit and client computer. The clients may be increased by implementing a proper router design. The router actually works on shortest path implementation and finding a correct end client. Web browser designs entangle suitable login name and password. If password is authentic the elliptic curve cryptography will decrypt the HTML pages and approbation the display in viewable form. The HTML pages are formed with link for reference with other related documents by using a HTML language. Bus arbiter, buffer, Elliptic curve cryptography and Ethernet module are created using VHDL language. A system on chip builder (SOPC builder) is used to create the Ethernet controller, bus arbiter and NIOS CPU instruction etc variable clock frequency generator will be supplied using PLL module using IP mega core.

The active modules are as follows

- Buffer
- Memory
- Key generation
- Encryption
- Decryption
- Montgomery multiplication

Buffer is used as a cache for speed matching between transmitter and receiver. If the intermediate storage is not there suppose the data coming from transmitter is ready but at all the case the receiver may not be available. So at that time the probability of data loss is high. The Memory is used to store data pages, software program and instruction set. The SRAM cell is designed. It is set in different options. One option is as inactive. Other is getting the data and another one is loading a data. The key generation, encryption and decryption in ECC are entangling for secured communication of web pages and the third person should not embezzle information. The most important in ECC security method is key pair generation which actually invigorates the security.

The Montgomery multiplication is utilized in ECC for modular multiplication that makes the exponent multiplication operations into simple one, thereby reducing the huge register usage. It is especially advantage

when exponent and the modulus number are too high. It may not be very advantages if the exponent number is too small. The main part of the Montgomery multiplication is it uses limited no of registers. If the register size is reduced that entice reduction in area and power consumption.

## II. DESCRIPTION

### A. Block Diagram

The FPGA inbuilt with NIOS II processor act as a web server for serving the information to web users [1]. The information is stored using SD card in the HTML format. The information is encrypted using Encryption formulas followed in ECC.

### B. System Client

A client is nothing but a computer which needs service from server in form of displaying the particular related all information. A request is raised from client side by entering a keyword of the information need to be displayed.

### C. Central HUB

The purpose of the central HUB is used to serve for more than one client shown in Fig.1

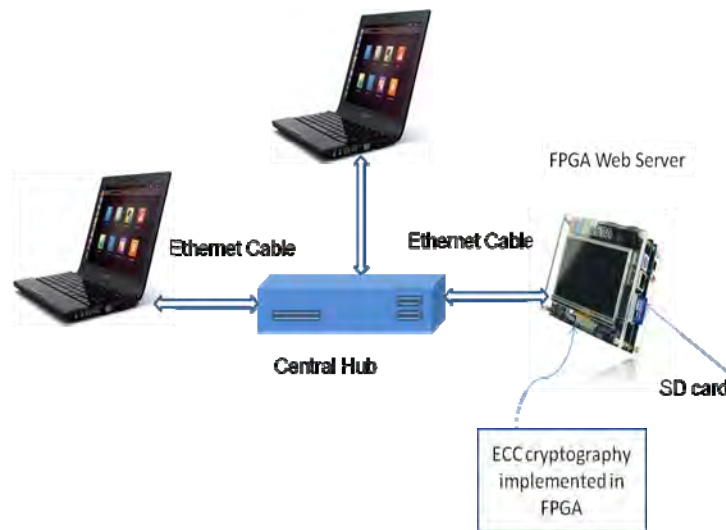


Fig. 1: General Diagram

## III. SYSTEM DESIGN

This design example shows a HTTP server using the sockets interface of the NicheStack™ TCP/IP Stack Nios II Edition on MicroC/OS-II to serve web content from the DE2-115 board[2,3,4]. The server can process basic requests to serve HTML, JPEG, GIF, PNG, JS, CSS, SWF, ICO files from the Altera read-only .zip file system.

The following describes the related SOPC system. The SOPC system used in this demo contains Nios II processor, On-Chip memory, JTAG UART, timer, Triple-Speed Ethernet, Scatter-Gather DMA controller and other peripherals etc. In the configuration page of the Altera Triple-Speed Ethernet Controller, users can either set the MAC interface as MII or RGMII.

Once the Triple-Speed Ethernet IP configuration has been set and necessary hardware connections have been made as shown in Fig. 2, FPGA web server is implemented using ALTERA NIOS II board.

Use	Connections	Module Name	Description	Clock	Base	End	Tags	IRQ
✓	[Connections diagram]	usb	ISP1362_IF					
		hc	Avalon Memory Mapped Slave	altpll_sys	0x134424d8	0x134424df		5
		dc	Avalon Memory Mapped Slave	altpll_sys	0x134424e0	0x134424e7		6
✓	[Connections diagram]	sdram	SDRAM Controller					
		s1	Avalon Memory Mapped Slave	altpll_sys	0x08000000	0x0fffffff		
✓	[Connections diagram]	tse_mac	Triple-Speed Ethernet					
		transmit	Avalon Streaming Sink	altpll_sys				
		receive	Avalon Streaming Source	altpll_sys				
		control_port	Avalon Memory Mapped Slave	altpll_sys	0x13442000	0x134423ff		
✓	[Connections diagram]	sgdma_tx	Scatter-Gather DMA Controller					
		csr	Avalon Memory Mapped Slave	altpll_sys	0x13442400	0x1344243f		7
		descriptor_read	Avalon Memory Mapped Master					
		descriptor_write	Avalon Memory Mapped Master					
		m_read	Avalon Memory Mapped Master					
		out	Avalon Streaming Source					
✓	[Connections diagram]	sgdma_rx	Scatter-Gather DMA Controller					
		csr	Avalon Memory Mapped Slave	altpll_sys	0x13442440	0x1344247f		8
		descriptor_read	Avalon Memory Mapped Master					
		descriptor_write	Avalon Memory Mapped Master					
		m_write	Avalon Memory Mapped Master					
✓	[Connections diagram]	descriptor_me...	On-Chip Memory (RAM or ROM)					
		s1	Avalon Memory Mapped Slave	altpll_sys	0x13440000	0x13440fff		

Fig . 2: SOPC builder connections

A. NIOS processor

A Nios II processor [15] includes a processor, some peripherals and memory on a single chip as shown in Fig. 3. A Nios II processor system has its own instruction set and programming model.

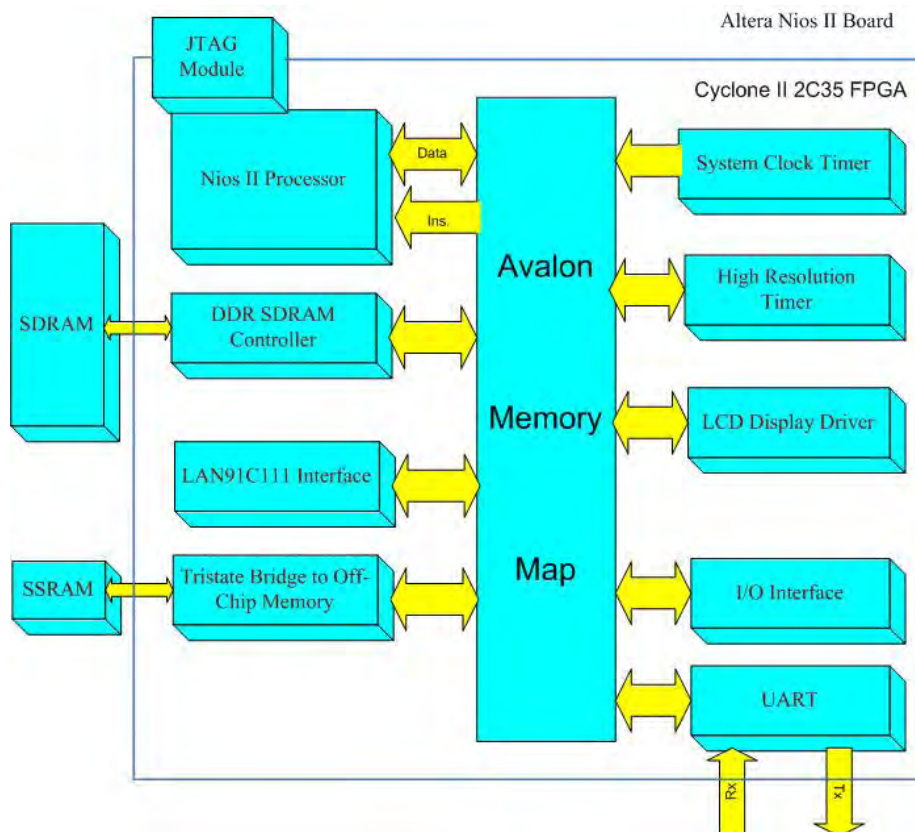


Fig. 3: ALTERA Nios II Board

B. ECC Cryptography

The ECC cryptography is the most secured method that is achieved with less key size [9, 13].

The encryption formula:

$$\text{Cipher text} = \text{message data}^{\text{public key}} \text{ mod } N$$

The decryption formula:

$$\text{Message data} = \text{cipher text}^{\text{private key}} \text{ mod } N$$

The public and private keys are formed based on certain rules mentioned in ECC.

*SD card:*

The SD card is storage unit of non-volatile type. It is available in different physical size. The information is secured by setting a password in card.

*C. HTML page*

The data is available in HTML format, which propagate from one link to another link.

IV. PROPOSED METHOD

*A. Montgomery Arithmetic*

Several modular multiplications are involved in ECC. The encryption formula is  $y=b^a \text{ mod } m$

The multiplication come modular operation is done at each single level and the immediate results are stored in temporary registers and the same steps are repeated till the exponent or index value exceeds [10, 14]. For example consider a number 2 with exponent value 5 and the final result is stored in the output register y.

E.g.  $2^5 \text{ mod } 3$

$A = (2 \times 2) \text{ mod } 3$

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output  $Y = A \text{ mod } n$  the simulation output of implementing Montgomery multiplication for the example is obtained as below. By viewing the simulation output as in Fig. 4, flow summary as in Fig. 5, power analyzer as in Fig. 6 and timing analyzer as in Fig. 7 using Quartus II software. The parameters like area, power and time have been improved.

*B. Output*

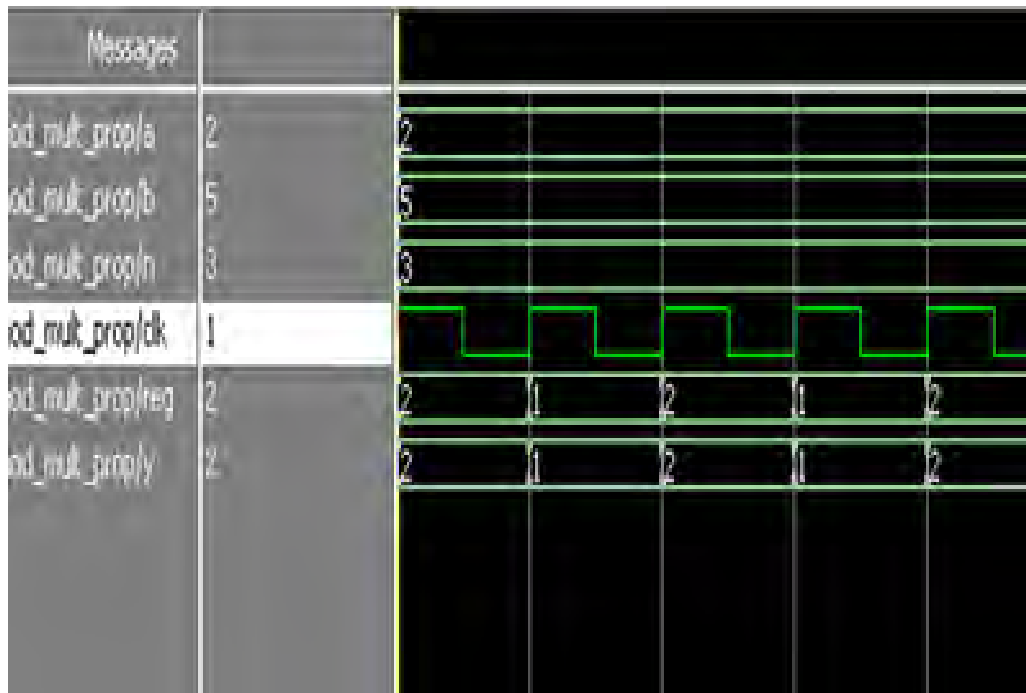


Fig. 4 :Output

Flow summary:

Flow Status	Successful - Thu Jan 03 17:44:52 2013
Quartus II Version	10.0 Build 218 06/27/2010 53 Web Edition
Revision Name	mod_mult_prop
Top-level Entity Name	mod_mult_prop
Family	Cyclone II
Met timing requirements	Yes
Total logic elements	513 / 4,508 (11%)
Total combinational functions	513 / 4,508 (11%)
Dedicated logic registers	30 / 4,508 (0.7%)
Total registers	30
Total pins	51 / 89 (.57%)
Total virtual pins	0
Total memory bits	0 / 119,808 (0%)
Embedded Multiplexer (Mux) elements	2 / 36 (.6%)
Total PLLs	0 / 3 (0%)
Device	EP2C5T14K6
Timing Mode	Final

Fig. 5: Flow summary

Power analyzer result:

<b>PowerPlay Power Analyzer Summary</b>	
PowerPlay Power Analyzer Status	Successful - Thu Jan 03 17:44:52 2013
Quartus II Version	10.0 Build 218 06/27/2010 53 Web Edition
Revision Name	mod_mult_prop
Top-level Entity Name	mod_mult_prop
Family	Cyclone II
Device	EP2C5T14K6
Power Models	Final
Total Thermal Power Dissipation	<b>35.11mW</b>
Core Dynamic Thermal Power Dissipation	0.00 mW
Core Static Thermal Power Dissipation	19.02 mW
I/O Thermal Power Dissipation	17.09 mW
Power Estimation Confidence	Low: user provided insufficient toggle-rate data

Fig. 6: Power Analyzer result

Timing analyzer result:

<b>Timing Analyzer Summary</b>									
Type	Slack	Required Time	Actual Time	From	To	From Clock	To Clock	Failed Paths	
1 Worst-case tsu	N/A	None	62.954 ns	a[2]	tmp[2]	-	ck	0	
2 Worst-case tco	N/A	None	7.286 ns	tmp[5]	reg[5]	ck	-	0	
3 Worst-case th	N/A	None	-1.150 ns	r[8]	tmp[8]	-	ck	0	
4 Clock Setup: ck	N/A	None	16.60 MHz (period = 60.234 ns)	tmp[3]	tmp[3]	ck	ck	0	
5 Total number of failed paths								0	

Fig.7 Timing analyzer result

The comparison table reveals that Montgomery Multiplication is efficient.

TABLE I

Comparison parameters	Existing method	Proposed method
Total logic elements	1523/4608(33%)	513/4608 (11%)
Total combinational functions	1523/4608(33%)	513/4608 (11%)
Dedicated logic registers	64/4608 (1%)	20/4608 (<1%)
Maximum time utilized	150.692ns	62.954ns
Total thermal power dissipation	37.70mw	35.11mw
Total pins	73/158 (46%)	51/89 (57%)

## V. SYSTEM IMPLEMENTATION

The FPGA web server is designed with the Quartus II software tool which has a SOPC builder. The SOPC builder software is used to create a chip with custom application.

The steps involved in creating a custom chip are

- Create a new project.
- Click Tools menu in that select SOPC builder.
- Select the Avalon component which is needed for the application.
- Run the program
- The message is displayed as “system generation was successful”. It indicates that the program was successfully created.

### A. FPGA web server

The Ethernet controller and TCP/IP protocol are generated with the help of SOPC builder [11, 12]. The ECC cryptography with Montgomery multiplication is integrated with SOPC generated program. The final program is downloaded in the ALTERA kit to design the web server. The results are shown below.

Comparison Table II explains between existing and proposed of FPGA web server obtained using tool Quartus II

TABLE II

Comparison parameters	Existing method	Proposed Method
Total logic elements	12,703	11,220
Total combinational functions	10,118	8,861
Dedicated logic registers	8,296	7,498
Total thermal power dissipation	1093.40mw	1005.55mw
Total pins	487	487

### B. Web server Automation

The file sharing concept of web server can be enhanced with system controlled automation of remote devices. DE2 FPGA web server can be designed to work in dual mode for html file sharing and also for device controlling as shown in Fig.8. An Ethernet cable connected with the FPGA server used to initiate TCP/IP Protocol and a dedicated USB Blaster cable is used as a control interface to control the SERVER connected device[5,6,7]. The tool control module of WEB server is shown in figure 8.

A GUI Interface is developed for user interaction with button controls; the controlling module is designed to process the kit level components like LED, SEVEN SEGMENT and VGA Devices [8].

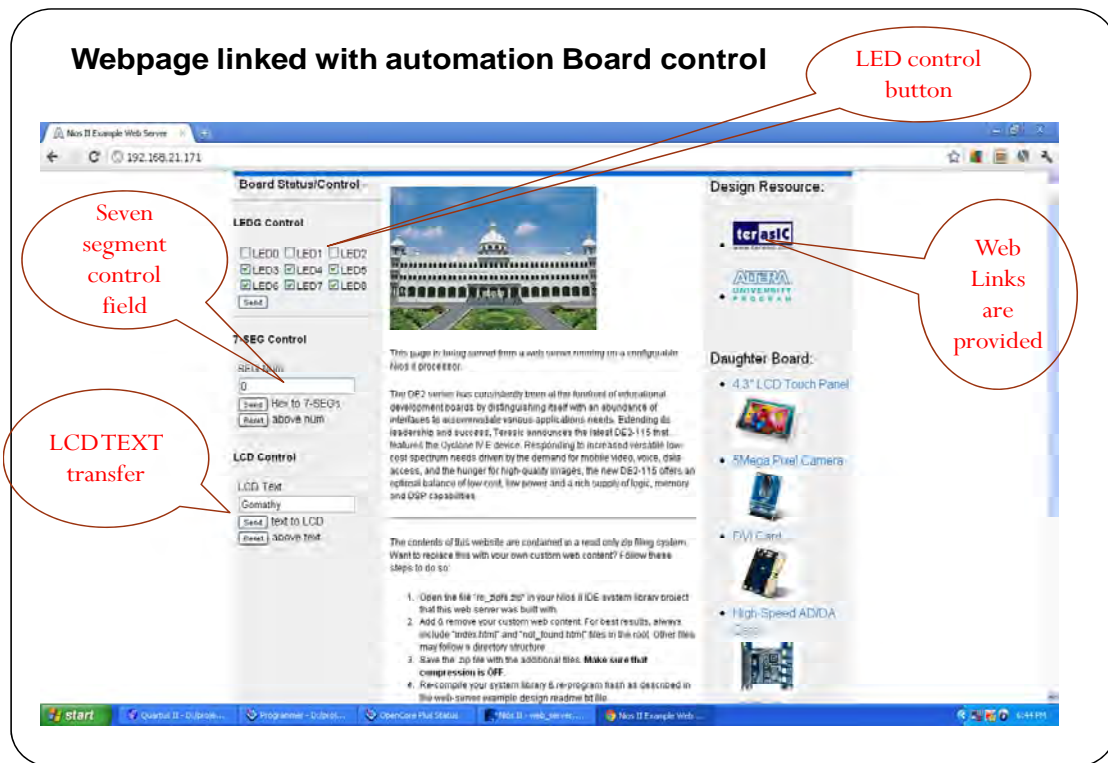


Fig. 8 :Webserver output screen

## VI. CONCLUSION

The NOC design of secured web server is successfully designed and implemented using ALTERA CYCLONE IV DE2 FPGA Board. The HTML files with JPEG, bmp images can be served through triple speed reconfigurable Ethernet port between FPGA server and client. The performance comparison existing elliptic cryptography with the modified ECC is tabulated by means of Power, delay time and area. The web server is designed with FPGA inbuilt with Nios II processor allows more flexibility in usage of different peripherals, interfaces and controllers thereby it is apparent to install in different application. The hardware design board of DE2 FPGA is configured using high level VHDL Language with low power elliptic curve cryptography. User authentication logic is developed in C++ language to encrypt and decrypt the HTML contents.

The web server logic for HTML file sharing and device control module is merged into a single entity, from which a client user can select any mode as per requirement.

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