Low Power Detection Architecture for MIMO Systems

Shirly Edward.A[#1],Malarvizhi.S[2],Anjana.R[#3],Aishwarya.R[#4]
[#]Department of ECE,SRM University,Vadapalani,Chennai,India.
[1]edward.s@vdp.srmuniv.ac.in
[3]anjana1101@gmail.com
[4]aishwarya.rajagopalan@yahoo.co.in
[2]Department of ECE,SRM University,Kattankulathur,Kancheepuram Dt.India.
[2] malarvizhi.g@ktr.srmuniv.ac.in

***Abstract*— This paper presents an architecture for K-best List Sphere Decoder (LSD) algorithm for Multiple Input Multiple Output (MIMO) Systems using Xilinx System Generator. We made use of an efficient bit-serial architecture, Distributed Arithmetic(DA) to reduce the computational complexity involved in the algorithm. The real-valued expanded channel matrix and received vectors are analyzed, designed and implemented using Xilinx Spartan-6 FPGA running at 100MHz. We compare the resource utilization of the conventional implementation of the algorithm with the proposed architecture for different number of layers. The conversion of multipliers into shift and adder units leads to area optimization and reduced power consumption. The total estimated power for our design is found to be 187mW**.

Keyword- MIMO,K-best LSD, Distributed Arithmetic, Xilinx System Generator.

I. INTRODUCTION

Multiple-Input Multiple-Output(MIMO) systems provides high data throughput by using multiple transmit and receive antennas all working at the same frequency without additional bandwidth and transmit power[1].MIMO techniques are included into several emerging wireless communication standards like 3rd generation partnership project (3GPP) long term evolution(LTE),IEEE 802.16e WiMAX broadband mobile standard and IEEE 802.11n wireless LAN. The increasing data rates and higher capacity requirements need improved detector implementation and architectural design. The main challenge in the practical implementation of MIMO systems lies in the efficient design of the detector which needs to separate the spatially multiplexed data streams.

The MIMO detection can be considered as integer least squares problem, the optimal solution for which is got by Maximum Likelihood(ML) detector[2].The ML detection requires an exhaustive search hence it is computationally very complex and not feasible as the possible points increases. QR decomposition will reduce the complexity of ML by the process of tree search and pruning. Depth-first, breadth-first (K-best) and Fixed complexity sphere decoder algorithms are available for pruning the tree. Hard output Depth-first SD algorithm was first implemented by Burg in [3] and Guo in [4] implemented the soft-output K-best decoder. In [5], the parallel merge algorithm was proposed to increase the throughput of the conventional K-best architectures.

The hard output SDs are modified to get soft reliability information of the transmitted bits as an output. The List Sphere Decoder (LSD) is a variant of SD, it applies the tree search algorithm and obtains a list of candidate symbol vectors, which is used to calculate the soft outputs. Hochwald and ten Brink[6] proposed the list sphere decoder. These algorithms are modified to continue the tree search to get a defined list of candidate symbol vectors and compute the Partial Euclidean Distance (PED). LSD is used to approximate the Maximum aposteriori (MAP) detection. The K-best LSD has the advantage of constant throughput.

In CMOS design circuits, the switching or dynamic power equation[8] is given by

$$P = kC_L V^2 f$$

Where k represents the switching activity factor, C_L the total capacitance, V the supply voltage and f the frequency of operation. Algorithmic power optimization reduces both physical capacitance and the switching activity factor. Physical capacitance can be reduced through efficient hardware implementation. Switching activity reduction can be achieved by reducing the switching frequency of nodes. Therefore, the design with reduced hardware complexity saves power.

In this paper, we show how the hardware complexity of K-best LSD reduces with the application of Distributed Arithmetic(DA), a bit serial architecture. Our design makes use of ROM ,Shifter and adder unit instead of multiplication in the PED calculation. The real valued and the complex valued signal are given as input to the proposed design and simulation results were verified.

The organization of the paper is as follows: Section 2 gives a brief introduction to MIMO system model, Maximum Likelihood detection and the sphere decoder. Section 3 summarizes the List Sphere Decoder and the K-best List Sphere Decoder algorithm. Section 4 describes the proposed architecture and its implementation. Section 5 presents the resource utilization and power estimation reports using Xilinx FPGA. Section 6 concludes the paper.

II. MIMO System Description

Consider a MIMO system with M transmit and N receive antennas, the received signal is given by the following relation,

$$y = Hs + n \tag{1}$$

where H is the M x N dimensional channel matrix, s is the M array transmitted signal with each element from a complex constellation ***o*** and n is an N dimensional i.i.d. Gaussian noise vector. We assume that the channel matrix is perfectly known at the receiver through channel estimation techniques. The mathematically optimal solution to find vector s from received vector y is called the Maximum Likelihood (ML) :

$$\hat{s} = \arg\min \| \hat{y} - Hs \|^2 \tag{2}$$
$$s \in o^M$$

ML is an exhaustive search over o^M possible constellations . The ML search space is over 2^{MQ} candidates which is dependent to the number of the constellation points *Q* and transmit antennas *M.* Among the various MIMO detection algorithms like zero-forcing, MMSE, V-BLAST, sphere decoders (SDs), the latter attracted more interest because of their lower complexity and near ML performance. As stated earlier, ML is the best mathematically optimal solution for MIMO detection. But the implementation of this algorithm is costly and impractical. Sphere decoders will reduce the complexity of ML by changing the problem to a tree search and pruning process. The sphere decoding is done after QR decomposition of the channel matrix.

Consider matrix H=QR , in which R is an upper triangular matrix and Q is a unitary matrix. Multiplying both sides of (1) by Q^H will result to:

$$\hat{y} = Rs + Q^H n \tag{3}$$

Where $\hat{y} = Q^H y$ **.** Solving the Equation (3), will lead to the solution:

$$\hat{s} = \arg\min P(s) \tag{4}$$

Where $P(s) = \left\| \hat{y} - Rs \right\|^2$. P(s) can be taken as a recursive sum of partial Euclidean Distances(PED).

III. List Sphere Decoder

A list sphere decoder outputs a list of the most likely symbol vectors and their Euclidean Distances. The trade off between performance and computational complexity depends on the list size. There are different types of search based algorithms for LSD ,namely breadth-first search (K-best LSD)[7], depth-first search(Schnorr-Euchner Enumeration(SEE)LSD)[7],metric-first search(Increasing Radius(IR) LSD)[7].In our paper, we consider K-best LSD algorithm for architectural implementation.

A. *K-best LSD Algorithm*

K-best LSD is a breadth-first search algorithm that considers all the candidate symbol vectors in parallel and computes the partial Euclidean distances (PEDs) at each level. K-best LSD[11] is preferred over other algorithms as it provides fixed throughput and reduced complexity. In this process, K best symbols with smallest Euclidean distance are chosen and stored.

The algorithm can be summarized as follows:

1) Initialize P_M=0 (here we take the number of antennas at transmitter and receiver as M=4, so we have taken P_4=0).
2) Initialize K=M-1, and calculate Partial Euclidean distances for all symbols admissible at level K:

$$P_k = P_{k+1} + \| y_k - \sum_{i=k}^{M-1} R_{k,i} s_i \|^2$$

3) Back substitute and choose K-best symbol vectors with smallest PEDs till K=0 and then terminate the process; else take K=K-1 and perform step (2).
4) Save these symbols and their corresponding PEDs.

IV. PROPOSED ARCHITECTURE FOR K-BEST LSD

In the hardware implementation of K-best LSD algorithm , the architecture computes the Partial Euclidean distance for K data paths in parallel. The multipliers required to implement the architecture makes it expensive in terms of hardware resources and power consumption.

We propose an architecture in Fig.1 for K-best LSD algorithm using Distributed Arithmetic a bit serial architecture. It consists of the preprocessing unit, ROM unit, shift and adder unit, Euclidean norm calculation unit and the PED unit . The real valued channel matrix is fed as input to the preprocessing unit . Here, we obtain the value of Q(unitary matrix) and R (the upper triangular matrix) after QR decomposition . With an apriori knowledge of the upper triangular matrix R the content of the ROM unit are initialized. Depending upon the layer information and input symbol vector, the content of the ROM is retrieved and fed to shift and add unit .

The Distributed Arithmetic unit in our architecture comprises of ROM unit and shift and adder unit. This unit replaces the multiply-accumulate term in the Partial Euclidean Distance Equation. The output of DA unit is fed to the norm calculation unit, for which the estimate of y is given as another input. The estimate of y is got by combining Q^H with y. Finally, the partial Euclidean Distance(PED) is calculated.

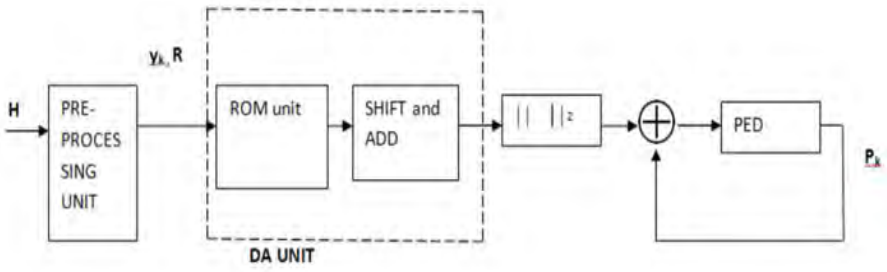

Fig.1 Proposed K-best LSD

A. Implementation

Xilinx System Generator enables high-level modelling and provides wide range of options for implementing signal processing systems. Simulink in MATLAB environment, includes Xilinx System Generator blockset [10] which is a powerful tool for hardware/software co-design.System Generator provides access to shift register logic, distributed and block memory and embedded multipliers. The Xilinx blockset maps the Intellectual Property(IP) cores with high level blocks for efficient implementation in the target Xilinx FPGA. The Xilinx System Generator is used to implement and verify the proposed architecture on the Spartan6-xc6slx25t FPGA.

We had considered a 4×4 MIMO system with 4-QAM modulation for our design. The channel information is assumed to be perfectly known at the receiver. The Rayleigh channel matrix is taken into consideration. We applied Real Value Decomposition(RVD) to the estimated complex channel matrix H to convert all the complex values into real values. This reduces the complexity of the LSD. The real valued matrix is given as input to the preprocessing unit where QR decomposition is performed. Both the real valued and complex valued signal models for K-best List Sphere Decoder are implemented and the results were verified. Fig.2 shows the Xilinx system generator implementation of a single Distributed Arithmetic unit. This DA unit computes multiply-accumulate operation in one clock cycle. The ROM stores the layer information and the upper triangular matrix values which can be retrieved depending upon the input. The Block RAM memory type is opted for our design. For the layer value k = 4, the ROM depth is chosen to be 64.The shift and adder operation is carried out in sequence. Four DA units are combined in parallel, to obtain the Partial Euclidean Distances for k=4. We have also implemented the conventional method[9] for finding the partial Euclidean distances for K-best LSD using Xilinx System Generator.

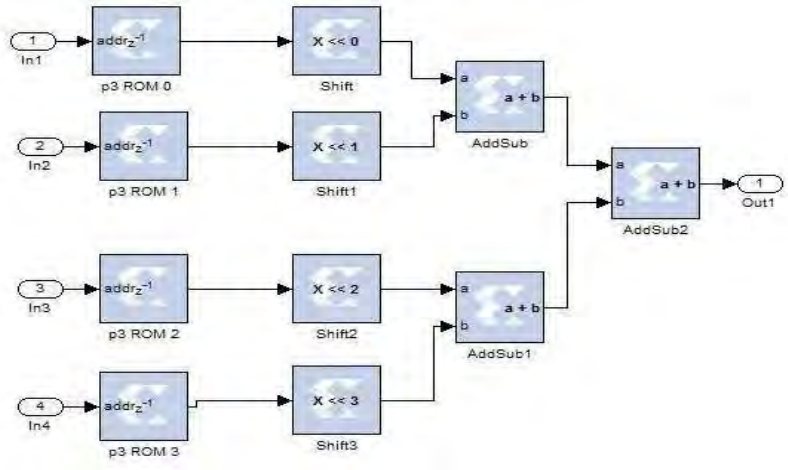

Fig. 2 Distributed Arithmetic unit

V. RESULTS AND DISCUSSION

The results of conventional method and proposed design were verified. The hardware resources were estimated for each module and compared. The comparison is presented in Table.I.It can be clearly inferred from the table that there has been a significant reduction in the resource utilization in the proposed model compared to the conventional method. The results show 50% reduction in slices,55% reduction in LUT usage and 80% decrease in the multipliers used. The power estimation is done by Xilinx Xpower Analyzer using System Generator. From the results listed in Table.II it is clear that our proposed design consumes less power compared to the conventional method.

TABLE I
FPGA Resource utilization summary

Resources	**Conventional method for k=4**	**Proposed for k=2**	**Proposed for k=4**	**Proposed for k=8**
Slices	380	72	190	480
BRAMs	0	8	16	32
LUTs	623	127	280	726
Mults/DSP48s	20	2	4	8

TABLE II
Timing and Power results

Parameters	**Conventional method for k=4**	**Proposed for k=4**
Estimated Power	298mW	187mW
Maximum Frequency	214.961MHz	77.7MHz

VI. CONCLUSION

The proposed architecture for K-best list sphere decoder for different number of layers were implemented and the resources utilized were compared. The implementation of proposed design requires only a small number of ROM-LUTs which leads to a negligible increase in circuit complexity. The parallel calculation of partial Euclidean distances would increase the throughput and decrease the latency. Hardware complexity in the

conventional method is greatly reduced with our design. Our future work will be to design and develop receiver algorithms for MIMO-OFDM system with the bit serial architecture for emerging wireless communication standards.

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