Newly-Constructed Single Phase Multilevel Inverter for Distributed Energy Resources

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***Abstract*— Distributed energy resources systems are small power generation tools used to afford substitute solution or added enrichment of traditional electric power system. This paper is mainly concentrated on 1Ø multi-level inverter for Distributed Energy Resources. The objective of this paper is to reduce switches with increase in multi-level outputs which inherently reduces the cost & harmonics. Seven-level inverter with 6 switches and thirteen-level inverter with 8 switches are carried out using MATLAB 7.10 version (Simulink). Total Harmonic Distortion (THD) is analysed for two types of multi-level inverter in MATLAB. For implementing hardware, the circuit is tested in PROTEUS 7.4 version software which helps in troubleshooting real time problem.**

***Keywords* – Multi-level inverter, Distributed Energy Resources (DER), Renewable energy, solar energy, Wind generator.**

I. INTRODUCTION

In considering the global warming and change in climate it is important to focus on emission of greenhouse gases and there reduction. The main cause of global warming is due to burning of fossil fuels for producing electricity so now everyone focusing on renewable resources. It is difficult to replace all non-renewable electricity plants into renewable one mainly considering in cost point of view. But one can reduce thermal power plant emission by adopting DER. By DER typically about 3kW – 10000kW range is possible either it can be used as an alternative or synchronized with traditional power lines depends on utility usage. To use DER's in electrical power system we need an inverter. In case of micro grid system 1Ø multilevel inverter is usually adopted. Various research works are going on over inverter circuit configuration mainly in reducing the switches at higher voltage level. In such arrangements, utmost Distributed Energy Resources regularly supply a DC voltage that differs in a wide range according to different load conditions. Further by reducing switches & increasing level will reduce filter cost & harmonic content. 7- Level cascaded multilevel inverter [2] topology requires 12 switches but in this new multilevel inverter it requires 6 switches in which same multilevel is obtained. Invariably switching losses and cost also reduced. In reality a high step up converter is used before inverter input circuit for maintaining high constant voltage. In this paper we are going to study only about multilevel inverter circuitry.

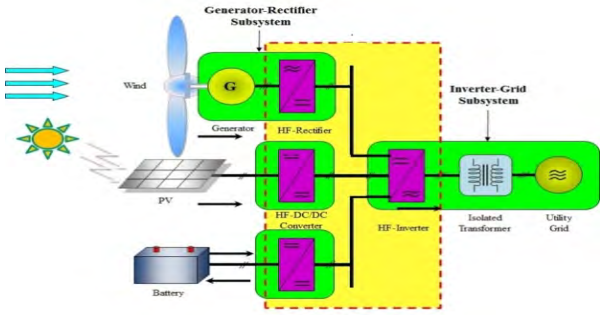

Fig.1 Structure of Multi-level inverter for different DER application.

The new multi-level inverter topology has minimum number of switching devices, improved output waveform and lower total harmonic distortion (THD). In this proposed topology 6 switches & 7-level MLI is proposed and to authenticate the effectiveness of the topology a prototype is constructed and tested.

II. PROPOSED INVERTER

DER is nothing but the interconnection of various renewable sources to the common grid, one of such

DER is shown in Fig.1. A PV cell, wind turbine & a battery which are connected to input of an inverter, here three different constant voltages is made provided for the inverter circuitry [3]. The core aim of the proposed topology is to reduce number of switches. For explaining, 7 and 13 level inverter with two and three dc voltage source of different voltages are taken respectively and this circuit configuration is developed. This 7-level inverter carries 6 switches in two legs, carrying three switches in each leg. The switches are named as MA1, MA2, MA3, MB1, MB2 and MB3.

MA1, MA2, MA3 are placed in first leg and MB1, MB2, MB3 are placed in second leg as shown in Fig.2. In cascaded multilevel inverter the switching losses are more due to higher switching frequency. In this proposed topology, 4 MOSFET working with different range of frequencies. MA1 and MB1 are operated at 50 Hz line frequency.

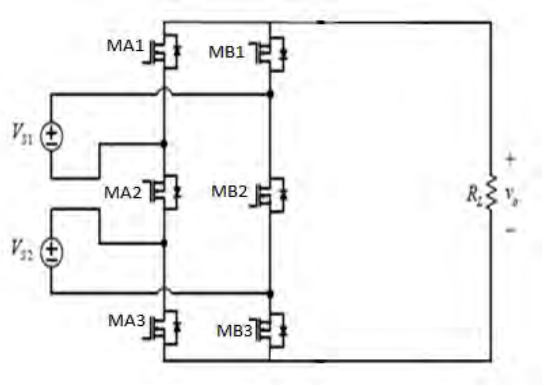

Fig.2. 7-level inverter circuit diagram

Compared with cascaded multilevel topology switching losses are reduced. Having voltage stresses in account, MA2 and MB2 have more voltage stress i.e. (V_{s1} + V_{s2}) & respective switches have respective voltage stress i.e. (V_{s1} & V_{s2}).

A. Switching Schemes with operations

Switching pattern for the proposed inverter is shown in table 1.

Modes	MA1	MA2	MA3	MB1	MB2	MB3	Voltage levels
Mode 1	-	*	-	*	-	*	(V_{s1}+V_{s2})
Mode 2	-	*	*	*	-	-	V_{s1}
Mode 3	*	*	-	-	-	*	V_{s2}
Mode 4	-	-	-	*	*	*	zero
Mode 5	-	-	*	*	*	-	-V_{s2}
Mode 6	*	-	-	-	*	*	-V_{s1}
Mode 7	*	-	*	-	*	-	-(V_{s1}+V_{s2})

Table 1: Switching Sequence for seven level inverter

'*' denotes Switches are in ON state and

'–' indicates Switches are OFF state.

Mode 1:

***For positive (V_{s1}+V_{s2}) voltage level*:** MA2, MB1 and MB3 are switched on for getting a maximum voltage i.e. addition of two source voltages.

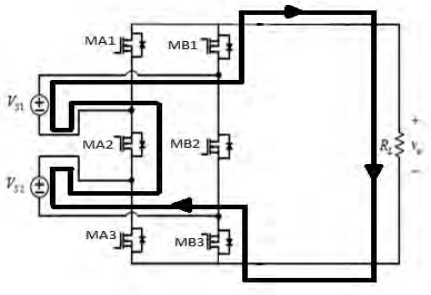

Figure.3.Switching Sequence for getting a voltage of "(Vs1+Vs2)": (MA2+MB1+MB3)

Mode 2:

For positive V_{s1} Voltage level: MA2, MA3, MB1 are switched on for getting a next higher priority level of voltage.

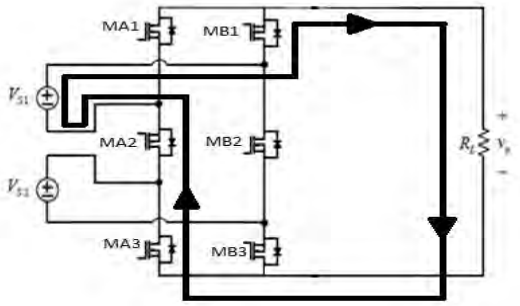

Figure.4. Switching Sequence for getting a voltage of "Vs1": (MA1+MB2+MB3)

Mode 3:

For positive V_{s2} Voltage level: MA2, MA1, MB3 are switched on for getting a lower priority level of voltage.

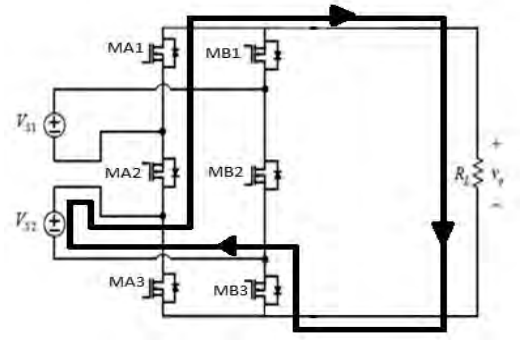

Figure.5. Switching sequence for getting a voltage of "Vs2": (MA1+MA2+MB3)

Mode 4:

For zero output voltage level: MB1, MB2, MB3 are switched on for getting zero output.

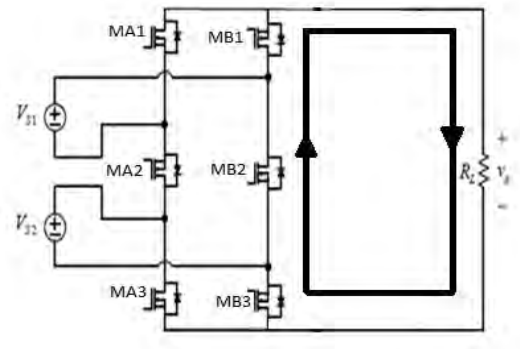

Figure.6. Switching sequence for getting a voltage of "zero": (MB1+MB2+MB3)

Mode 5:

For negative V_{s2} Voltage level: MA3, MB1, MB2 are switched on for getting a negative lower priority level of voltage.

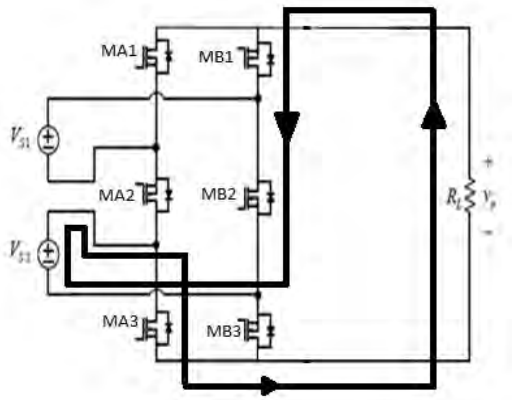

Figure.7. Switching Sequence for getting a voltage of "- (Vs2)": (MA3+MB1+MB2)

Mode 6:

For negative V_{s1} Voltage level: MA1, MB2, MB3 are switched on for getting a negative second higher priority level of voltage.

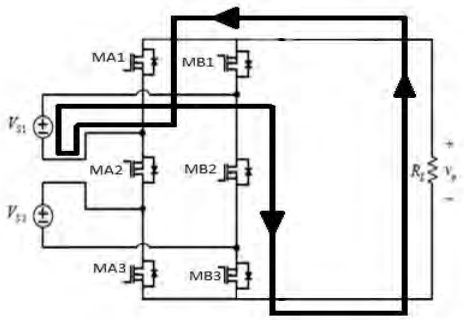

Figure.8. Switching Sequence for getting a voltage of "- (Vs1)": (MA1+MB2+MB3)

Mode 7:

***For negative (V_{s1}+V_{s2}) voltage level*:** MA1, MA3 and MB2 are switched on for getting a negative maximum voltage i.e. addition of two source voltages.

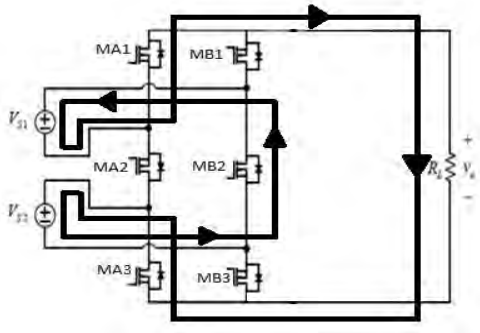

Figure.9. Switching Sequence for getting a voltage of "- (Vs1+Vs2)": (MA1+MA3+MB2)

B. Pulses for seven level proposed inverter

The pulses for seven level inverter are shown below,

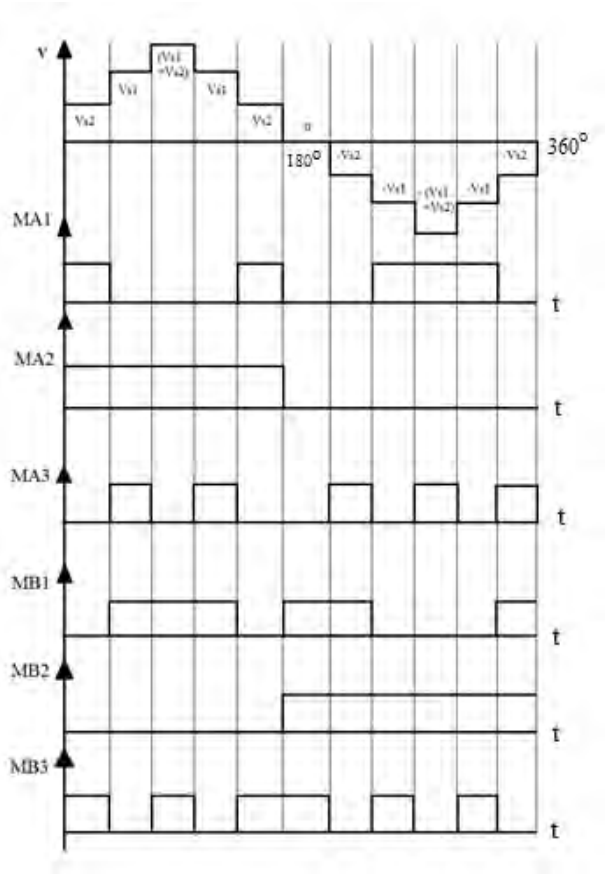

Figure.10 Triggering Pulses for Seven level inverter

At any instant any three switches are turned ON hence average power loss is low.

C. Facts of proposed inverter

The deserving point of this proposed topology is, if solar input source does not deliver power then we can run with minimum sources. To clear this above point we can go with next higher level of topology.

Thirteen level inverter

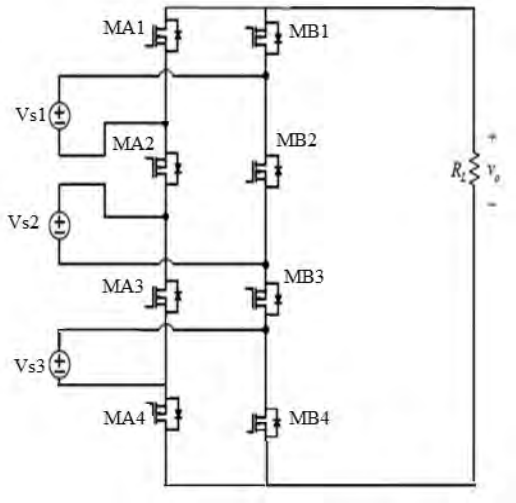

Figure.11 Thirteen level inverter circuit configuration

The above configuration results with a thirteen level inverter with following conditions which will be given in subsequence text. The main significant feature to be noted is 8 switches and 3 sources are used for bringing thirteen level output.

$$Vs2 > Vs3 > Vs1$$

By placing sources in this order we can get thirteen level output.

For example, in coastal areas solar panel will produce less voltage compare with wind, so we can place solar in first and second place should hold maximum output voltage because of this scenario we should go with wind generator and a constant battery is used as third voltage source which should be more than first source and less than second source.

Case1: If solar fails to give the required voltage then we can disconnect that source and run it as seven level inverter by closing the respective switches namely MA1 and MB1 meanwhile pulses also should be changed this can be carried out with help of microcontrollers.

Case2: If battery and wind fails then we can run it as three-level inverter, by switching on continuously the four respective switches MA1, MA2, MB1 and MB2.

Case 3: If the three source are of batteries and if they are placed as per above condition then there will not be any problem of power shortage across the load i.e. load will be independent.

When one input sources stops delivering power *we* will get output but its amplitude will be lower comparing with previous state. So our usage of load will be dependent on the source. The main drawback of this inverter is the load is source dependable.

In case 1 and 2 does not occur then our inverter will work well by giving constant power to the load with fewer harmonics. Now DER's are widely used and to install a renewable energy power system, installation cost is more. Meanwhile converter cost is also more. Reducing switches may be a suitable way of reducing the cost. This proposed topology is evidence for reduction in switches with higher multilevel output and this inherently reduces the cost. Micro-grid is not essential for this inverter which also meaningfully reduces the cost [4].

D. Simulation results

In this paper MATLAB, PROTEUS is used. Proteus is a real time software tool which is implemented before performing hardware. In MATLAB the seven level inverter circuit is simulated and results of output voltage and THD is shown

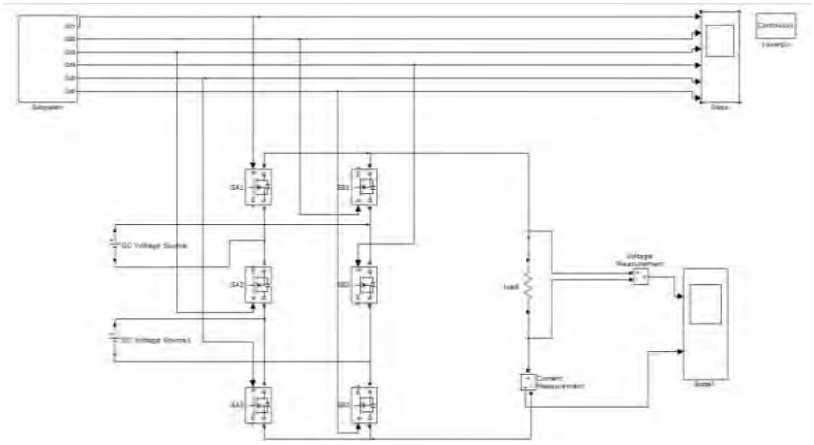

Figure.12 Seven level circuitry in MATLAB tool

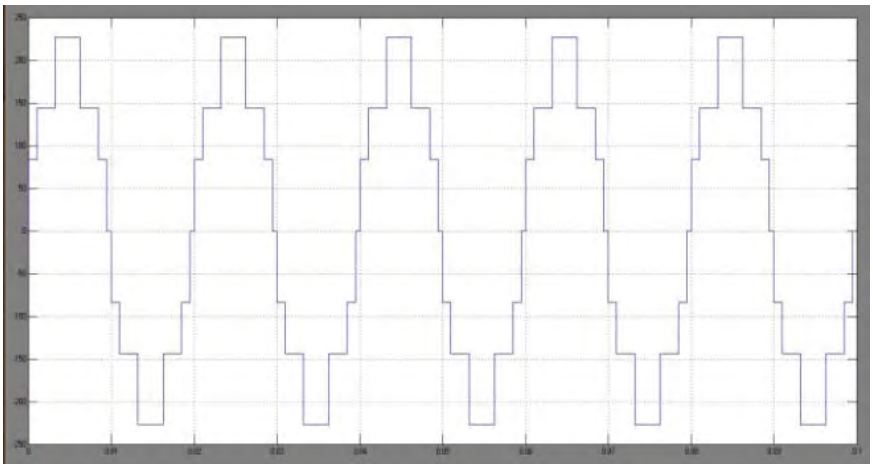

Figure.13 Seven level output using MATLAB tool

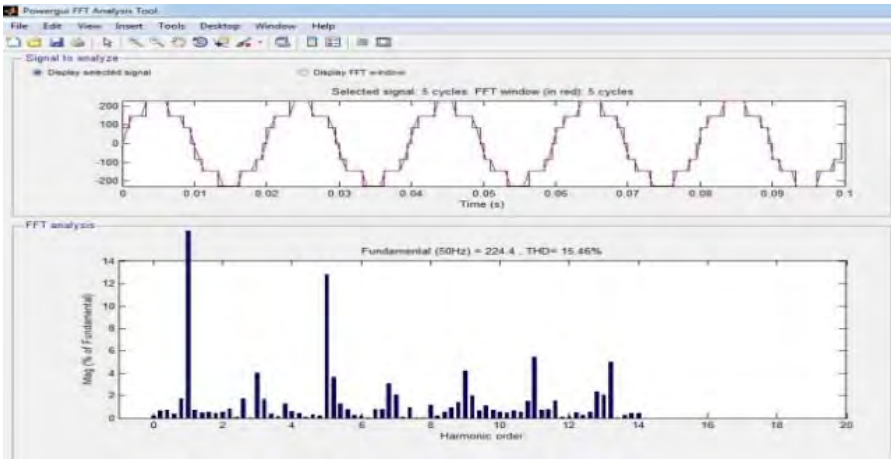

Figure.14 7 Seven level THD using MATLAB tool

The THD for seven- level inverter without using filter is 15.46% is determined using FFT analysis.

The thirteen level inverter is extended from seven level circuit configuration, there simulation output are shown below,

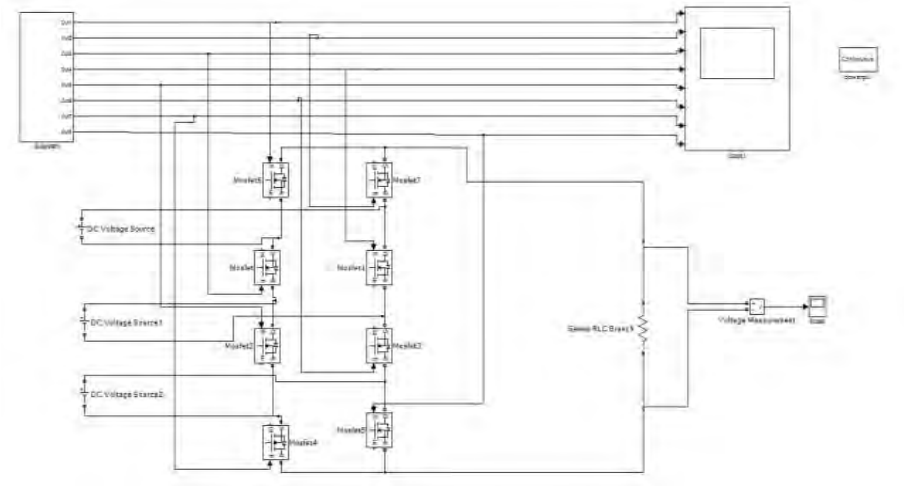

Figure.15 Thirteen level inverter circuit using MATLAB

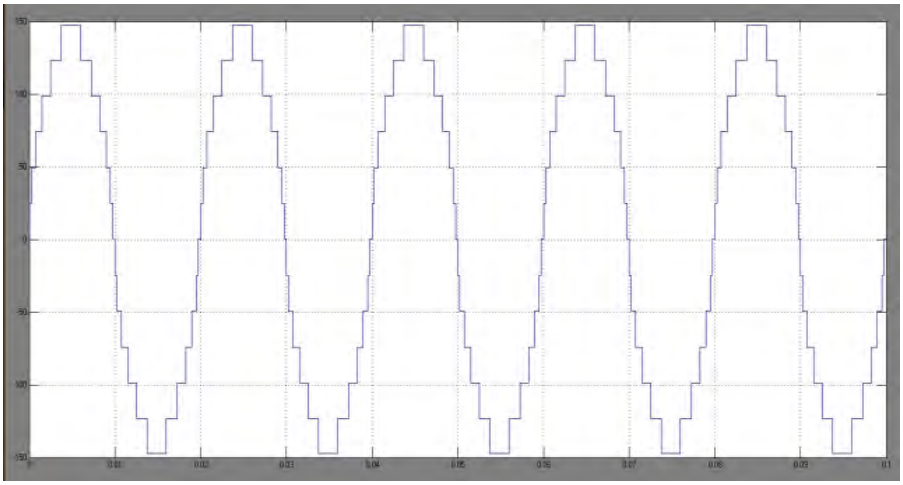

Figure.16 Thirteen level output using MATLAB tool

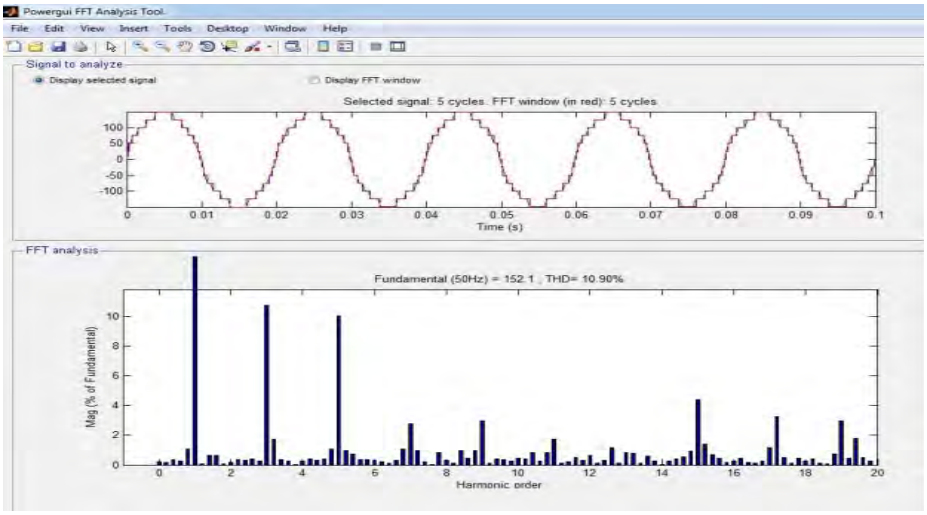

Figure.17 Thirteen level THD using MATLAB tool

The THD for thirteen level inverter without using filter is 10.90% is determined.

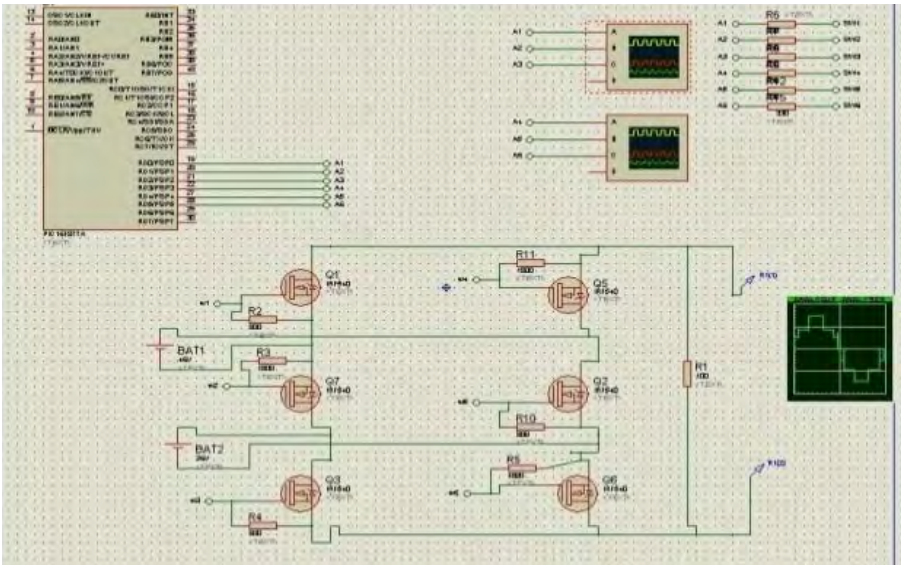

Figure.18 Seven level circuitry in Proteus Software

Figure.19 Seven level output in Proteus Software

E. Hardware implementation

The hardware is implemented for seven-level inverter, Six IRF460 – MOSFET are used in this design which has high voltage and current carrying capability. Gate Driver circuits are used for boosting the pulses which we get from a microcontroller. PIC16F877A is used for generating required pulses.

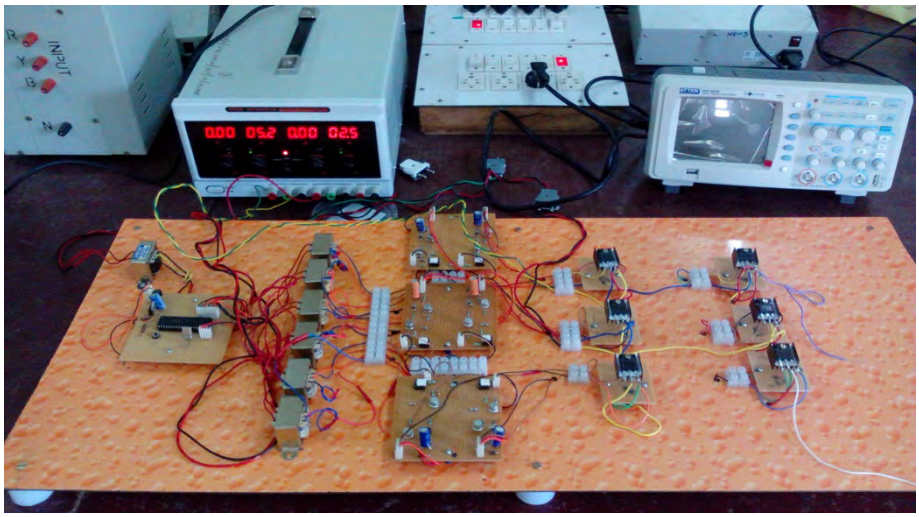

Figure.20 Hardware implementation of seven level inverter

And using Power Quality Analyzer we have calculated THD and it is given in Figure.21and Fig.22,

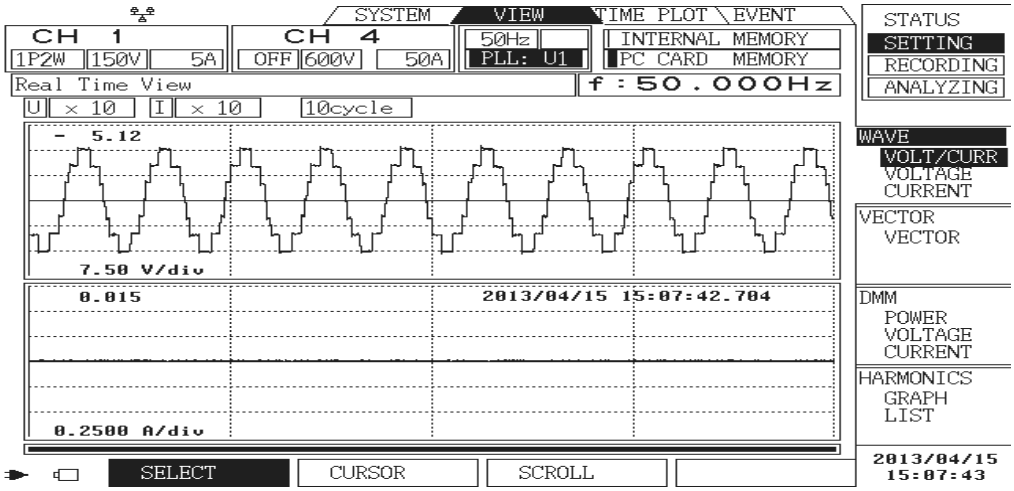

Figure.21

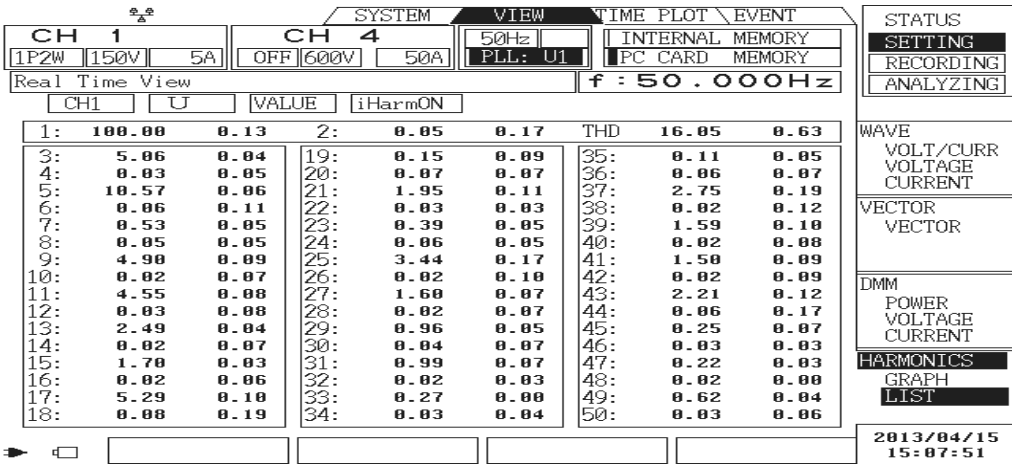

Figure.22

Tabulation:

Observation Sources	Total Harmonic Distortion (%)
Simulation Software	15.46%
Hardware	16.05%

III. CONCLUSION

This paper reports a substantial saving of switching devices used for a 1Ø multi-level inverter topology that harvests an important multi-level output for DERs. The agreement between the simulated software results and the observed output from the hardware circuit shows clearly that the new multi-level topology for DER works as expected generating desired seven level output using only 6 power switches. Total harmonic Distortion and reduction in switching are appreciable.

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