# Analysis of Current Source PWM Inverter for Different Levels with No-Insulating Switching Device

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***Abstract*—This paper gives the new set-up of inverter having DC current source (CSI) having no insulated switching device. In the proposed new CSI topology every switching device are connected across a common-source level, thus a single power supply gate drive circuit is required and no insulated power supply and the customary bootstrap circuit is applied. This CSI topology is even legitimate for utmost level of current waveform output, where the power switches number increases. As a turn up, gate drive complexity is reduced, and it also eliminates the cost of capacitors and transformers in switching devices, driver circuits. In addition, this new topology of current-source PWM inverter (CSI) can operate even at utmost switching frequency, as every switches will be connected across a common source level. In this paper the different level of proposed CSI operation principle, its design using computer simulation (MATLAB) with its total harmonic distortion (THD) is analyzed. The computer simulation using MATLAB determines the feasibility of this topology with the analysis of different level which results in reduction of its complexity and the physical size.**

**Keywords — multilevel inverter; current-source PWM inverter; common-emitter level; total harmonic distortion**

## I. INTRODUCTION

Power converter performance has vastly been improved recently after the development of the power devices such as IGBTs, IGCTs and MOSFETs which can perform even at high switching frequency for high and medium power application. The power MOSFETs based on silicon carbide (SIC) are used as its voltage rating is maximum and its switching speed is nearly ten times that of silicon (Si) found devices. In addition, the Sic-MOSFET resistance can be reduced by 1/500 times of presently used devices and the power density, efficiency of the power converter are improved as the operating temperature can exceed over 300°c.

The research interest in power converter has been increased due to the utmost development of semiconductor switches which has utmost performances. The multilevel inverter results in less distort output waveforms as compare to conventional two-level inverters. The two category of multilevel inverter are CSI and VSI. The voltage-source inverter (VSI) gives AC voltage waveform for DC voltage source. The DC current source gives AC current waveform when given to current-source inverter. The CSI has high impedance source thus gives short-circuit protection but an open-circuit protection is required for current continuity.

The circuit complexity as of driver circuit and its control needs more attention as the multilevel inverter has more number of semiconductor power switches. The dv/dt and serious EMI problems cannot be disregarded in application of utmost speed switching, mainly in high frequency noise currents in driving gate circuits. The CSI topology uses bulky inductors to have smooth DC current and the power switches are connected with discrete diodes in series are some drawbacks which reduce its efficiency. Due to the emerging of reverse-blocking IGBTs, the series diodes may not be needed in coming future.

In this paper, the CSI topology has the switches connected across a common source level, hence reducing the required gate drive circuit to a single driver circuit for all switches. This topology is still legitimate for utmost level of current waveform output, where power switches number increases. In addition, this topology also reduces the dv/dt problem as switches are across common-source level.

The performance of the CSI topology is analyzed and verified using computer simulation (MATLAB) for different level with its total harmonic distortion (THD), with the power IGBTs having diodes with blocking capabilities.

## II. WORKING AND ITS CIRCUIT SET-UP

Figure 1 gives the 2-level module of CSI with two switches connected across common-source level. The 2-level CSI is connected with 3-level current-source inverter (CSI) to have higher level current-source inverter (CSI) with power switches connected across common-emitter level to have utmost level of current waveform output. The 3-level CSI is the main inverter which is further connected with one or more number of 2-level CSI to have different level of the proposed CSI. The relation between CSI output current level number and 2-level current –source inverter (CSI) number can be given by the equation:

$$N= 3+2m \quad (i)$$

Where, N is CSI output current levels number and m is the two-level CSI number modules.

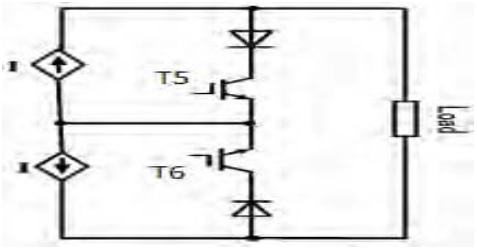



Figure1. Two-Level CSI

### *A. PRINCIPLE OF OPERATION*

#### *A1. THREE-LEVEL CSI*

Figure 2 gives the circuit set-up for three-level CSI. The switches (**T1**, **T2**, **T3** and **T4**) are linked to common-source level. Table A gives the sequence for switching of the 3-level CSI to have 3-level current waveform output. Here all the sources (DC current) is of same amplitude given as **i1= i2= i**.

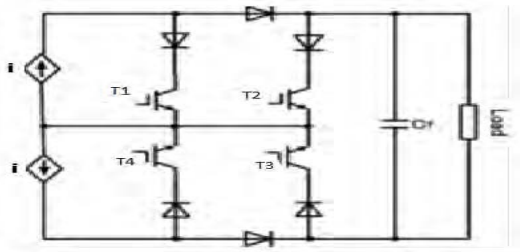



Figure2. Three (3)-Level CSI

The 3-level current output (**+i**, **0** & **–i** current-level) are obtained by:

1) **Current i: T3** is switched on to make current **i1** pass through the load. **T4** is switched on to have circulating path for the current **i2**. **T1** and **T2** are kept off.
2) **Current 0: T1** and **T4** are switched on to have circulating paths for currents **i1** & **i2**. **T2** and **T3** are kept switched off thus, no current pass through the load.
3) **Current -i: T2** is switched on to make current **i2** pass through the load, in the opposite direction. **T1** is switched on to have circulating path for current **i1**. **T3** & **T4** are kept off.

| 1 | 2 | 3 | 4 | Output |
|---|---|---|---|---|
| ! | ! | # | # | i |
| # | ! | # | ! | 0 |
| # | # | ! | ! | i |

Table A. Switching sequence of three-level CSI
! : - represents switch is OFF, #: - represents switch is ON

#### *A2. FIVE-LEVEL CSI*

Figure 3 gives the circuit set-up for 5-level CSI. The switches (**T1** to **T6**) are linked to a common-source level. Table B gives the sequence for switching of 5-level CSI to have 5-level current waveform output. Here all the sources (DC current) is of same amplitude given as **i1= i2= i3= i4= i.**

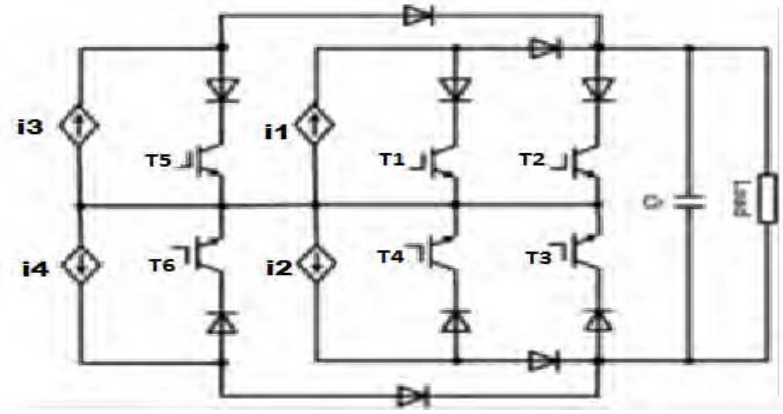



Figure3. Five (5)-Level CSI

The 5-level current output **(+2i**, +**i**, **0**, **i** & **-2i** current-level) are obtained by:

1) **Current 2i: T3** is switched on to make current **i3** and **i1** pass through the load. **T4** & **T6** are switched on to have circulating paths for the currents **i2** & **i4**. **T1**, **T2** & **T5** are kept off.
2) **Current i**: **T3** is switched on to make current **i1**pass through the load.**T4**, **T5** & **T6** are switched on to have circulating paths for the current **i2**, **i3 & i4**. **T1**&**T2** are kept off.
3) **Current 0: T1**, **T4**, **T5** & **T6** are switched on to have circulating paths for currents **i1**, **i2**, **i3** & **i4**. **T2** and **T3** are kept switched off thus, no current pass through the load.
4) **Current –i: T2** is switched on to make current **i2** pass through the load, in the opposite direction. **T1**, **T5** & **T6** are switched on to have circulating paths for currents **i1**, **i3** & **i4**. **T3** & **T4** are kept off.
5) **Current–2i: T2** is switched on to make currents **i2** & **i4** pass through the load, in the opposite direction. **T1** & **T5** are switched on to have circulating paths for currents **i1** & **i3**. **T3**, **T4** & **T6** are kept off.

| 1 | 2 | 3 | 4 | 5 | 6 | Output |
|---|---|---|---|---|---|---|
| ! | ! | # | # | ! | # | +2i |
| ! | ! | # | # | # | # | +i |
| # | ! | ! | # | # | # | 0 |
| # | # | ! | ! | # | # | -i |
| # | # | ! | ! | # | ! | -2i |

Table B. Switching sequence of five-level CSI
! : - represents switch is OFF, #: - represents switch is ON

### *A3. SEVEN-LEVEL CSI*

Figure 4 gives the circuit set-up for 7-level CSI. The switches (**T1** to **T8**) are linked to a common-source level. Table C gives the sequence for switching of the 7-level CSI to have 7-level current output waveform. Here all the sources (DC current) is of same amplitude given as **i1=i2=i3=i4=i5=i6=i**.

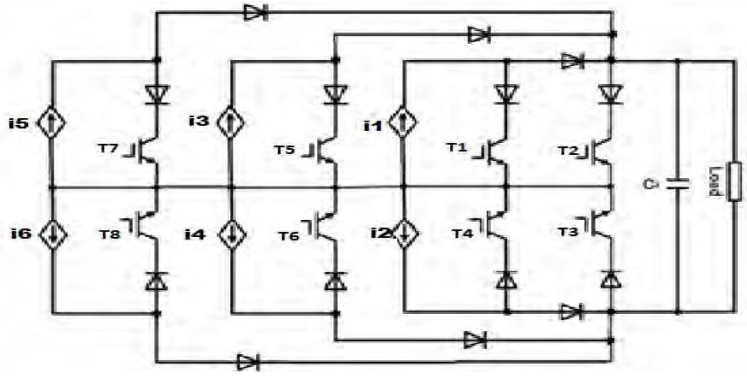


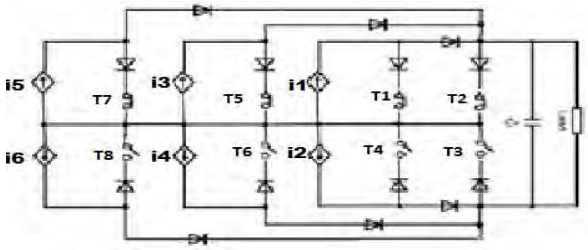

Figure4. Seven (7)-Level CSI

The 7-level current output (+**3i**, +**2i**, +**i**, **0**, **-i**,**-2i** & **-3i** current-level) are obtained by:

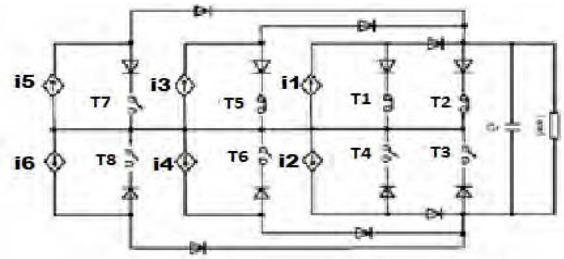
1) **Current 3i: T3** is switched on to make current **i3**, **i1** & **i5** pass through the load. **T4**, **T6** & **T8** are switched on to have circulating paths for the currents **i2, i4** & **i6**. **T1**, **T2**, **T5** & **T7** are kept off.
2) **Current 2i**:**T3** is switched on to make currents **i1**& **i3** pass through the load.**T4**, **T6**, **T7** & **T8** are switched on to have circulating paths for the currents **i2**, **i4**, **i5** & **i6**. **T1**, **T2** & **T5** are kept off.
3) **Current i: T3** is switched on to make current **i1** pass through the load. **T4**, **T5**, **T6**, **T7** & **T8**are switched on to have the circulating paths for the current **i2**, **i3**, **i4**, **i5** & **i6**. **T1** & **T2** are kept off.
4) **Current 0: T1**, **T4**, **T5**, **T6**, **T7** & **T8** are switched on to have circulating paths for currents **i1**, **i3**, **i5**, **i2**, **i4 & i6**. **T3** & **T2** are kept switched off thus, no current pass through the load.
5) **Current –i: T2** is switched on to make current **i2** pass through the load, in the opposite direction. **T1**, **T5**, **T6**, **T7** & **T8**are switched on to have circulating paths for currents **i1**, **i3**, **i4**, **i5** & **i6**. **T3** &**T4** are kept off.
6) **Current –2i: T2** is switched on to make currents **i2** & **i4** pass through the load, in the opposite direction. **T1**, **T5**, **T7** & **T8** are switched on to have circulating paths for currents **i1**, **i3**, **i5** & **i6**. **T3**, **T4** & **T6** are kept off.
7) **Current –3i: T2** is switched on to make currents **i2**, **i4** & **i6**pass through the load, in the opposite direction. **T1**, **T5** & **T7** are switched on to have circulating paths for currents **i1**, **i3** & **i5**. **T3**, **T4**, **T6** & **T8**are kept off.

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | Output |
|---|---|---|---|---|---|---|---|---|
| ! | ! | # | # | ! | # | ! | # | 3i |
| ! | ! | # | # | ! | # | # | # | 2i |
| ! | ! | # | # | # | # | # | # | I |
| # | ! | ! | # | # | # | # | # | 0 |
| # | # | ! | ! | # | # | # | # | -i |
| # | # | ! | ! | # | ! | # | # | -2i |
| # | # | ! | ! | # | ! | # | ! | -3i |

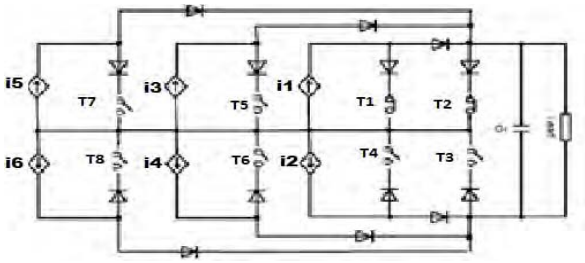
Table C. Switching sequence of seven-level CSI
! : - represents switch is OFF, #: - represents switch is ON



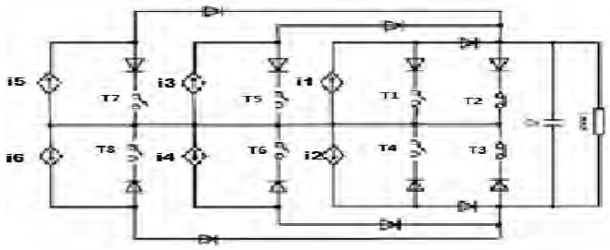

(1) Current +3i



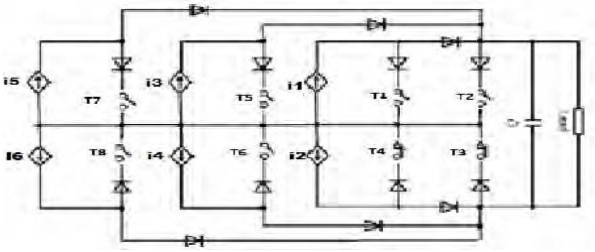

(2) Current +2i



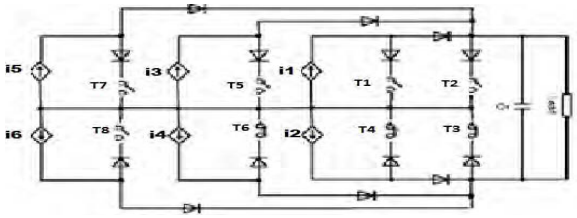

(3) Current +i



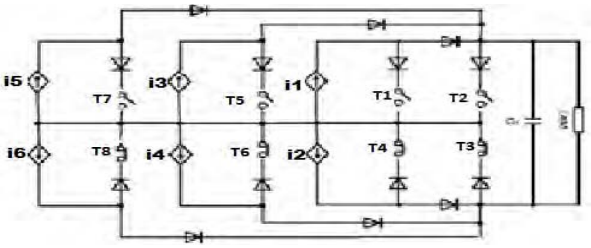

(4) Current 0




(5) Current –i




(6) Current –2i




(7) Current –3i

### *A4. NINE-LEVEL CSI*

Figure 5 gives the circuit set-up for 9-level CSI. The switches (**T1** to **T10**) are linked to a common-source level. Table D gives the sequence for switching of the 9-level CSI to have 9-level current output waveform. Here all the sources (DC current) is of same amplitude given as **i1= i5= i3= i7= i2= i6= i4= i8= i**.

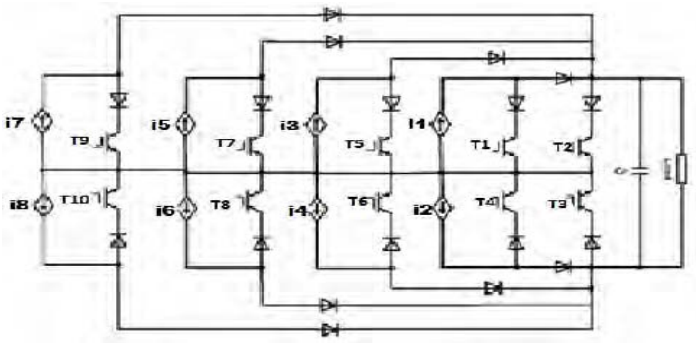


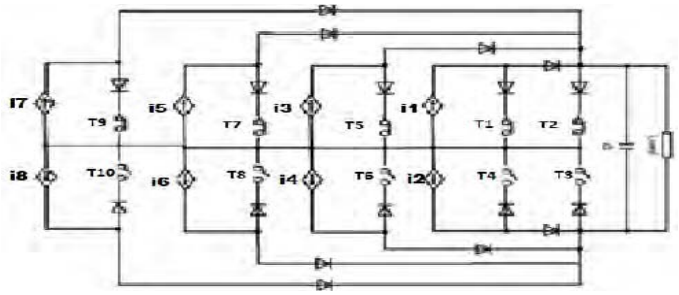

Figure5. Nine-Level CSI

The 9-level current output (+**4i**, +**3i**, +**2i**, +**i**, **0**, **-i**, **-2i**,**-3i** & **-4i** current-level) are obtained as follows:

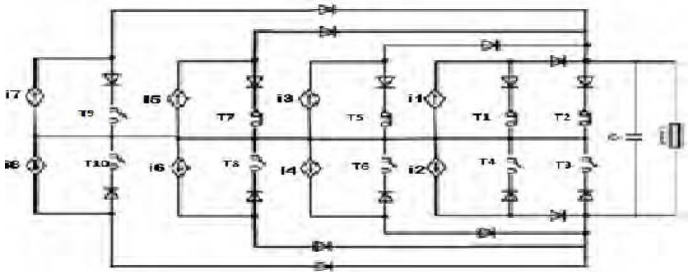
1) **Current 4i: T3** is switched on to make currents **i1**, **i3**, **i5** & **i7**pass through the load. **T4**, **T6**, **T8**&**T10** are switched on to have circulating paths for the currents **i2**, **i4**, **i6** & **i8**. **T1**, **T2**, **T5**, **T7** & **T9** are kept off.
2) **Current 3i: T3** is switched on to make currents **i1**, **i3** & **i5**pass through the load. **T4**, **T6**, **T8**, **T9** & **T10** are switched on to have circulating paths for the currents **i2**, **i4**, **i6**, **i7** & **i8**. **T1**, **T2**, **T5** & **T7** are kept off.
3) **Current 2i: T3** is switched on to make currents **i1**&**i3**pass through the load. **T4**, **T6**, **T7**, **T8**, **T9** & **T10** are switched on to have circulating paths for the currents **i2**, **i4**, **i5**, **i6**, **i7** & **i8**. **T1**, **T2** & **T5** are kept off.
4) **Current i: T3** is switched on to make current **i1** pass through the load. **T4**, **T6**, **T8**, **T10, T5**, **T7** & **T9** are switched on to have circulating paths for the current **i2**, **i4**, **i6**, **i8**, **i3**, **i5** & **i7**. **T2** & **T1** are kept switched off.
5) **Current 0: T1**, **T5**, **T7**, **T9**, **T4**, **T6**, **T8** & **T10** are switched on to have the circulating paths for currents **i1**, **i5**, **i3**, **i7**, **i2**, **i6**, **i4** & **i8**. **T3** & **T2** are kept switched off thus, no current flow through the load.
6) **Current –i: T2** is switched on to make current **i2** pass through the load, in the opposite direction. **T1**, **T5**, **T6**, **T7**, **T8**, **T9** & **T10** are switched on to have circulating paths for currents **i1**, **i3**, **i5**, **i7**, **i4**, **i6** & **i8**. **T4** & **T3** are kept off.
7) **Current –2i: T2** is switched on to make currents **i2** and **i4** pass through the load, in the opposite direction. **T1**, **T5**, **T7**, **T8**, **T9** & **T10** are switched on to have circulating paths for currents **i1**, **i3**, **i5**, **i6**, **i7** & **i8**. **T3**, **T4** & **T6** are kept off.
8) **Current –3i: T2** is switched on to make currents **i2**, **i4** and **i6** pass through the load, in the opposite direction. **T1**, **T5**, **T7**, **T9** & **T10** are switched on to have circulating paths for currents **i1**, **i3**, **i5**, **i7** & **i8**. **T3**, **T4**, **T6** & **T8** are kept off.
9) **Current -4i: T2** is switched on to make currents **i2**, **i4**, **i6** & **i8** pass through the load, in the opposite direction. **T1**, **T5**, **T7** & **T9** are switched on to have circulating paths for currents **i1**, **i3**, **i5** & **i7**. **T3**, **T4**, **T6**, **T8** & **T10**are kept switched off.

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | Output |
|---|---|---|---|---|---|---|---|---|---|---|
| ! | ! | # | # | ! | # | ! | # | ! | # | 4i |
| ! | ! | # | # | ! | # | ! | # | # | # | 3i |
| ! | ! | # | # | ! | # | # | # | # | # | 2i |
| ! | ! | # | # | # | # | # | # | # | # | i |
| # | ! | ! | # | # | # | # | # | # | # | 0 |
| # | # | ! | ! | # | # | # | # | # | # | -i |
| # | # | ! | ! | # | ! | # | # | # | # | -2i |
| # | # | ! | ! | # | ! | # | ! | # | # | -3i |
| # | # | ! | ! | # | ! | # | ! | # | ! | -4i |

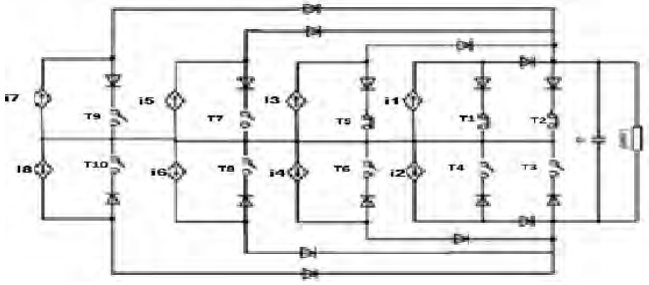
Table D. Switching sequence of nine-level CSI
! : - represents switch is OFF, #: - represents switch is ON



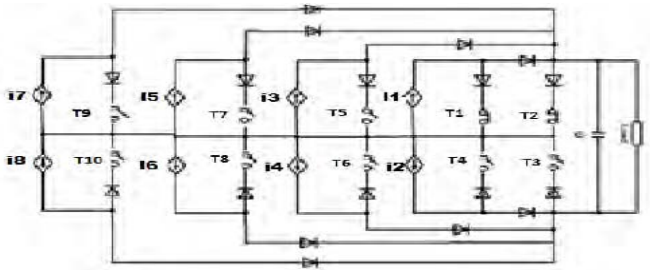

(1) Current +4i



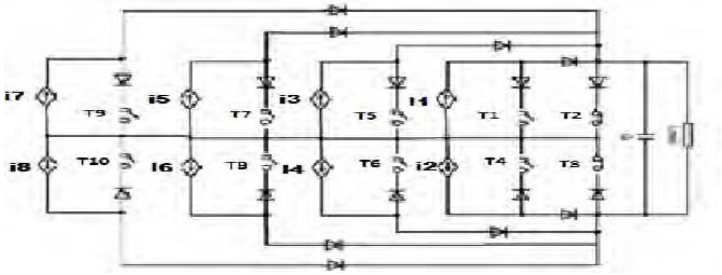

(2) Current +3i



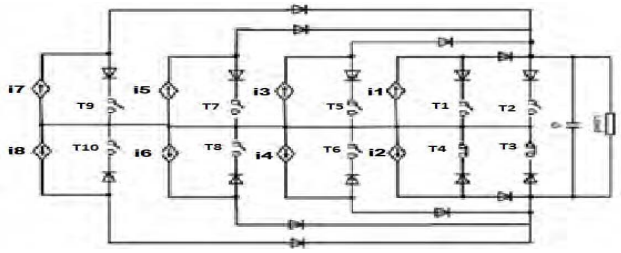

(3) Current +2i



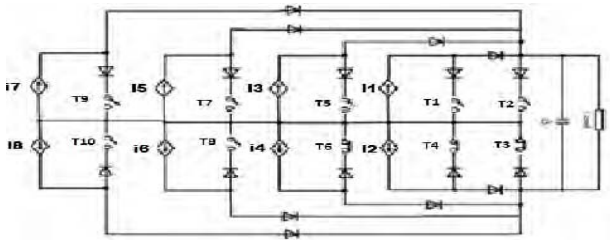

(4) Current +i



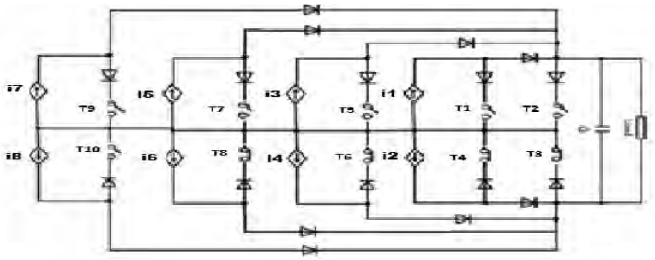

(5) Current 0



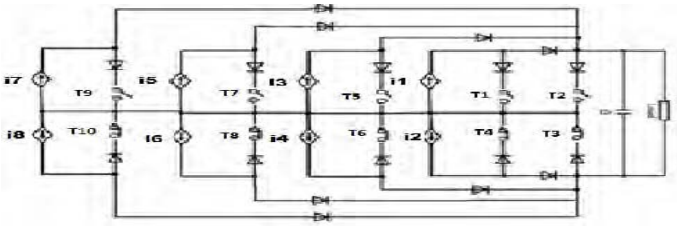
(6) Current –i



(7) Current –2i



(8) Current –3i



(9) Current –4i

### *A4. ELEVEN-LEVEL CSI*

Figure 6 gives the circuit set-up for 11-level CSI. The switches (**T1** to**T12**) are linked to a common-source level. Table E gives the sequence for switching of the 11-level CSI to have 11-level current output waveform. Here all the sources (DC current) is of same amplitude given as **i1=i5=i9=i7=i3=i2=i6=i10=i4=i8=i.**

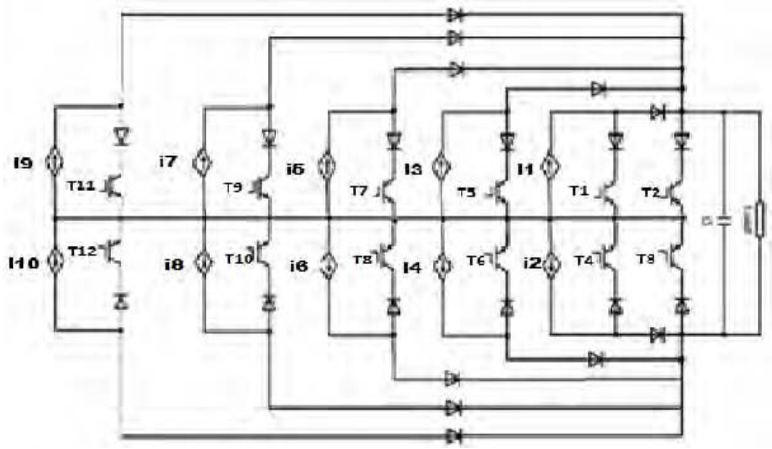


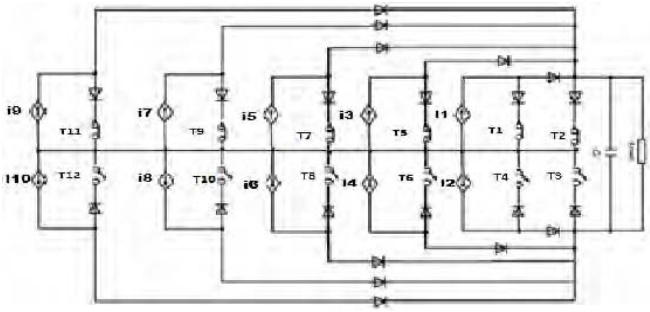
Figure6. Eleven-Level CSI

The 11-level current output (+**5i**, +**4i**, +**3i, +2i**, +**i**, **0**, **-i**, **-2i**, **-3i**, **-4i**&**-5i** current-level) are obtained by:

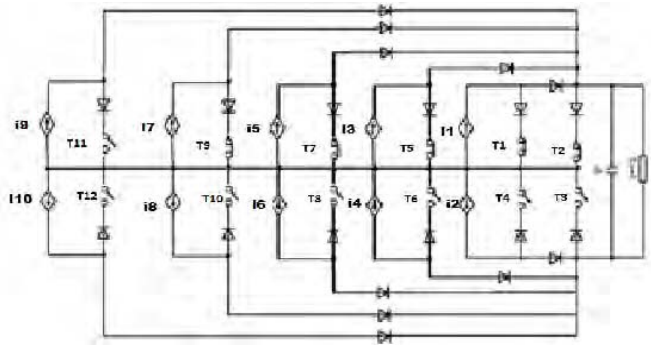
1) **Current 5i: T3** is switched on to make currents **i1**, **i3**, **i5**, **i7** & **i9** pass through the load. **T4**, **T6**, **T8**, **T10** & **T12** are switched on to have circulating paths for the currents **i2**, **i4**, **i6**, **i8** & **i10**. **T1**, **T2**, **T5**, **T7**, **T9** & **T11** are kept switched off.
2) **Current 4i: T3** is switched on to make currents **i1**, **i3**, **i5** & **i7** pass through the load. **T4**, **T6**, **T8**, **T10**, **T11** & **T12** are switched on to have circulating paths for the currents **i2**, **i4**, **i6**, **i8**, **i9** & **i10**. **T1**, **T2**, **T5**, **T7** & **T9** are kept switched off.
3) **Current 3i: T3** is switched on to make currents **i1**, **i3** & **i5** passthrough the load. **T4**, **T6**, **T8**, **T9**, **T10**, **T11** and **T12** are switched on to have circulating paths for the currents **i2**, **i4**, **i6**, **i7**, **i8**, **i9** & **i10**. **T1**, **T2**, **T5** & **T7** are kept switched off.
4) **Current 2i: T3** is switched on to make currents **i1** & **i3**passthrough the load. **T4**, **T6**, **T8**, **T10**, **T12**, **T7**, **T9, T11** & **T12** are switched on to have circulating paths for the currents **i2**, **i4**, **i6**, **i8**, **i10**, **i5**, **i7** & **i9**. **T1**, **T5** & **T2** are kept switched off.
5) **Current i: T3** is switched on to make current **i1**passthrough the load. **T4**, **T6**, **T8**, **T10**, **T12**, **T5**, **T7**, **T9** & **T11**are switched on to have circulating paths for the current **i2**, **i4**, **i6**, **i8**, **i10**, **i3**, **i5**, **i7** & **i9**. **T2** & **T1** are kept switched off.
6) **Current 0: T1**, **T7**, **T11**, **T5**, **T9**, **T4**, **T8**, **T12**, **T8** & **T10** are switched on to have the circulating paths for currents **i1**, **i5**, **i9**, **i3**, **i7**, **i2**, **i6**, **i4**, **i8** & **i10**. **T3** & **T2** are kept switched off thus, no current flow through the load.
7) **Current –i: T2** is switched on to make current **i2** pass through the load, in the opposite direction. **T1**, **T7**, **T11**, **T5**, **T9**, **T6**, **T12**, **T8** & **T10** are switched on to have circulating paths for currents **i1**, **i5**, **i3**, **i9**, **i7**, **i4**, **i8**, **i6** & **i10**. **T4** & **T3** are kept switched off.
8) **Current –2i: T2** is switched on to make currents **i2** & **i4** pass through the load, in the opposite direction. **T1**, **T5**, **T7**, **T8**, **T9**, **T10**, **T11** & **T12** are switched on to have circulating paths for currents **i1**, **i3**, **i5**, **i6**, **i7**, **i8**, **i9** & **i10**. **T3**, **T4** & **T6** are kept switched off.
9) **Current –3i: T2** is switched on to make currents **i2**, **i4** & **i6** pass through the load, in the opposite direction. **T1**, **T5**, **T7**, **T9**, **T10**, T**11** & **T12** are switched on to have circulating paths for currents **i1**, **i3**, **i5**, **i7 & i8**. **T3**, **T4**, **T6** & **T8** are kept switched off.
10) **Current –4i: T2** is switched on to make currents **i2**, **i4**, **i6** & **i8** pass through the load, in the opposite direction. **T1**, **T5**, **T7**, **T9**, **T11** & **T12** are switched on to have circulating paths for currents **i1**, **i3**, **i5**, **i7**, **i9** & **i10**. **T3**, **T4**, **T6**, **T8** & **T10** are kept switched off.
11) **Current –5i: T2** is switched on to make currents **i2**, **i4**, **i6**, **i8** & **i10** pass through the load, in the opposite direction. **T1**, **T5**, **T7**, **T9** & **T11** are switched on to have circulating paths for currents **i1**, **i3**, **i5**, **i7** & **i9**. **T3**, **T4**, **T6**, **T8**, **T10** & **T12** are kept switched off.

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | O/P |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ! | # | # | # | ! | # | ! | # | ! | # | ! | # | +5i |
| ! | # | # | # | ! | # | ! | # | ! | # | # | # | +4i |
| ! | # | # | # | ! | # | ! | # | # | # | # | # | +3i |
| ! | # | # | # | ! | # | # | # | # | # | # | # | +2i |
| ! | ! | # | # | # | # | # | # | # | # | # | # | +i |
| # | ! | ! | # | # | # | # | # | # | # | # | # | 0 |
| # | ! | ! | ! | # | # | # | # | # | # | # | # | -i |
| # | ! | ! | ! | # | ! | # | # | # | # | # | # | -2i |
| # | ! | ! | ! | # | ! | # | ! | # | # | # | # | -3i |
| # | ! | ! | ! | # | ! | # | ! | # | ! | # | # | -4i |
| # | ! | ! | ! | # | ! | # | ! | # | ! | # | ! | -5i |

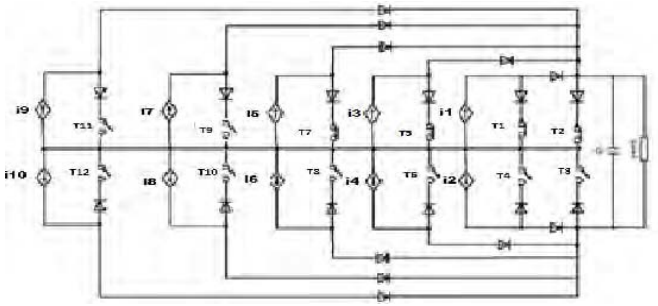
Table E. Switching sequence of eleven-level CSI
! :- represents switch is OFF, #: - represents switch is ON



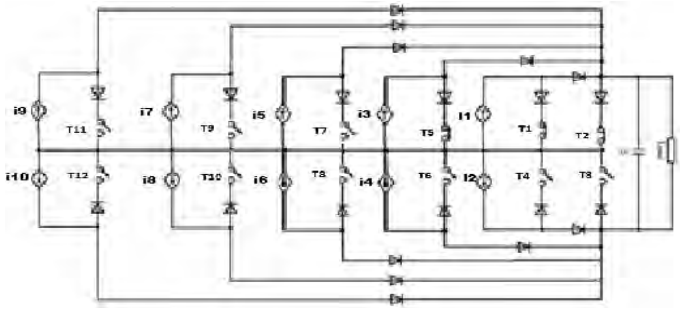

(1) Current +5i



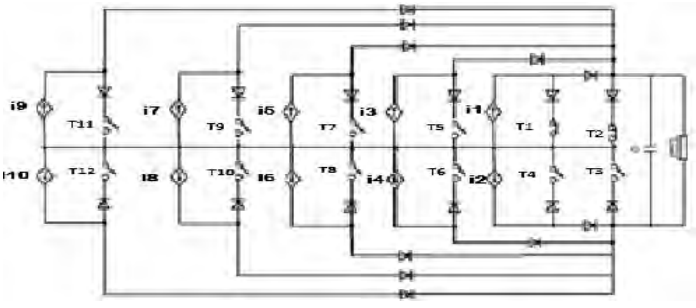

(2) Current +4i



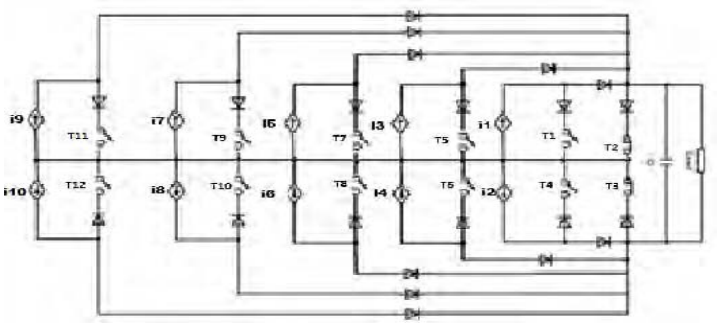

(3) Current +3i



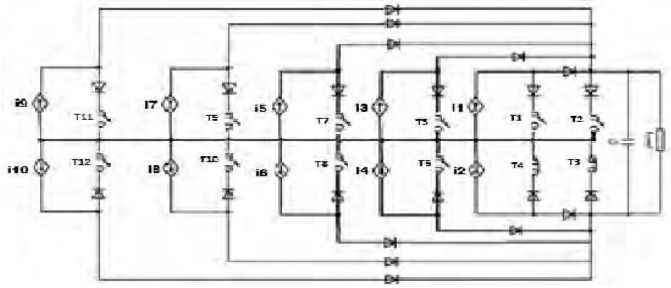

(4) Current +2i



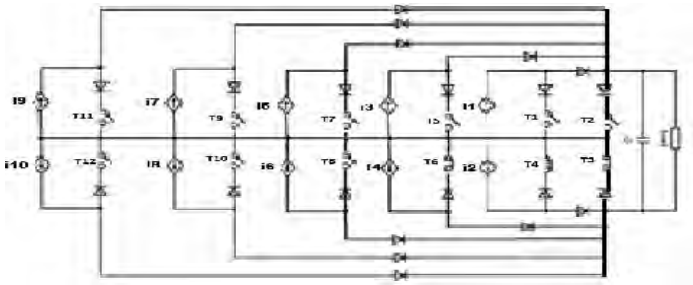

(5) Current +i



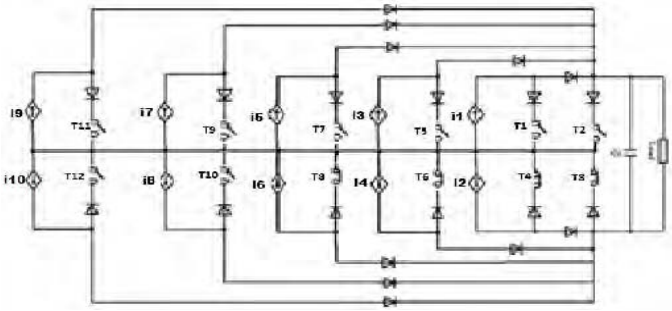
(6) Current 0



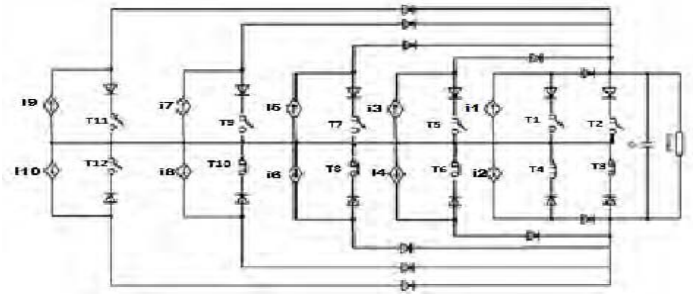
(7) Current –i



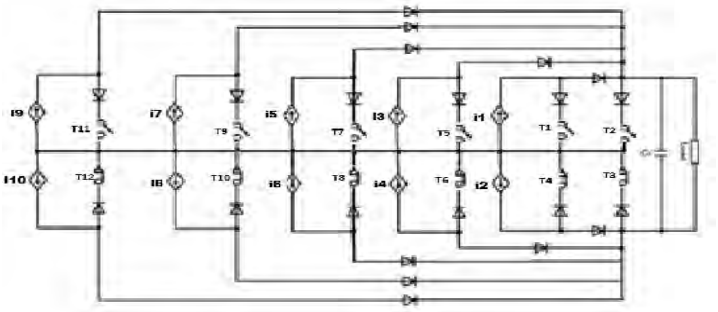
(8) Current –2i



(9) Current –3i



(10) Current –4i



(11) Current –5i

*B. PWM Modulation Strategy*

The Pulse Width Modulation (PWM) operation is employed, to acquire an improved current output waveform with low distortion, rather than staircase waveform technique. The staircase waveform technique can be acquired easily in view of switching frequency, but its main drawback is that it leads to more output waveform distortion and it requires a large size of filter.

This CSI topology has a Sinusoidal Pulse width modulation (SPWM) based with multi carrier level shifted operation which is used to have the CSI switches gate signals, have the PWM current waveform as in figure 7. The carrier waveforms will be in phase to each other having equal frequency. The modulated signals frequency (sinusoidal reference waveform) gives the current output waveform fundamental frequency whereas, the CSI switches switching frequency is given by triangular carrier waves frequency. N-1 triangular carriers of equal frequency are needed to have N-level current waveform output with this modulation.

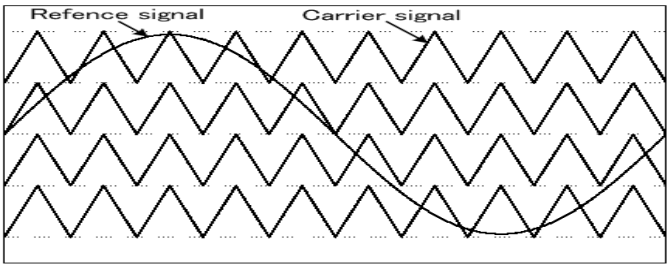



Figure7. Sinusoidal PWM based with Multi-carrier

## III. RESULT OF COMPUTER SIMULATION

The working of this CSI for different level CSI (three-level, five-level, seven-level, nine-level and eleven-level) are verified using computer simulation with MATLAB software. In this topology, RL load is considered with R = 10Ω, L = 1.2mH and filter capacitor (cf) = 5μf. The switching frequency considered is 50KHZ. The triggering sequence, voltage output waveform and current output waveform for different level CSI are listed below:

### *A1. THREE-LEVEL CSI*

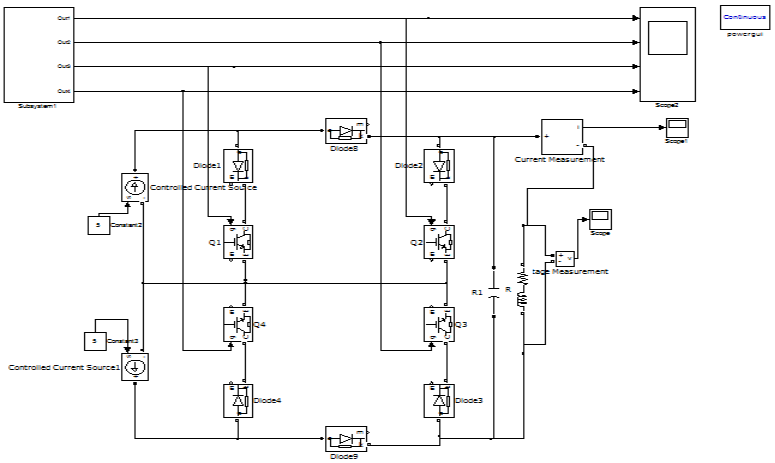



Figure8 (a) MATLAB Configuration

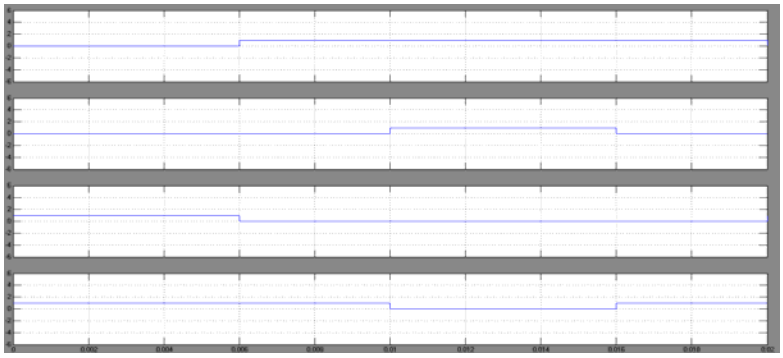


Figure8 (b) Triggering Sequence

Figure8 (c) Output Voltage Waveforms

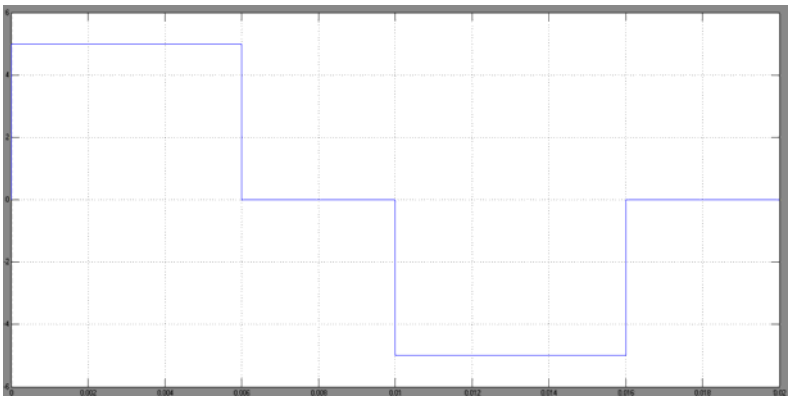


Figure8 (d) Output Current Waveforms

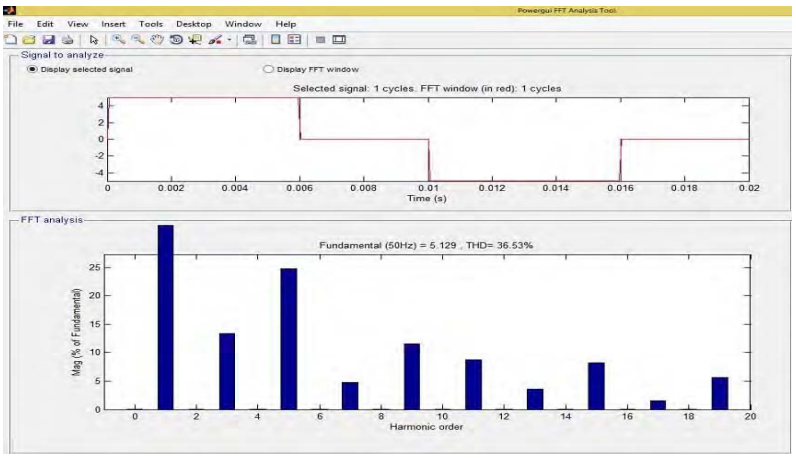



Figure 8 (e) THD Analysis

### *A2. FIVE-LEVEL CSI*

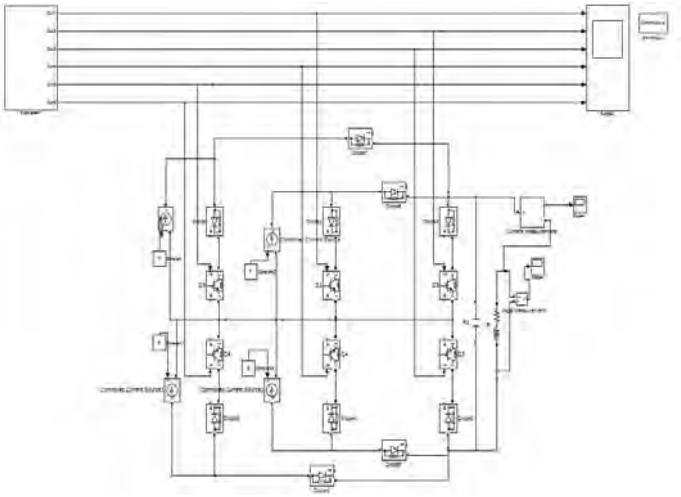


Figure 9 (a) MATLAB Configuration

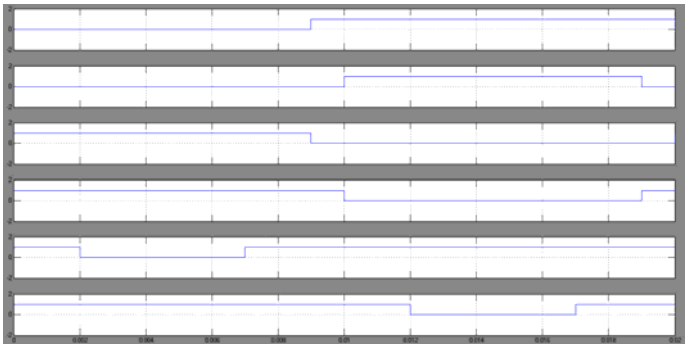


Figure 9 (b) Triggering sequence

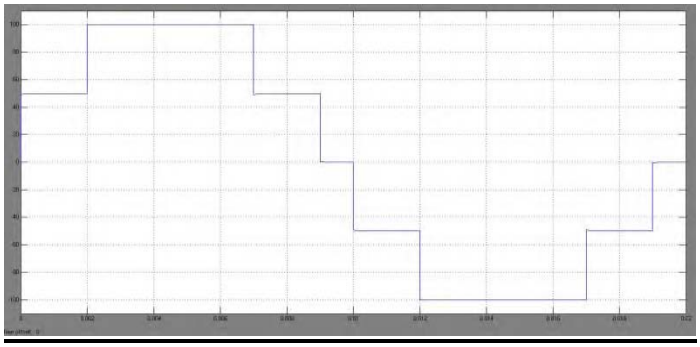


Figure 9 (c) Output voltage waveforms

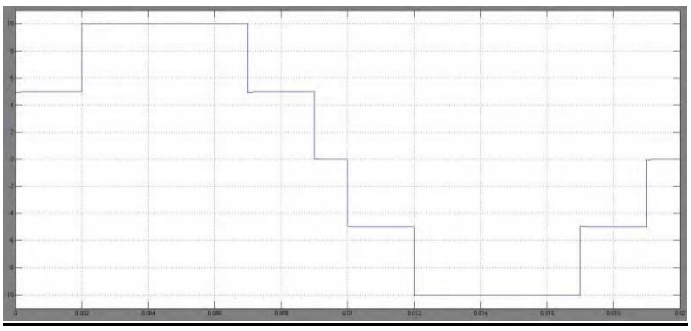


Figure 9 (d) Output Current Waveforms

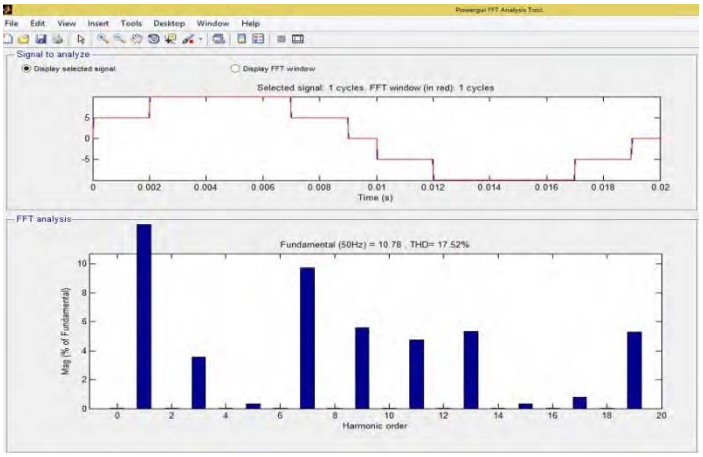



Figure 9 (e) THD Analyses

### *A3. SEVEN-LEVEL CSI*

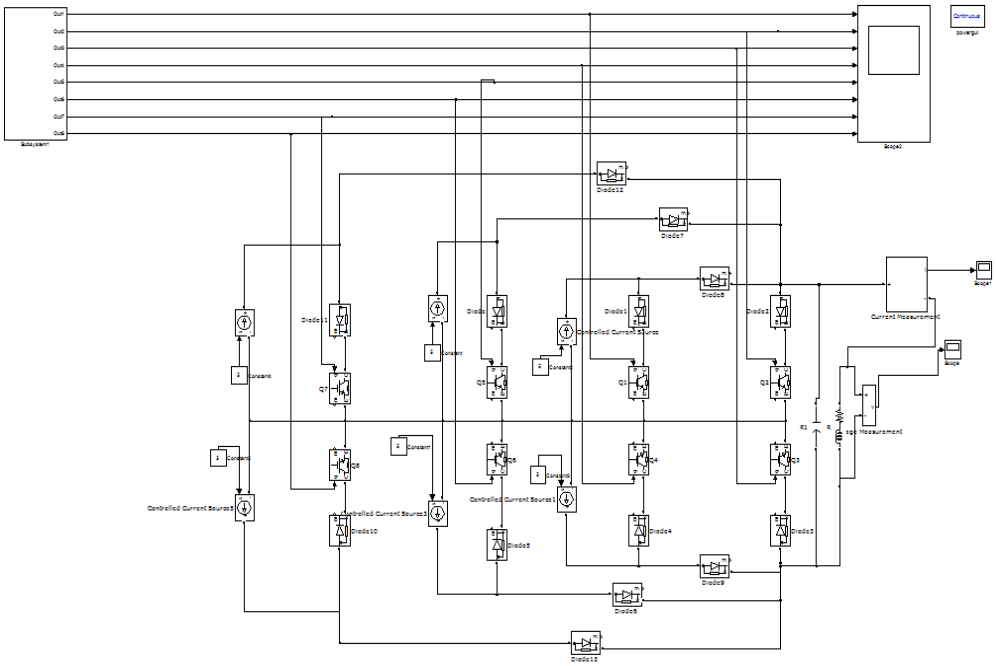


Figure 10 (a) MATLAB Configuration

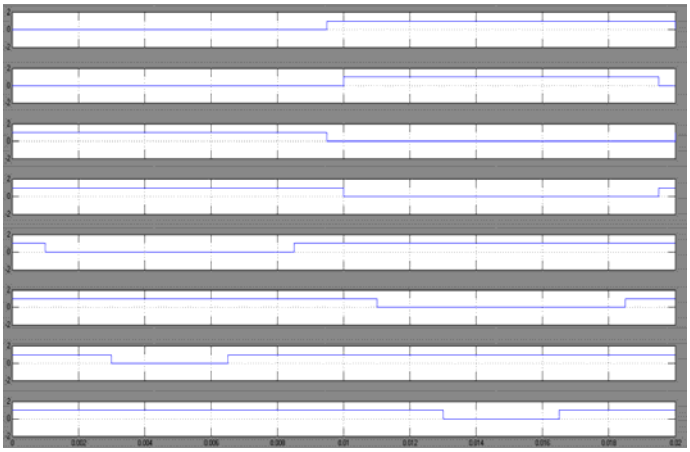


Figure 10 (b) Triggering Sequence

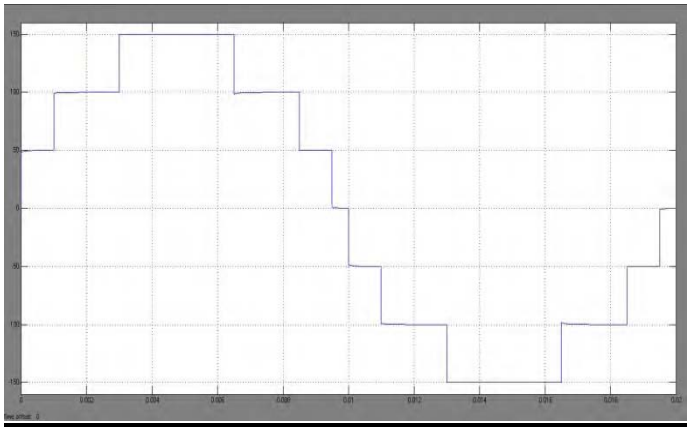


Figure 10 (c) Output voltage waveforms

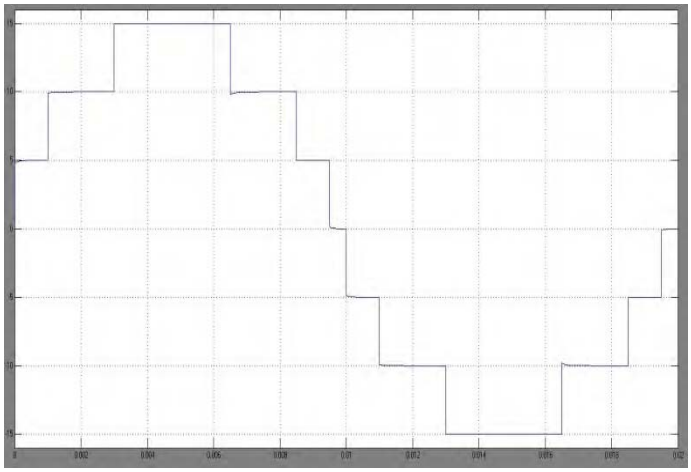


Figure 10 (d) Output Current Waveforms

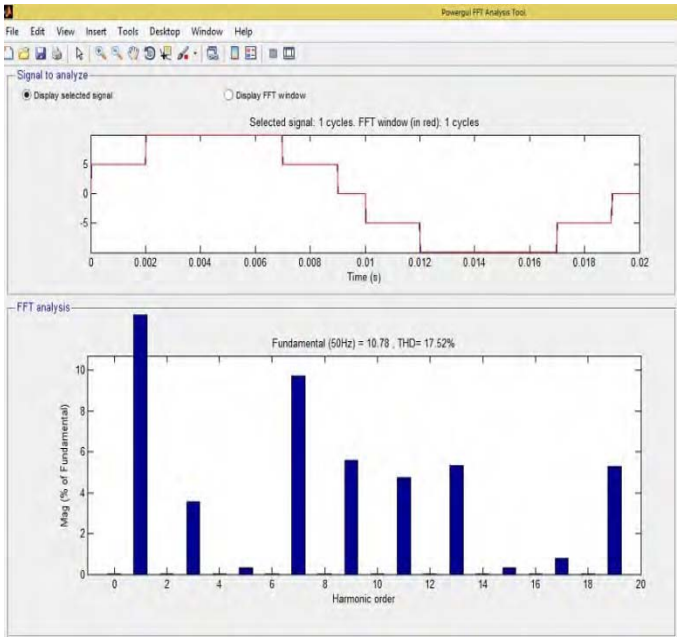



Figure 10 (e) THD Analyses

### *A4. NINE-LEVEL CSI*

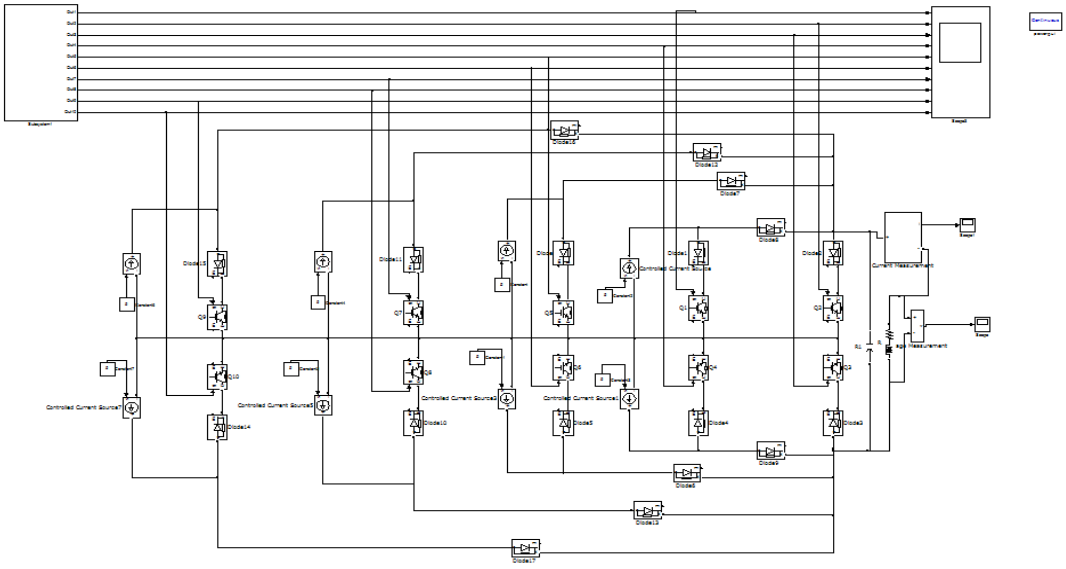


Figure 11 (a) MATLAB Configuration

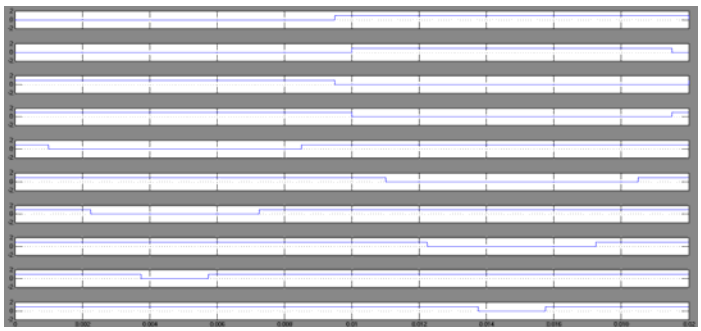


Figure 11 (b) Triggering Sequence

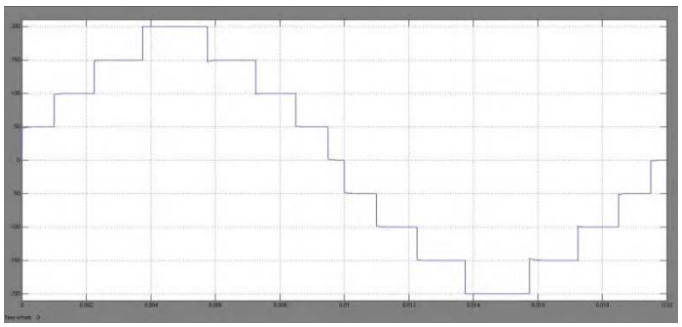


Figure 11 (c) Output Voltage Waveforms

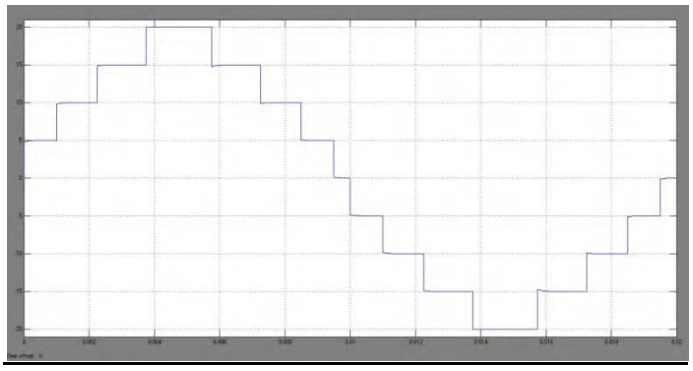


Figure 11 (d) Output Current Waveforms

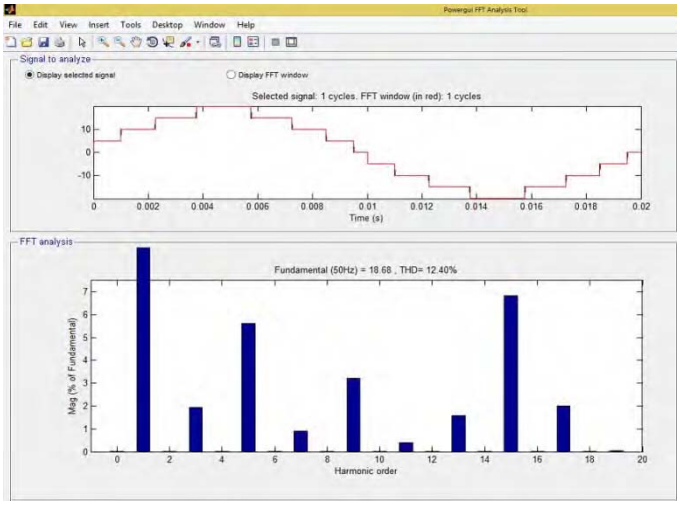



Figure 11 (e) THD Analyses

### *A5. ELEVEN-LEVEL CSI*

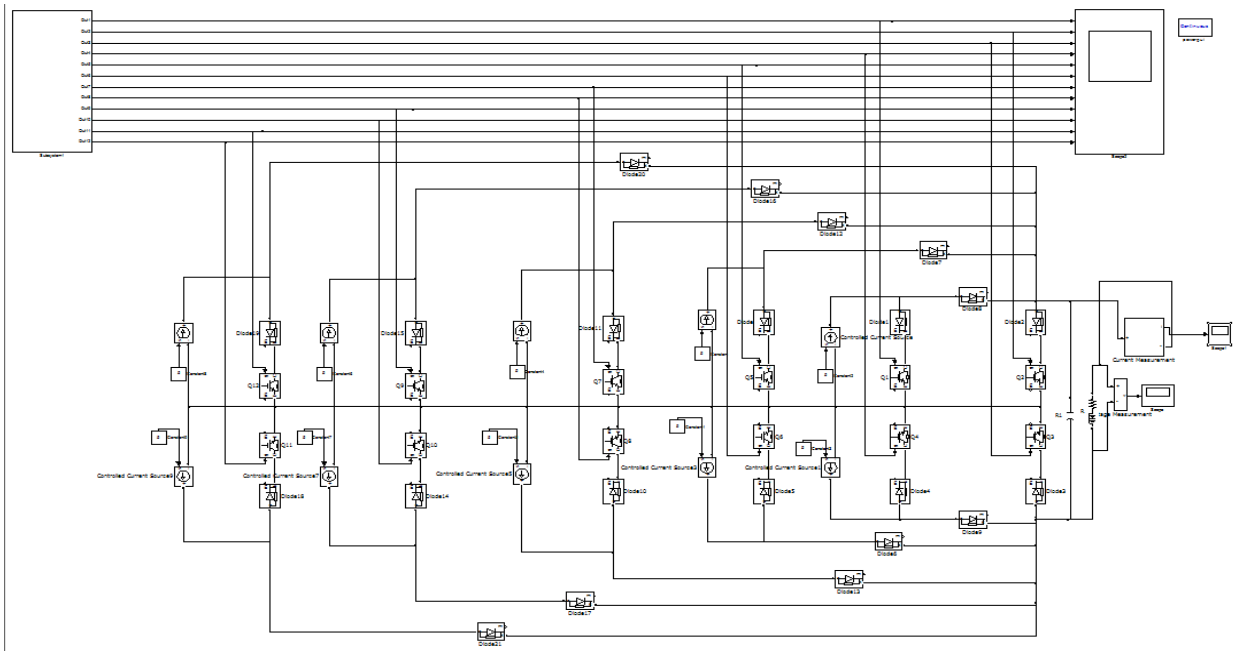


Figure 12 (a) MATLAB Configuration

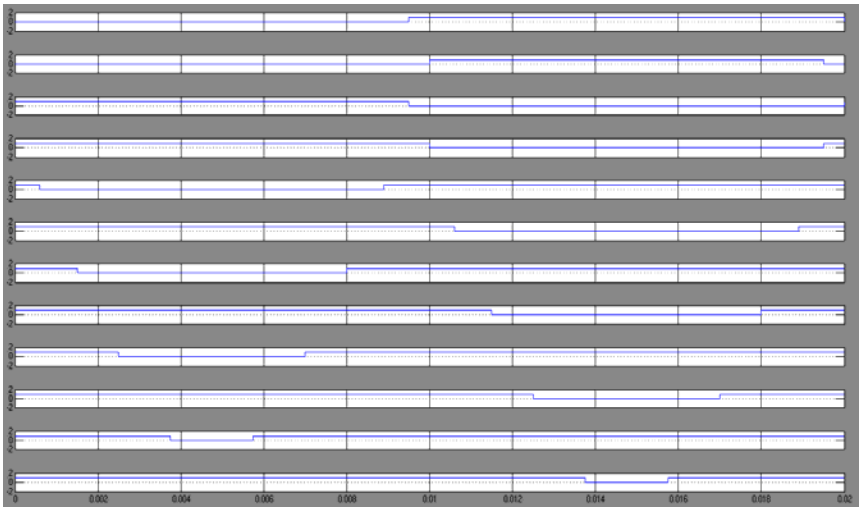


Figure 12 (b) Triggering Sequence

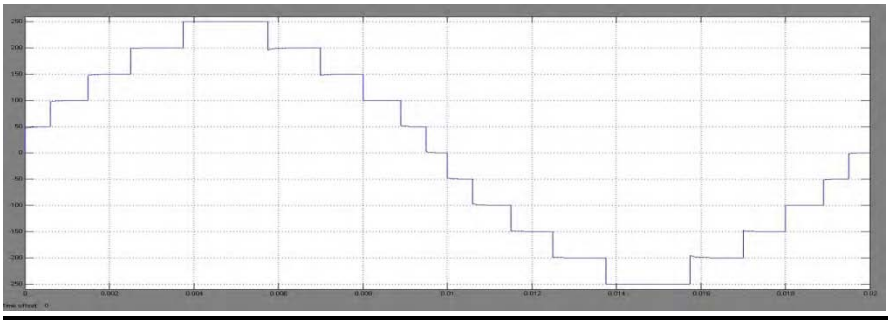


Figure 12 (c) Output Voltage Waveforms

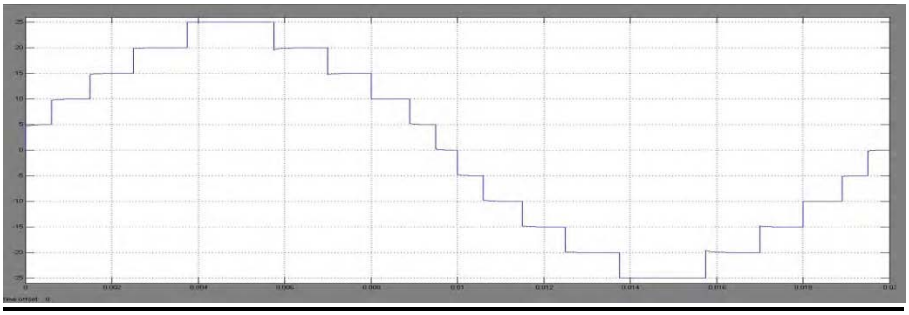


Figure 12 (d) Output Current Waveforms

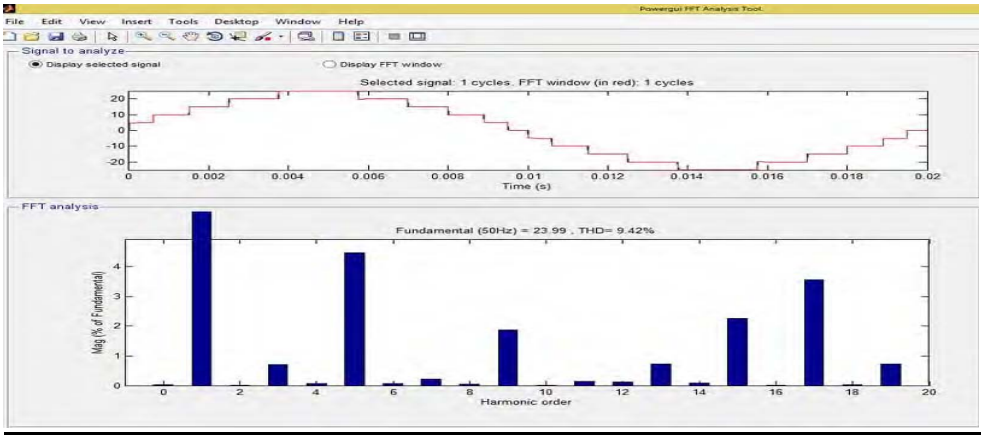



Figure 12 (e) THD Analyses

Table 6 gives the comparison of total harmonic distortion (THD) for different level of CSI with the number of switches and the power supplies.

| CSI-level | Power Switch | Power Supply | Fundamental Voltage (V) | Fundamental Current (A) | THD |
|---|---|---|---|---|---|
| Three | 04 | 02 | 51.29 | 5.129 | 36.53 |
| Five | 06 | 04 | 107.8 | 10.78 | 17.52 |
| Seven | 08 | 06 | 155.5 | 15.55 | 15.11 |
| Nine | 10 | 08 | 186.8 | 18.68 | 12.40 |
| Eleven | 12 | 10 | 239.9 | 23.99 | 09.42 |

## IV. CONCLUSION

In this paper the different levels of the CSI topology have been given and its accuracy is verified by the use of the computer simulation with MATLAB software. This CSI multilevel inverter topology results in reduction of its gate drive circuit complexity and its control circuit. This CSI topology is also applicable if there is more number of switches to have utmost level of current waveform output. The different level of CSI topology THD is also analyzed and as the number of level increases the THD is reduced.

## V. REFERENCES


[1] Suroso and T. Noguchi, "Three-level Current-Source PWM Inverter with No Isolated Switching Devices for Photovoltai Conditioner," *IEEJ Transaction on Industry Application*, Vol. 129, No.15 2009.

[2] F. L. M. Antunes, A. C. Braga and I. Barbi, "Application of a generalized current multilevel cell to current source inverters," *IEEE Transaction on Power Electronic*," Vol. 46, No.1, February 1999.

[3] T. Noguchi, Y.Nozuki, and Suroso, "Discussion on Novel Topologies of Multi-level Power Converter Based on Duality," P*roceed. Of IEE-Japan Tech. Meet.*, SPC-08-89 (June, 2008) (in Japanese).

[4] B. P. McGrath, and D. G. Holmes, "Natural current Balancing of Multicell Current Source Inverter," *IEEE Transaction on Power Electronic*, Vol. 23, No.3, May 2008.

[5] G. Ledwich, "Current Source Inverter Modulation," *IEEE Transaction on Power Electronic*, Vol. 6, October 1991.

[6] S. Kwak, and H. A. Toliyat, "Multilevel Converter Topology Using Two Types of Current-Source Inverters," *IEEE Transaction on Inductry Applications*, Vol. 42, No.6, November/December 2006.