A Case Study of Nanoscale FPGA Programmable Switches with Low Power

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***Abstract*: The trend in VLSI and system design is moving away from high speed to low power due to the rapid growth in the portable consumer electronics market. The technology evolution of deep submicron (DSM) will be able to manage the needs and demands of future computing world. A rapid growth of future computing have led to challenges of very deep submicron (DSM) regime. Here, the leakage power plays a major contributor to the total power dissipation involved in the circuit as the threshold voltage becomes small while we reduce the operating supply voltage. We present some techniques to reduce the power dissipation involved while interconnecting logic blocks in the Field Programmable Gate Arrays (FPGAs). The interconnections or connectivity among logic blocks are done by routing switches. We use pass-transistor logic, transmission logic and multiplexers for the construction of these routing switches. We present a technique which has both sleep mode in which the leakage power is reduced and low-power mode in which the dynamic power is reduced. These models are built by using Electronic Design Automation (EDA) tools like DSCH (Digital Schematic) and Microwind layout tools using BSIM4 MOSFET model in 60 nm technology. Results show that the pass-transistor approach is having low power consumption . The leakage and dynamic power are also reduced by the circuit which has the programmability option to change sleep mode and low-power mode.**

Keywords: DSM, Field-programmable gate arrays (FPGAs), interconnect, leakage, power.

I. INTRODUCTION

Since the transistor count and switching frequency were much low in the past decades, power dissipation was not an issue. As the technology shrinks, plenty of transistors, speedy and become much smaller, are being packed into a chip, which in turn increase the operational frequency and processing capacity per chip at a very higher rate. As a result increased power dissipation has come into picture. Since number of integrated transistors become double in once in 18 months, there is a much need to fabricate low power VLSI chips. Portable consumer electronic products powered by batteries is an another factor for low power VLSI Design, since the battery technology alone can not solve the low power problem [1].

High power dissipation also leads to the reduced time of operation, higher weight due to batteries, reduced mobility, cooling cost, and reduced reliability. Battery life time depends on the meantime between charging and system cost. Since the device temperature increases due to high density of transistors, the failure rate, cooling, and packing costs are the reasons for the low power digital VLSI design. Also, it disturbs the environment in the form of heat, it becomes a major problem nowadays.

In VLSI deep sub-micron technology, power dissipation is becoming widely recognized as a top-priority issue. Since there are millions of transistors placed in tiny chip, major problems of heat dissipation and large consumption of power would come into the picture. Due to the rise in temperature, reliability of an electronic decreases. So, timing i.e., performance degrades with temperature. Compared to dynamic current leakage current may dominate while we implement deep sub-micron 90 nm or below [2].

Since the number of transistors and operational frequency were much low in the past decades, power dissipation was not an issue. As the technology grows, faster and smaller transistors are being packed into a chip, which leads to a growth in operational frequency and processing capacity per chip in turn in increased power dissipation. Since number of integrated transistors become double in once in 18 months, there is a much need to fabricate low power VLSI chips. Portable consumer electronic products powered by batteries is an another factor for low power VLSI Design, since the battery technology alone can not solve the low power problem [3].

Because of higher weight batteries and lagging in battery technology, designers are forced to implement their designs with low power. To reduce the low power, both the dynamic and static power are being considered during the system operation. Techniques like by increasing the length of the transistors or reducing the width of the transistors in a circuit help to minimize the leakage power dissipation. Also, the methods like Multi-threshold mechanism, adaptive body biasing are used for minimizing leakage power. Like leakage power,

the dynamic power can be reduced by reducing the switching capacitance, the operating supply voltage and clock frequency. By doing so, the life time of a device or system can be increased [2].

The need for quick designs and less time-to-market has led to the deep research in Programmable logic Devices (PLDs). An organization of array of gates idea developed during the design era of Read Only Memories (ROM) . Then advanced technology like System On Programmable Chips (SOPC) become much popular which use programmable devices, memories and configurable logic all on one chip. Due to the technology evolution, these basic array structures like ROMs become to CPLD (Complex Programmable Logic Devices) and FPGAs [1].

II.IMPLEMENTATION OF PROGRAMMABLE SWITCHES IN AN FPGA

Over the last decade , for the implementation of digital circuits FPGAs are being used widely in industry. Programmable logic function and interconnect are the most critical part which decides the performance and other quality metrics of the design. FPGA architecture has a dramatic effect on the quality of the final device's speed performance, area efficiency, and power consumption.

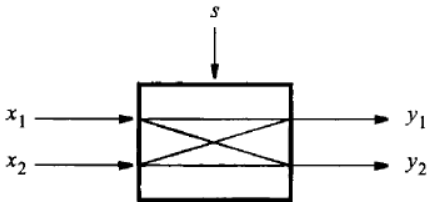

Figure 1: A 2x2 crossbar switch

A routing switch contains n inputs and k outputs, whose sole function is to provide a capability to connect any input to any output, is usually referred to as an nxk crossbar switch. Crossbars of various sizes can be created, with different number of inputs and outputs. When there are two inputs and two outputs, it is called a 2x2 crossbar. Figure 1 shows a basic 2x2 crossbar switch which can be implemented using multiplexers, pass transistors and transmission gates, etc [4].

A. Switch design using Multiplexer

Figure 2 shows a 2x2 crossbar which uses a 2-to-1 multiplexer as a basic component foe the switching mechanism. in which the multiplexer select inputs are controlled by the signal s which is shown in Figure 2. The wire x1 is get connected to y1 and x2 with y2 when s=0. The wire x1 is get connected to y2 and x2 with y1 when s = 1. Since one set of wires are having connected with another set of wires, these crossbar switches are pertinent where the connectivity is important. Figure 3 shows the simulation report using DSCH CAD tool and the results are verified. Multiplexers can also be used in a more general way to synthesize logic functions. The design becomes simple because of the 2-to-1 multiplexer involves very few number of transistors [7].

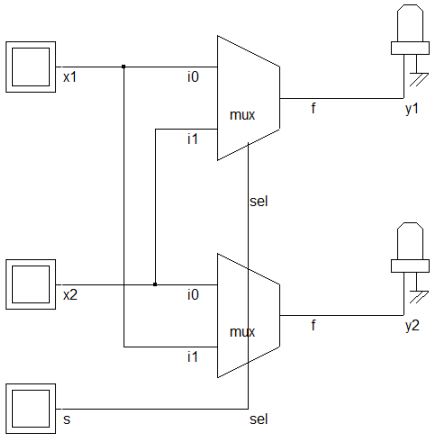

Figure 2: Switch using multiplexer

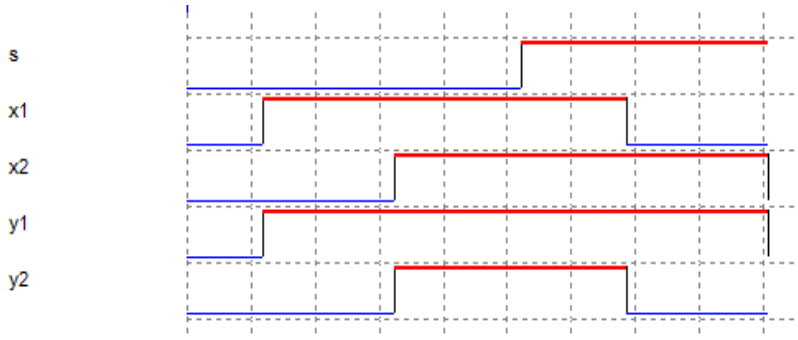

Figure 3: Simulation result using multiplexer

B. Switch design using Pass-transistor logic

To reduce the number of transistors involved in the design, the same can be implemented using pass transistors, which is shown in Figure 4. Here the design is implemented using nMOS pass transistors which are good for passing logic 0. While the pMOS pass transistors are good for passing logic 1. Since pMOS pass transistors are slower in speed, most of the logic circuit design may be implemented using nMOS logic or CMOS logic. Figure 5 shows the simulation timing diagram report for this pass-transistor logic implementation.

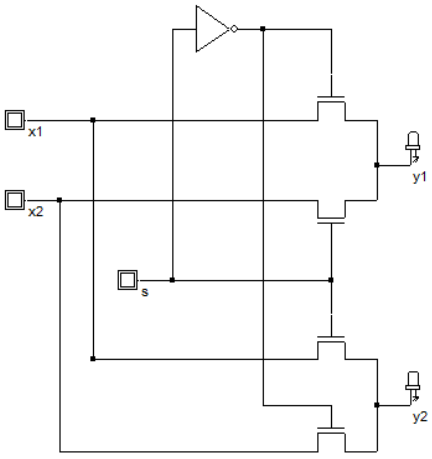

Figure 4: Switch using pass-transistor logic

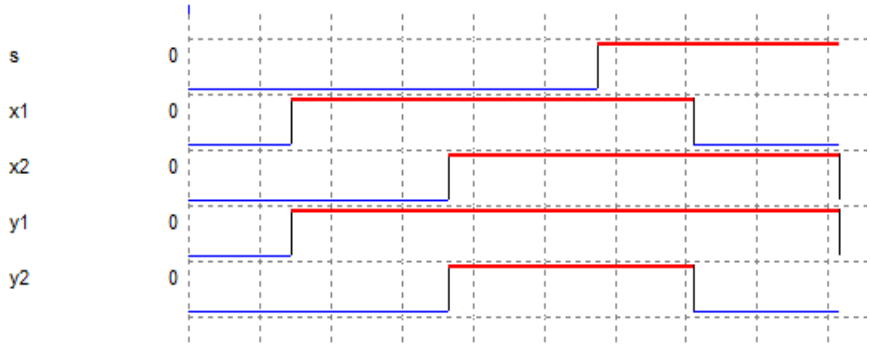

Figure 5: Simulation result using pass-transistor logic

C. Switch design using Transmission Gate logic

To avoid the threshold loss problem, both nMOS and pMOS transistors can be implemented, which is being referred as transmission gate logic. Figure 6 shows the design part and the functionally verification results are depicted in Figure 7. Transmission gates are widely used for multiplexer implementations. Even the logic blocks inside an FPGA are implemented multiplexers followed by memory elements to remember the previous data. Latches and Flip-Flops are also design by the transmission gates. The main advantage of the CMOS transmission gate compared to nMOS logic is to allow the input signal to be transmitted to the output without the threshold attenuation [7].

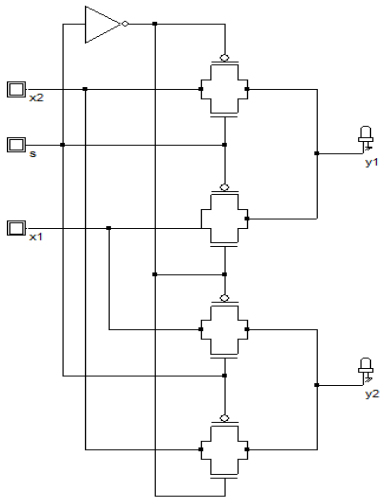

Figure 6: Switch using transmission gate logic

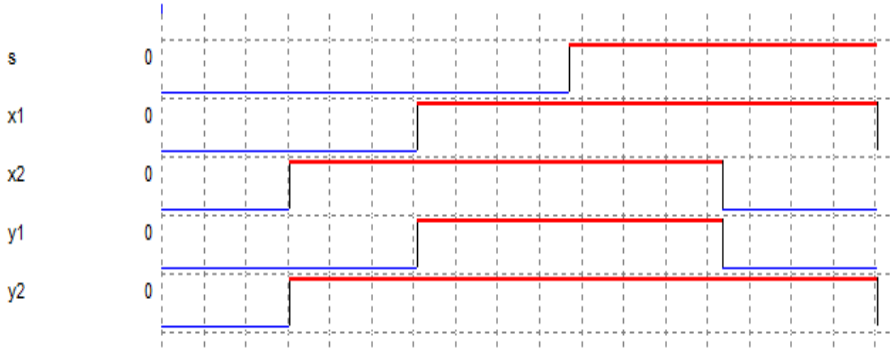

Figure 7: Simulation result using transmission gate logic

III. FOUR INPUT ROUTING SWITCH WITH LOW LEAKAGE POWER

A variety of techniques for leakage optimization in ASICs have been proposed and we present one of the technique to reduce the static power for the 4-input routing switch which is shown in Figure 8. Here the nMOS transistors are used to implement a 4-to-1 multiplexer along with the level-restoring buffer. Here the additional pMOS transistor (MP) serves the buffer's input to rail V_{DD} when the logic-1 were passed through the switch. Otherwise, a weak '1' may be transferred via the multiplexer which causes the pMOS turned partially ON in the buffer circuit. So, here a reasonable amount of leakage power may be reduced.

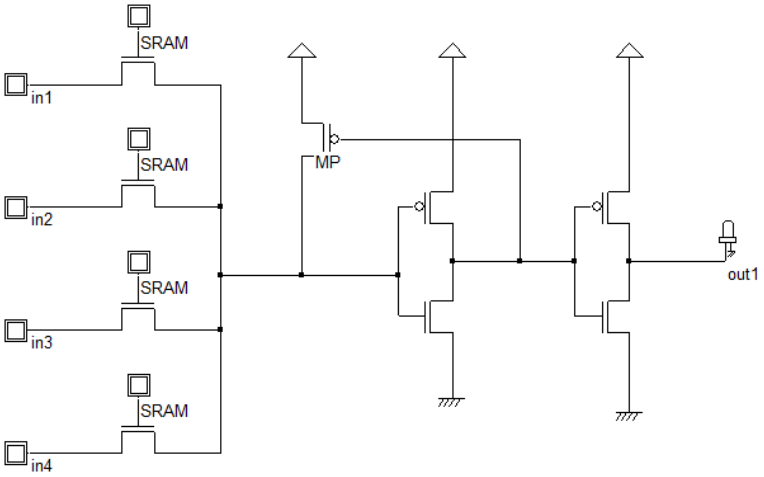

Figure 8: Leakage reduction technique

IV SLEEP LEAKAGE REDUCTION TECHNIQUE

We introduce sleep transistors into the pMOS network of CMOS logic gates where the SLEEP transistors are ON when the circuit is active and are turned OFF when the circuit in the sleep mode [5] [6]. Also it can be operated with Sleep mode Vs Low power mode. When Sleep = 1 and Low Power = 0, the circuit becomes sleep mode and both additional nMOS and pMOS transistors (MN and MP) are OFF. When Sleep = 0 and Low Power = 1, MP is OFF but MN is made ON which produces threshold drop since the other end is connected to V_{DD} rail. Here, V_{DD} becomes $V_{DD} - V_t$, so that the full logic voltage swing is reduced which helps for the reduction in power. This technique schematic is shown in Figure 9 and the timing diagram results are in Figure 10.

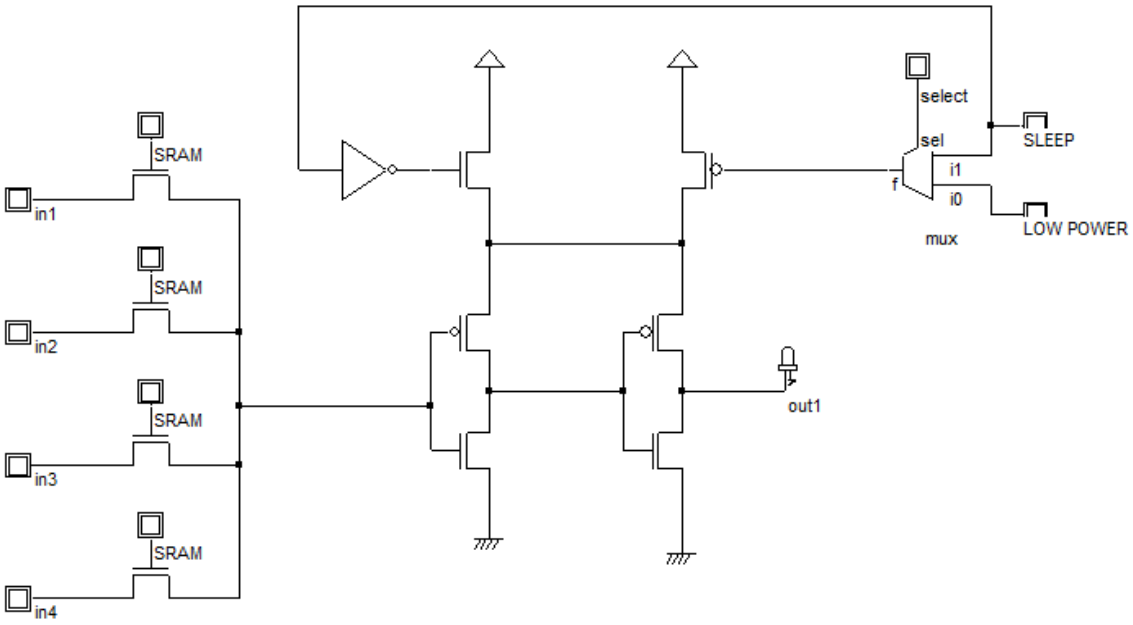

Figure 9: Sleep mechanism

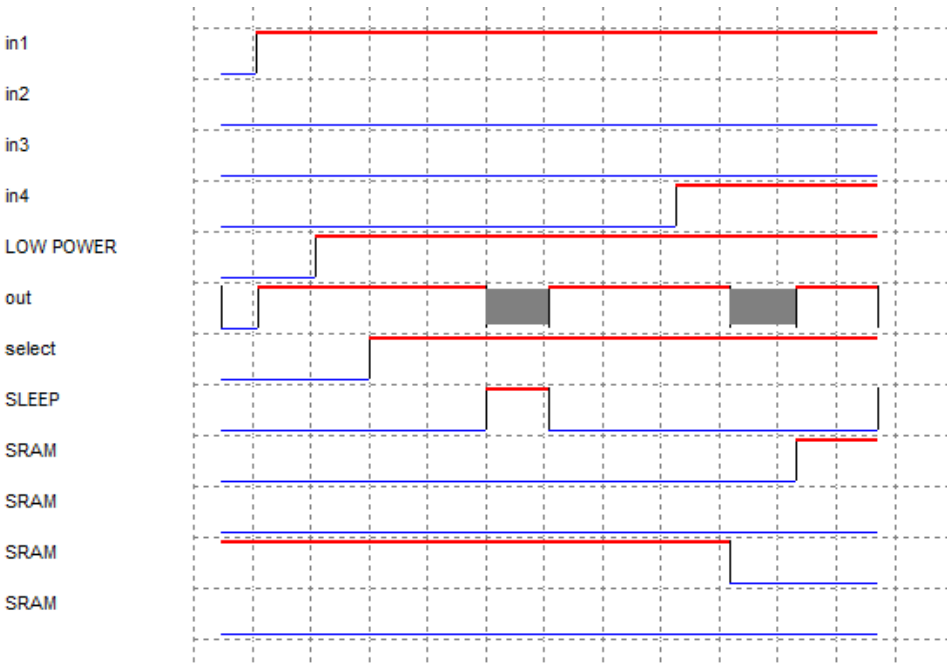

Figure 10: Simulation result using Sleep mechanism

V RESULTS AND DISCUSSION

a. Area and Power analysis of basic 2x2 crossbar switch

Using Microwind EDA tool, the layouts for each design are made and the area for the circuits are estimated. Also the power dissipation for each circuit is estimated and tabulated in Table 1 and Table 2. Routing switch

using pass-transistor logic offers less area (58 μm^2) wiith minimum power (1.882 µ-watts) at the cost of threshold loss problem. To avoid threshold loss problem, transmission-gate logic is implemented at the cost of more area (143.7 μm^2) with slightly more power. The corresponding layouts are shown in Figure 11, Figure 12 and Figure 13.

Table 1: 2x2 Crossbar Switch Result Analysis

Switch Designs	Layout		Power (µ watts)
	Area	No. of transistors	
Multiplexer	108.0 μm^2	6 nMOS 6 pMOS	1.117
Pass-Transistor Logic	58 μm^2	5 nMOS 1 pMOS	1.882
Transmission-Gate Logic	143.7 μm^2	5 nMOS 5 pMOS	2.295

Table 2: Leakage Power Reduction Techniques

Switch Designs	Layout		Power (µ watts)
	Area	No. of transistors	
4-input Routing Switch	154 μm^2	6 nMOS 3 pMOS	2.147
Sleep Vs Low-Power mechanism	258 μm^2	9 nMOS 6 pMOS	1.139

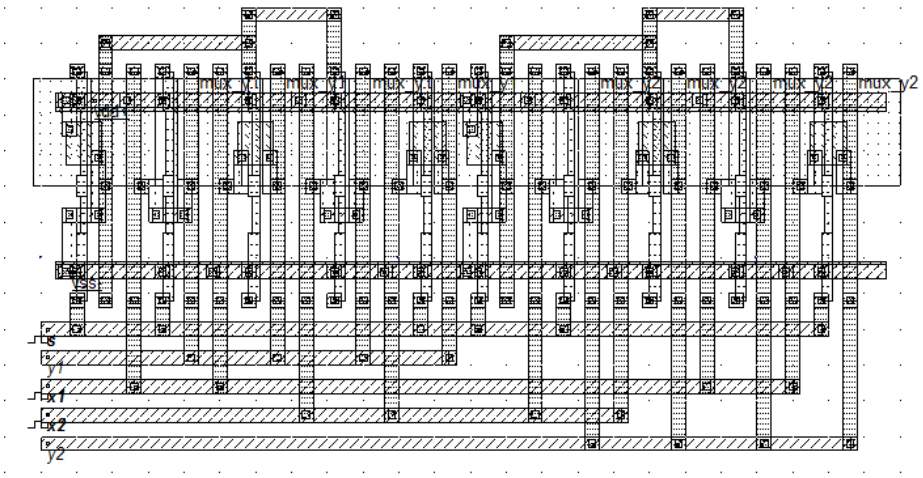

Figure 11: Layout of switch using multiplexer

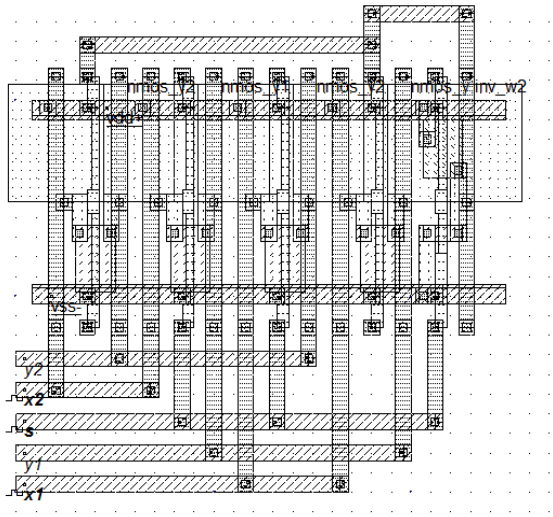

Figure 12: Layout of switch using pass-transistor logic

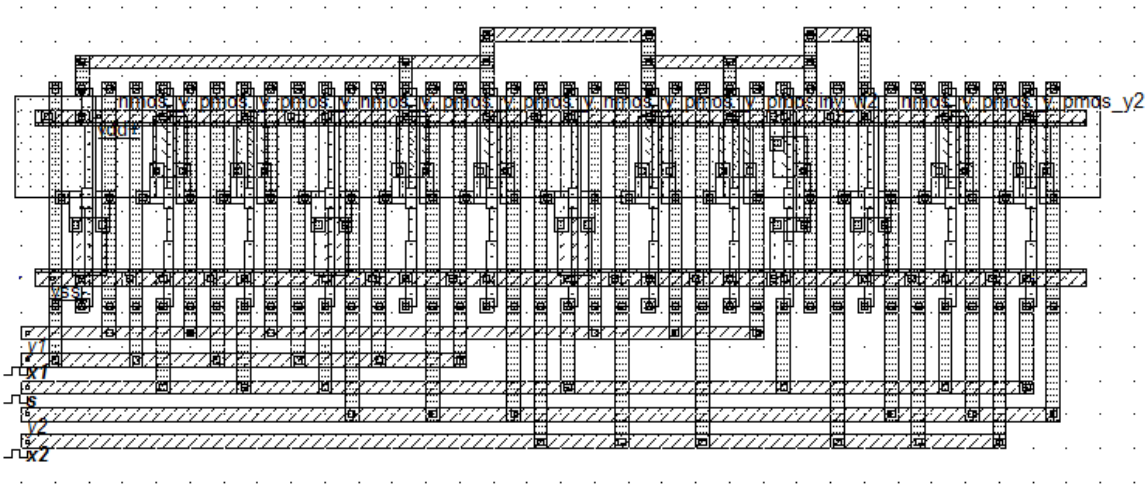

Figure 13: Layout of switch using transmission-gate logic

b. Area and Power analysis of 4-input routing switch

A 4-input routing switch multiplexer layout with leakage power reduction technique is shown in Figure 14. Even if the output at the multiplexer is V_{DD}-V_t, it doesn't make the pMOS transistor partially ON. Simulation results show that the Sleep Vs. Low-power approach is known as better technique which dissipates 1.139 µ-watts only. This is much reduced one compared to the previous design 2.147 µ-watts but the cost of more area (258 μm^2).

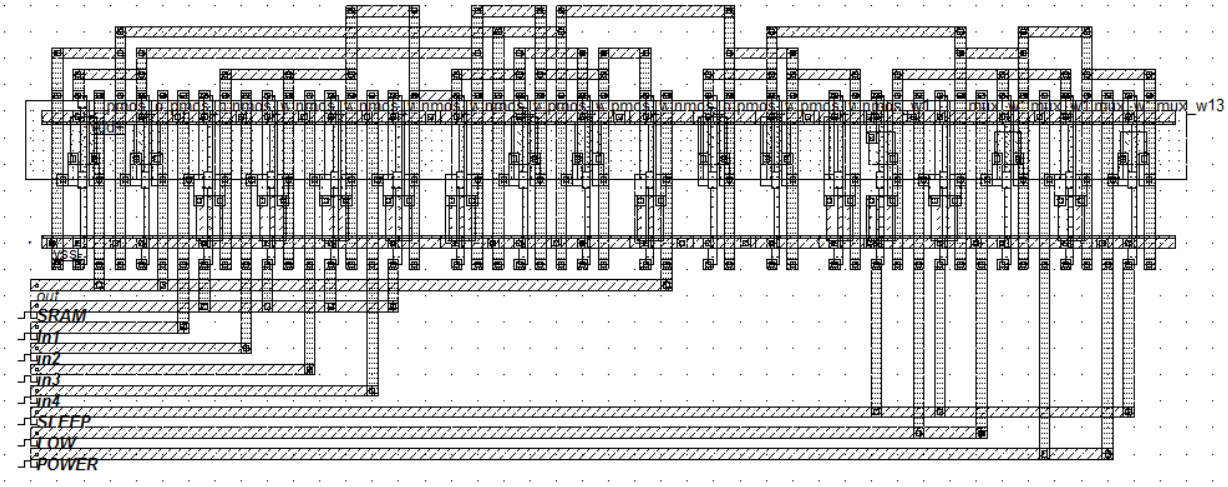

Figure 14: Layout of 4-input routing switch with low leakage power

VI CONCLUSION

Since low power design is more important and mandatory nowadays, these experiments help us to understand more about the design tricks for the switching architecture of FPGA. Because more activities are involved while implementing the prototype designs on FPGA, the area and the power are the primary constraints to improve the design and specifications. We understand the pass-transistor logic is good as far as the area is concerned but at the cost of performance issue. Also , the Sleep Vs. Low-power mode technique is quite more practical to reduce the leakage power involved in the design. In future, we may implement dynamic CMOS logic styles to the routing switch circuit designs with the detailed analysis of speed, area and power. Also, we may implement the designs to reduce the leakage power using methods like using multi-threshold CMOS design, Variable threshold CMOS designs and Adaptive body biasing, etc.

VII REFERENCES

[1] Zainalabedin Navabi , “Embedded Core Design with FPGAs”, Tata Mc-Graw Hill, pp.197-241, 2004.

[2] Michael Keating, David Flynm, Robert Aitken, Alan Gibbsons and Kaijian Shi , “Low Power Methodology Manual for System-on-Chip Design”, Springer publishers, pp.1-19, 2008.

[3] Gary K.Yeap, “Practical low power digital VLSI DESIGN”, Academic publishers, pp.1-22, 1998.

[4] Stephen Brown, Zvonko Vranesic, “Fundamentals of Digital Logic with VHDL Design”, Tata McGraw Hill, pp.315-377, 2005.

[5] Jason H.Anderson and Farid N.Najm , “A Novel Low-Power FPGA Routing Switch”, IEEE Custom Integrated Circuits Conference, pp.719-722, 2004.

[6] Anderson, J.H. and Najm, F.N. , “Low Power Programmable FPGA Routing Circuitry”, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 17(8): 1048-1060, 2009.

[7] Ejnioui A and Ranganathan, “Routing on switch matrix multi-FPGA systems”, Thirteenth International Conference on VLSI Design, pp.248-253, 2000.