A Design of Modified 64 bit Wallace Multiplier using 45 nm Technology

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Abstract—**Multipliers plays a vital role in the field of digital processing of information especially signal and image. The key benefit of 64 bit multiplier is high precision computation but it has to be faster as well. In this paper, we have designed a modified 64 bit Wallace multiplier. The designed multiplier reduces the number of half adders which are mainly used in the reduction phase of multiplier and also they do not contribute in the reduction of partial products. For the entire multiplication process we have used only 38 half adders. The multiplier is designed using Verilog-HDL and implemented using TSMC 45nm technology. It is found that the designed multiplier has reduced number of half adder in each stage and it consumes 15.22 mW at 166 MHz.**

Keywords - Fast multiplier, 64-bit multiplier, Low power design.

I. INTRODUCTION

The multiplier is one of the area, power and latency hungry hardware blocks. Very Large Instruction Word (VLIW) multipliers are common units in most of the high performance systems such as digital signal processors (DSP) and general purpose processors (GPU). The performance of multiplier unit influences overall performance of the DSP and GPU based systems. The 64 bit computation is to perform high precision computation at faster rate than other multipliers. It can process 64 bit data in one clock cycle.

Modified Wallace multiplier is similar like Wallace multiplier which some modification during the partial product formation. High speed Wallace multiplier [1] has three different stages in multiplication process. First stage is the formation of N x N product matrix, second stage is the reduction of the products matrix, the matrix is grouped into non overlapping group of three as shown in figure 1, one bit is just passed on to the next stage, two bits are given to the half adder and three bit are given to a full adder. This process continues till final output is of the height of two terms. The final output of the second stage is passed on to the third stage which contains carry propagation adder to generate the final output. The half adders that are used in during the second phase will help only in rearranging the bit and does not help in reduction of complexity of the multiplier.

The paper is organized as: The architecture of modified Wallace multiplier is explained in section II. The various implementations on 180nm, 90nm and 45nm were illustrated in section III. In section IV the concluding remarks were given.

II. MODIFIED WALLACE MULTIPLIER

Reduced complexity Wallace multiplier reduction [2] consists of three stages. First stage the N x N product matrix is formed and before the passing on to the second phase the product matrix is rearranged to take the shape of inverted pyramid. During the second phase the rearranged product matrix is grouped into non-overlapping group of three as shown in the figure 2, single bit and two bits in the group will be passed on to the next stage and three bits are given to a full adder. The number of rows in the in each stage of the reduction phase is calculated by the formula.

$$r_{i+1} = 2\left\lfloor \frac{r_i}{3} \right\rfloor + r_i \bmod 3 \qquad [1]$$

If the value calculated from the equation (1) for number of rows in each stage in the second phase and the number of row that are formed in each stage of the second phase does not match, only then the half adder will be used. The final product of the second stage will be in the height of two bits and passed on to the third stage. During the third stage the output of the second stage is given to the carry propagation adder to generate the final output.

Since the representation of 64 bit multiplication is infeasible we have represented the product matrix formation of two 9 bit numbers in figure 1. The inverted pyramid shape formation of the product matrix is shown in the figure 2.

								P19	P18	P17	P16	P15	P14	P13	P12	P11
							P29	P28	P27	P26	P25	P24	P23	P22	P21	
						P39	P38	P37	P36	P35	P34	P33	P32	P31		
					P49	P48	P47	P46	P45	P44	P43	P42	P41			
				P59	P58	P57	P56	P55	P54	P53	P52	P51				
			P69	P68	P67	P66	P65	P64	P63	P62	P61					
		P79	P78	P77	P76	P75	P74	P73	P72	P71						
	P89	P88	P87	P86	P85	P84	P83	P82	P81							
P99	P98	P97	P96	P95	P94	P93	P92	P91								

Figure 1: Product matrix formed by multiplying two 9 bit numbers

P99	P89	P79	P69	P59	P49	P39	P29	P19	P18	P17	P16	P15	P14	P13	P12	P11
	P98	P88	P78	P68	P58	P48	P38	P28	P27	P26	P25	P24	P23	P22	P21	
		P97	P87	P77	P67	P57	P47	P37	P36	P35	P34	P33	P32	P31		
			P96	P86	P76	P66	P56	P46	P45	P44	P43	P42	P41			
				P95	P85	P75	P65	P55	P54	P53	P52	P51				
					P94	P84	P74	P64	P63	P62	P61					
						P93	P83	P73	P72	P71						
							P92	P82	P81							
								P91								

Figure 2: Product matrix, rearranged as an inverted pyramid shaped.

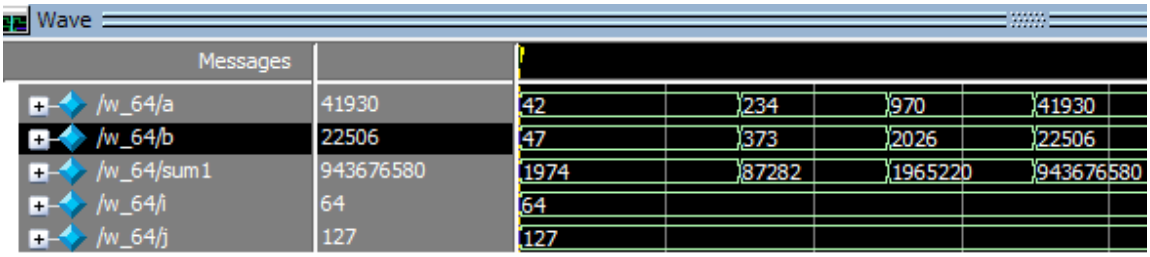

Figure 3: Simulation result of 64 bit modified Wallace multiplier

TABLE 1
Results of Power Dissipation, cells, Cell Area of 64 Bit Multiplier in three different Technologies

Technology	**Power dissipation in nW**			**No. of cells**	**Cell area (μm^2)**
	Leakage	**Dynamic**	**Total**		
180 nm	1414800	25591705	27006506	8682	452138
90 nm	1793420	58893801	60687222	27441	292942
45 nm	2402	9900772	9903175	12447	46596

III. RESULTS

The figure 4 shows the post routed 64 bit Modified Wallace multiplier in 45 nm technology. The total memory usage during Post-CTS (Clock Tree Synthesis) is 407 Mbytes and the total memory usage during Post-Route process is 456 Mbytes. The total path in both setup and hold mode is 128.The Density of the time design is 80.962%. The table 2 shows the values of power in mW used in 64 bit modified Wallace multiplier. So from the table we infer that 15.22 mW is utilized by the designed multiplier.

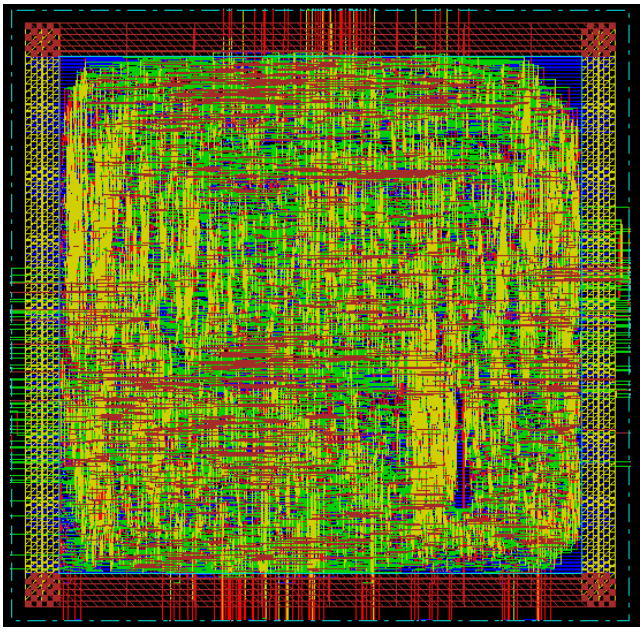

Figure 4: Post Routed 64 Bit Modified Wallace Multiplier in 45 nm Technology

TABLE II
Result of Total Power Consumed by 64 Bit Modified Wallace Multiplier in 45 nm Technology

	Values in mW	**Equivalent percentage (%)**
Total Internal Power	6.639	43.64
Total Switching Power	7.184	47.22
Total Leakage Power	1.392	9.147
Total Power	15.22	100

IV. CONCLUSION

The total number of half adders that are used in the reduction process of a 64-bit Wallace multiplier was reduced by 98%. The reduction of half adders in the multiplication causes reduction in the total power which is consumed by the multiplier. The multiplier was designed using Verilog-HDL and implemented using TSMC 45nm. The functional verification was done using Cadence IUS. Using Cadence Encounter RTL complier the power dissipation and area was calculated. Cadence Encounter tool was used to perform the Back End Process. The total design operates at a frequency of 166 MHz. Hence this design can be used for higher bit precision computation of multipliers in various digital applications.

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