New Low-Power and High-Speed 9T SRAM cell in Dynamic Domino Logic

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***Abstract*— This study presents the design of low power 9T SRAM cell using dynamic domino logic to achieve low power dissipation. The internal structure of the proposed 9T SRAM has cross coupled dynamic inverters which periodically updates the internal node voltage levels which, increase the read and write stability of the circuit. The SRAM design also has charge keeper transistor which resolves the problems in charge leakage so that the node voltages are not affected. The study investigates the impact of read/write delay, power dissipation, read stability, write-ability, and compares the results with that of standard 6T, 9T and 10T SRAM cell. The comparative study is based on Monte Carlo simulation to analyse the power improvements with its counterpart. The simulation results reveals appreciable improvement in read and write delay of about 54% with 67% of power consumption when compared to the existing 6T, 9T and 10T SRAM cell.**

Keyword- Read stability, Write stability, Static Noise Margin, Dynamic domino logic, Charge keeper

I. INTRODUCTION

LOW-POWER and high speed design has become a critical issue in the design of high performance SRAM cells. The design of SRAM cell reported in [1-20] has been implemented with Complementary Metal Oxide Semiconductor (CMOS) logic, Pass Transistor logic (PT) and Transmission Gate (TG) logic. The circuit designed using CMOS SRAM improves the driving capability but has undesirable delay time. The use of Pass Transistor Logic has many advantages over the CMOS design due the reduced transistor count and smaller node capacitances thus decreasing the required area, rise/fall times and power dissipation. However, this scheme suffers from leakage problems because the input inverter is not the full swing signal and it becomes worse when the supply voltage drops. While designing SRAM using TG has reduced driving capability as well as the logic requires true and complementary signals. To surrogate the problems associated with CMOS, PT and TG, this proposed SRAM cell incorporates dynamic domino logic to improve delay and power performance.

A number of SRAM cell topologies have been reported in the past decade [1-14]. Among these topologies, resistive-load four-transistor (4T) cell, load-less 4T cell and six-transistor (6T to 10T) SRAM cell have received attention in practice, owing to their symmetry in storing logic “one” and logic “zero”. The 4T [1] SRAM cell uses resistors as load devices in an NMOS circuit. This topology yields a smaller area and allow higher packing density, but requires an additional polysilicon layer and masking step to be added to the fabrication process. Additionally the large value of resistors (typically greater than 5 GΩ) has to implant in the circuit design. This leads to several changes in the electrical characteristics and has poor stability at low voltage. In a conventional 6T [2-3] SRAM cell, the data stored in the cell is distributed because of voltage division between the cross coupled inverters and the access transistors during a read operation. The data is most susceptible to external noise during this inherent disturbance produced by the direct-data-read-access mechanism of a standard 6T SRAM cell. This fact means that the device dimensions and threshold voltage targets established for the SRAM devices are a compromise by design. An improved version of 6T cell is reported in [4-6], which utilizes 8T to enhance the noise tolerance and suitable for low-voltage and high – speed applications. The additional transistors in 8T could lead to increase in area as well as metal density for additional read and write lines. Still the circuit suffers from stability problems. To surmount this adverse effect a modified 9T cell has been reported in [7-8] which incorporates two separate accesses transistor for read and write operation. To avoid the charge leakage problem the aspect ratio of the transistors were made high.

The organization of the paper is as follows: The section II, describes the existing 6T, 8T and 9T SRAM cell. Section III, presents the proposed 9T SRAM in dynamic domino logic. Section IV presents the simulation results under various supply voltages. Section V presents the discussion. Finally the conclusion is presented in section VI.

II. EXISTING SRAM CELLS

The schematic diagram of 6T SRAM cell is shown in Fig1a. During read, the WL voltage is raised, and the memory cell discharges either BL (bit line true) or BLB (bit line complement), depending on the stored data on nodes Q and QB. A sense amplifier converts the differential signal to a logic-level output. Then, at the end of the read cycle, the BLs returns to the positive supply rail. During write, WL is raised and the BLs are forced to either VDD (depending on the data), overpowering the contents of the memory cell. During hold, WL is held low and the BLs are left floating or driven to VDD.

To address the reduced read SNM problem, the read and write operations are separated by adding read access structures to the original 6T cell, thus increasing the transistor count to 8. Fig 1b shows the schematic design of an 8T SRAM cell. The transistor configuration (i.e. M1 through M6) is identical to a conventional 6T SRAM cell. Write access to the cell occurs through the write access transistors and from the write bit lines, BL and BBl. Read access to the cell is through the read access transistor and controlled by the read word line, RWL .The read bit line, RBL is recharged prior to the read access.

A 9T SRAM cell enhances the data stability and reduces leakage power consumption. The schematic of the 9T SRAM cell is shown in Fig 1c. The upper sub-circuit of the new memory cell is essentially a 6T SRAM cell with minimum sized devices (composed of N1, N2, N3, N4, P1, and P2 with W = Wmin and L = Lmin). The two write access transistors (N3 and N4) are controlled by a write signal (WL). The data is stored within this upper memory sub-circuit. The lower sub-circuit of the new cell is composed of the bit-line access transistors (N5 and N6) and the read access transistor (N7).

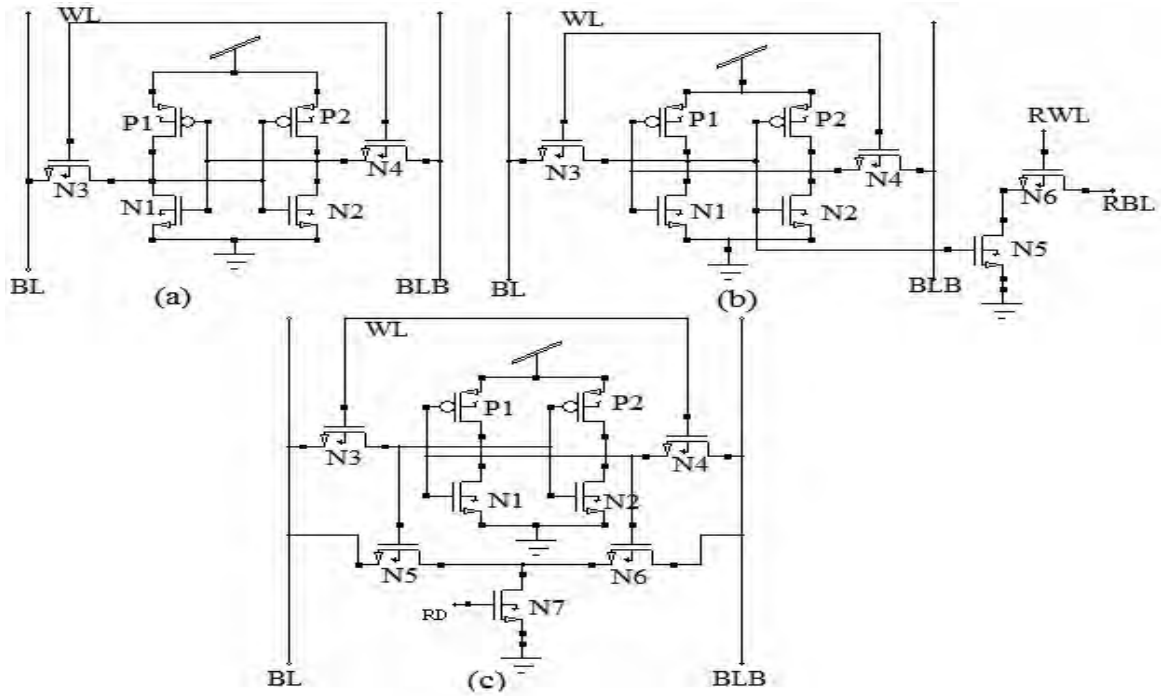

Fig 1. Existing SRAM Cell. a)6T SRAM b)8T SRAM c)9T SRAM

III. PROPOSED 9T SRAM CELL IN DYNAMIC DOMINO LOGIC

The proposed 9T SRAM cell is depicted in Fig 2 has nine transistor (N1, N2,N3,N4,N5,N6,N7,P1,P2). The proposed 9T memory cell has been implemented with two cascade dynamic inverters (P1, N1, N2, P3, N4 and N3) which operate at different clock rates. These dynamic inverters provide the storage of logical values. The transistors N5, N6 act as the access transistor for controlling word line signal for read and write operations. The access transistors N5 and N6 are controlled by the word line signal BL and BLB that defines the operational modes. These access transistors connect the bit line to store the value of node A and B. The transistor P2 acts as a keeper to avoid charge sharing problem and to maintain the stability of the circuit. The transconductance of keeper transistor β_{KP} should be twice in order to maintain the stable data as well as from noise susceptibility. The operations of this proposed SRAM cell during read/ write and hold state is reported in the functional Table 1.

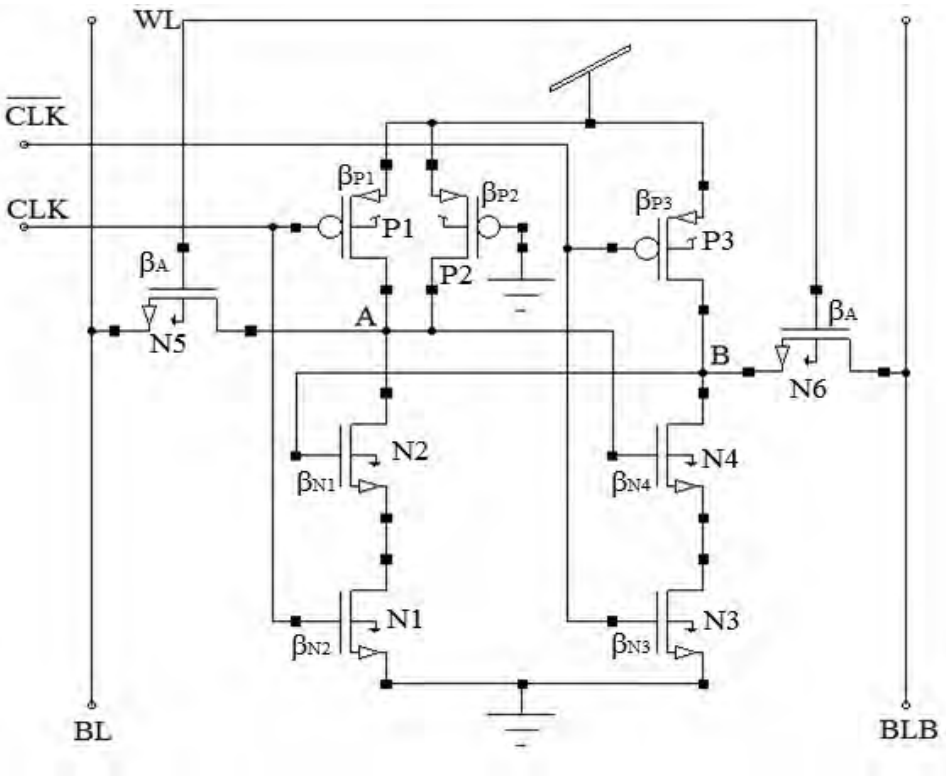

Fig 2. Proposed Low-power 9T SRAM Cell

A. READ Operation:

During read operation both BL and BLB is made high. To read logic '0' node A is grounded so that the transistors N1and N2 will be in ON state there by the voltage is discharge through access transistor N5 via N1 and N2. During this time node B is high which makes transistor N3 and N4 ON there by charges the access transistor N6.Now the sense amplifier detect the logical levels of BL and BLB. If BL is discharge then the data read is '0'. Similarly to read logic '1' node B is grounded so that the transistors N3 and N4 will be in ON state there by the voltage is discharged through the access transistor N6 via N3 and N4. During this time node A is high which makes the transistor N1 and N2 OFF there by charges the access transistor N5. If sensed output for BL is high the data read is logic '1'.

For read stability the aspect ratio of the transistors N1and N2 should be larger than N5. The aspect ratio of pull down network of transistor β_N (N1andN2) to access transistor β_A is called pull down ratio PD.

$$\text{Pull down ratio (PD)} = \frac{\beta N}{\beta A} \qquad (1)$$

Where β_N = transconductance of pull down NMOS (N1 and N2)

β_A = transconductance of access transistor (N5)

$\beta = K` \frac{W}{L}$, $\quad K` = \mu\, Cox$

This parameter PD defines the read stability of the SRAM cell. In this proposed 9T SRAM the transconductance ratio of ($\beta_N/\beta_A>1$) is made greater than 1.

B. WRITE Operation

During write operation BL and BLB should be complementary to each other. To write logic '0' the preliminary condition has to check. If previously stored value is '1' the status of node A is high and node B is Low. Therefore to write logic '0' force node B to high thereby the node voltage at A will be discharged through N1 and N2. Similarly to write logic '1', check the previously stored values of node A and B. If previously stored value is '0' the status of node A is low and node B is high. Therefore to write logic '1' force node A to high thereby the node voltage at B will be discharged through BLB.

For write stability the aspect ratio of the transistors P3 should be lesser than N6. The aspect ratio of pull up network of transistor β_P (P3) to access transistor β_A (N6) is called pull up ratio PU.

$$\text{Pull up ratio (PU)} = \frac{\beta P}{\beta A} \qquad (2)$$

Where β_p = transconductance of pull up PMOS (P3)

β_A = transconductance of access transistor (N6)

$\beta = K` \frac{W}{L}$, $K` = \mu Cox$

This parameter PU defines the write stability of the SRAM cell. In this proposed 9T SRAM the transconductance ratio of ($\beta_P/\beta_A<1$) is made lesser than 1.

C. HOLD State

To hold the data in the cell, make BL and BLB inactive and the word line signal WL is kept low thereby the access transistor N5 and N6 will be in cut off region which results in isolation of bit line and cell. Stability of the hold state depends upon the two cascaded dynamic inverter feed back into the input with different clock and the inverter ratio (βN/βP) establishes the midpoint voltage for each dynamic inverter.

TABLE I
Functional Table for the proposed 9T SRAM Cell

Operation	Bitline state	Node condition	Bit line operation
Read '0'	BL & BLB= High WL= High	A=0, B=1	BL -> Discharging ,BLB->charge
Read '1'	BL & BLB= High WL= High	A=1, B=0	BL -> charge, BLB-> Discharging
Write '0'	BL =true, BLB= complementary WL= High	If previous value is '1' A=1, B=0	B is force to charge from BLB
Write '1'	BL =true, BLB= complementary WL= High	If previous value is '0' A=0, B=1	A is force to discharge from BLB
Hold	WL= Low	Hold the previous value A & B	_

IV. SIMULATION RESULTS

The proposed 9T SRAM cell is simulated using Tanner EDA with BSIM3v3 250nm technology with supply voltage ranging from 1V to 5V in steps of 0.5V. The simulation setup for the proposed 9T SRAM cell is shown in Fig. 3. The circuit is simulated with a 100MHz clock frequency. Since the operation of proposed SRAM is based on dynamic logic characteristics, the input should be change in precharge phase and the results are obtained during evaluation phase. The delay parameter is calculated from all the transitions from an input combination to another, and the delay at each transition has been measured from the time that clock signal reaches 50% of the supply level. The reference circuits that are compared with the proposed SRAM (a) 6T [2-3], (b) 8T [4-6], (c) 9T [7-8]. The simulated wave for read and write operations are shown in Fig. 4 and 5. The transconductance ratio of access transistor β_A, where as β_{N1}, β_{N2}, β_{P1} and β_{P3} are the transconductance ratio of cross coupled dynamic inverter and βP2 is the conductance of keeper PMOS transistor.

$\beta_A = K` \frac{2.50\mu}{0.25\mu}$, $\beta_{N1} = \beta_{N2} = K` \frac{5.00\mu}{0.25\mu}$, $\beta_{N3} = \beta_{N4} = K` \frac{2.50\mu}{0.125\mu}$, $\beta_{P1} = K` \frac{2.50\mu}{0.25\mu}$, $\beta_{P2} = K` \frac{2.50\mu}{0.125\mu}$, $\beta_{P3} = K` \frac{1.50\mu}{0.625\mu}$

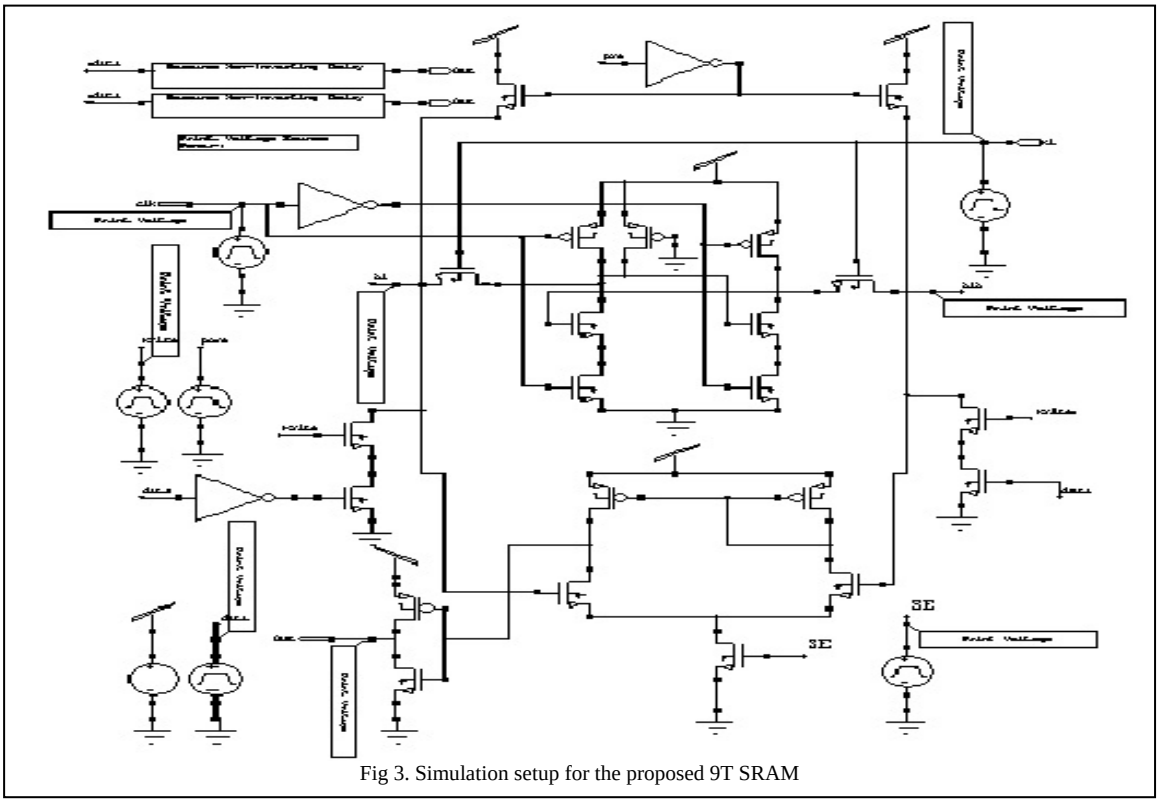

Fig 3. Simulation setup for the proposed 9T SRAM

For read operation the clock operates in precharge and evaluation phase. During precharge the sense enable (SE) and word line signal (WL) is made high. During precharge phase the bit line signals BL and BLB are high. In the evaluation phase depending on the read value either 0 or 1 the corresponding bit lines are high and low respectively. The status of write enable (WR) is low for both precharge and evaluation mode. To have data stability the inputs are not changed during evaluation phase. The read operation is shown in Fig. 4.

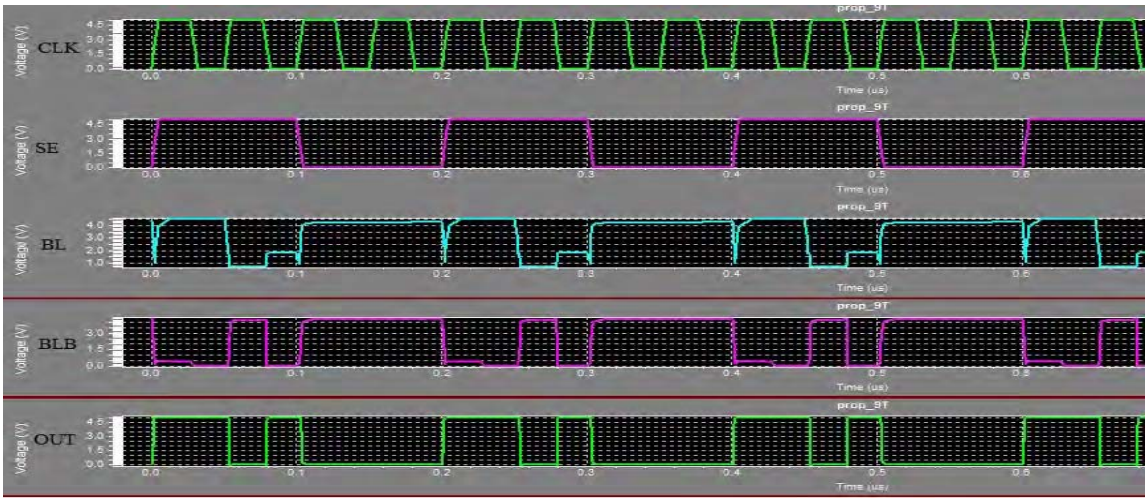

Fig 4. Waveform of Read operation

Similarly for write operation the clock operates in precharge and evaluation phase. During precharge the sense enable (SE) is made low and word line signal (WL) is made high. During precharge phase the bit line signals BL and BLB are complementary to each other. In the evaluation phase depending on the write value either 0 or 1 the corresponding bit lines are high and low respectively. The status of write enable (WR) is high for both precharge and evaluation mode. To have data stability the inputs are not changed during evaluation phase. The write operation is shown in Fig. 5.

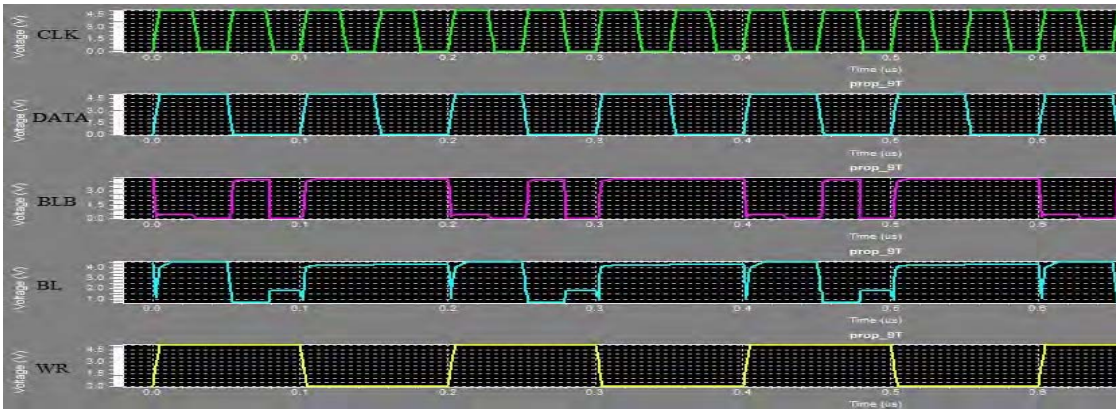

Fig 5. Waveform of Write operation

The proposed 9T SRAM along with the existing SRAM cells are simulated with the same setup and in same input voltages. Table 2 provides the rise time, fall time, read delay and write delay with various voltages ranges from 1.2V to 5V between proposed and its counterpart.

TABLE II
Delay performance of proposed 9T SRAM with existing SRAM

SRAM Cell	Voltage	Delay			
		RiseTime	FallTime	Read delay	Write delay
6T	1.2V	7.9462e-011	4.9486e-010	5.0379e-008	2.5238e-008
	2.5V	6.3217e-011	2.6274e-010	5.0370e-008	2.5386e-008
	3V	6.2365e-011	2.3271e-010	5.0368e-008	2.5553e-008
	3.3V	6.1872e-011	2.1694e-010	5.0366e-008	2.5664e-008
	4.2V	6.1741e-011	2.4170e-010	5.0359e-008	4.9149e-008
	5V	7.5929e-011	8.3941e-010	5.0350e-008	4.9504e-008
8T	1.2V	8.3427e-011	4.9447e-010	5.0363e-008	2.5212e-008
	2.5V	6.5840e-011	2.6142e-010	5.0356e-008	2.5386e-008
	3V	6.2278e-011	2.3300e-010	5.0354e-008	2.5553e-008
	3.3V	6.0156e-011	2.1688e-010	5.0352e-008	2.5664e-008
	4.2V	6.5023e-011	2.4219e-010	5.0345e-008	4.9145e-008
	5V	8.1594e-011	8.4161e-010	5.0336e-008	4.9505e-008
9T	1.2V	3.6036e-010	8.5933e-011	2.6345e-008	2.5117e-008
	2.5V	7.5076e-010	5.8068e-011	2.6230e-008	2.5058e-008
	3V	9.0091e-010	5.6948e-011	2.6185e-008	2.5049e-008
	3.3V	9.9100e-010	5.6522e-011	2.6158e-008	2.5051e-008
	4.2V	1.2185e-009	7.8555e-011	2.6078e-008	2.5783e-008
	5V	1.3837e-009	2.3848e-010	2.6006e-008	2.4962e-008
Prop 9T	1.2V	6.8192e-010	1.4002e-010	1.4292e-009	4.5324e-009
	2.5V	1.1581e-009	1.1604e-010	1.7248e-009	4.3702e-009
	3V	1.1760e-009	1.1487e-010	1.6090e-009	4.2306e-009
	3.3V	1.1867e-009	1.1629e-010	2.1109e-009	4.0140e-009
	4.2V	1.2190e-009	1.3706e-010	2.7475e-009	3.2412e-009
	5V	1.3310e-009	2.6277e-010	2.9027e-009	2.5411e-009

The power is analysed for read and write operation for all the complete transition and its variation is reported in Table 3. The power consumption reported for various voltages from 1.2V to 5V for the proposed and its existing SRAM cells.

TABLE III
Power consumption of proposed 9T SRAM with existing SRAM

SRAM Cell	Power Consumption (µw)					
	5V	4.2V	3.3V	3V	2.5V	1.2V
6T	192.74	192.05	191.36	192.05	192.05	191.36
8T	190.74	190.98	192.65	190.14	191.82	190.14
9T	193.62	192.84	193.53	192.84	192.15	192.84
Prop 9T	189.74	188.93	188.94	188.98	188.93	188.14

performs better than its existing counterparts in terms of power, read and write delay. Fig. 6 shows the power consumption of proposed and existing SRAM cells. From this graph it can be observed that nearly 72% of improvement in power consumption with 6T, nearly 65% improvement with 8T and 86% with existing 9T. Fig 7 shows the performance of read/write delay for proposed and existing SRAM cells at 5V. From this graph it is noticed that for CMOS cells reported in [1-15] the read/write delay are higher when compared to dynamic domino logic. Nearly 45% of read/write delay can be enhanced through the proposed 9T SRAM cell.

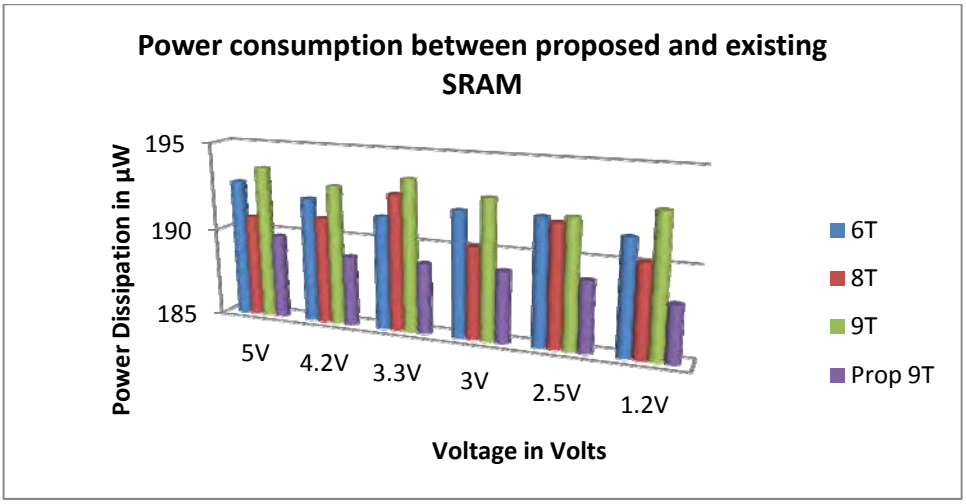

Fig 6. Power Comparison between proposed and existing SRAM cell

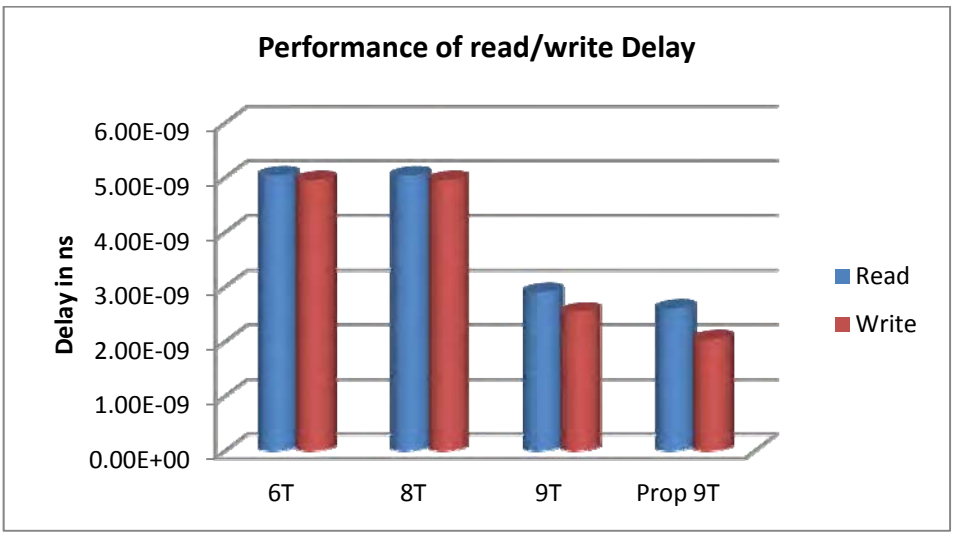

Fig 7. Performance of read/write delay for proposed and existing SRAM cell

VI. CONCLUSION

A new Low-power and High-speed 9T SRAM cell using dynamic domino logic has been presented. The performance of this proposed SRAM cell presents an overall 67% of power reduction when compared to other SRAM cells with slight increase in transistor count. The write/delay factor has been improved over 54% when compare to its counterpart. The primary advantage of this proposed SRAM cell, it exhibits low power and high speed due the dynamic domino logic and provides more read and write stability because of periodic updates in the internal node.

Appendix A

Device Specification for the proposed 9T SRAM cell

.LIB TT_PMOS_PARAMETERS
.PARAM TOxP=5nm
.PARAM dVthP=0
.PARAM CjP=1.9E-3
.PARAM CjswP=3.8E-10
TOX = 5.6E-9
+U0 = 100
+CGDO = 5.59E-10 CGSO = 5.59E-10 CGBO = 5E-10
+CJ = 1.857995E-3 PB = 0.9771691 MJ = 0.4686434
+CJSW = 3.426642E-10 PBSW = 0.871788 MJSW = 0.3314778
+CJSWG = 2.5E-10 PBSWG = 0.871788 MJSWG = 0.3314778
+CF = 0 PVTH0 = 4.137981E-3 PRDSW = 7.2931065
.ENDL TT_PMOS_PARAMETERS
.LIB TT_NMOS_PARAMETERS
.PARAM TOxN=5nm
.PARAM dVthN=0
.PARAM CjN=1.9E-3
.PARAM CjswN=4.4E-10
TOX = 5.6E-9
U0 = 284.0529492
CGDO = 4.65E-10 CGSO = 4.65E-10 CGBO = 5E-10
+CJ = 1.698946E-3 PB = 0.99 MJ = 0.450283
+CJSW = 3.872151E-10 PBSW = 0.8211413 MJSW = 0.2881135
+CJSWG = 3.29E-10 PBSWG = 0.8211413 MJSWG = 0.2881135
.ENDL TT_NMOS_PARAMETERS

Output of Transient Response:

Time<s> v(write)<V> v(data)<V> v(wl)<V> v(pre)<V> v(Z)<V> v(clk)<V> v(blb)<V> v(X)<V> v(bl)<V>

0.000000e+000 0.0000e+000 0.0000e+000 0.0000e+000 0.0000e+000 5.0000e+000 0.0000e+000 4.3465e+000 1.7230e-007 4.3478e+000

2.500000e-009 2.5000e+000 2.5000e+000 2.5000e+000 2.5000e+000 4.5913e+000 2.5000e+000 7.4030e-001 7.1616e-001 1.1163e+000

2.843452e-009 2.8435e+000 2.8435e+000 2.8435e+000 2.8435e+000 4.1359e+000 2.8435e+000 8.2908e-001 2.2357e+000 1.6395e+000

2.941425e-009 2.9414e+000 2.9414e+000 2.9414e+000 2.9414e+000 3.8218e+000 2.9414e+000 9.2423e-001 3.1506e+000 1.9830e+000

2.990412e-009 2.9904e+000 2.9904e+000 2.9904e+000 2.9904e+000 3.6134e+000 2.9904e+000 9.3931e-001 3.4449e+000 2.0754e+000

3.074697e-009 3.0747e+000 3.0747e+000 3.0747e+000 3.0747e+000 3.3986e+000 3.0747e+000 9.7741e-001 3.5103e+000 2.1651e+000

3.248540e-009 3.2485e+000 3.2485e+000 3.2485e+000 3.2485e+000 3.3280e+000 3.2485e+000 1.0373e+000 3.3906e+000 2.3410e+000

3.548559e-009 3.5486e+000 3.5486e+000 3.5486e+000 3.5486e+000 3.2948e+000 3.5486e+000 1.1492e+000 3.1813e+000 2.6156e+000

4.011521e-009 4.0115e+000 4.0115e+000 4.0115e+000 4.0115e+000 3.2813e+000 4.0115e+000 1.3219e+000 2.8685e+000 3.0233e+000

4.635043e-009 4.6350e+000 4.6350e+000 4.6350e+000 4.6350e+000 3.4563e+000 4.6350e+000 1.5289e+000 2.5268e+000 3.4463e+000

4.946805e-009 4.9468e+000 4.9468e+000 4.9468e+000 4.9468e+000 3.5453e+000 4.9468e+000 1.5766e+000 2.4615e+000 3.5488e+000

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