IMPLEMENTATION OF X-FACTOR CIRCUITRY IN DECOMPRESSOR ARCHITECTURE

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Abstract- VLSI testing majorly concern with test time and power consumed during testing process. This paper presents efficient Decompressor architecture for low power test applications. The aim of the paper is to reduce the transition count of shift-in test pattern which reduces the power. X-factor circuitry, the concept adopt on the decompressor architecture in efficient way to improve performance of testing. The X-factor circuitry Decompressor design captured in VerilogHDL that targeted to TSMC 0.25 micron CMOS technology and results are analyzed.

Keywords: Decompressor, X-factor circuitry, Shift-in test pattern.

I. INTRODUCTION

VLSI design and testing application have tradeoff on three prime factors: Area, Power and Speed. Testing the design requires additional logic in the silicon to check the Faults which may occur during the hardware development process. DFT is based on ATPG and standard scan gained large acceptance as a dependable method certain high test coverage. The development of test generation and scan placing is automatic and provides assurances quality of results and very high predictability. The Number of fault models and coverage's can be detected by using generated test sets of Conventional ATPG systems. While detecting Faults in ATPG it will depends on scan cells, but only few cells are quantified. Random values are placed in remaining places. Extra faults are detected by indicated patterns; these are placed on a tester. Preponderance of present test compression methods, together with the LFSR coding proceeds gain of low test cube fill rates. Reduce cost related through testing complex circuit. The design circuit that it will be easier to test. Scan patterns and scan cells directly proportional to volume of test data. The test compaction, that is reduce the number of test patterns by merging compatible patterns and compression are reduce the data volume through coding and architectural approaches. The decompressor architecture is to find out the number of common and conflicts in n-number of test pattern. The proposed technique to implement the Decompressor architecture with X-filling concept.

II. RELATED WORK

Embedded Deterministic test is based on standard scan methodology. Embedded means high fault coverage, arbitrary fault models and minimum number of patterns. Deterministic, it is simple, more complex, unlimited numbers of the scan chains and short scan load time [1]. Existing methods that develops a decompressor architecture that presented the Test data and biasing logic. The biasing logic contains 3 AND gates. Gates are used for best tradeoff between the switching activities [2]. This is done during the compression and scan shift-in. To Developing this architecture requires additional space along with core, so we going for proposed technique. Embedded deterministic test (EDT) also called as Test-data volume compression [7]. EDT mitigates manufacturing test charge by providing the individuals of two instructions, which diminish the size, scan test time and data value. In paper [4] implementation can reduces data volume and time by division of several scan chains in same vector [6]. This paper deals for any fault model this compressed test patterns suited, and it is cost effective. The procedure of novel test data volume compression (EDT) generally contributes test stimulated compression manner [3]. So distribute test data sets to decompressor in continuous on chip flow. The existing method ATPG has broadly acceptable and reliable methodology that provides test coverage in paper [8]. The shadow *register* is to be used in paper [5] and to save the current state. Shadow registers are used for the need of modify the read only registers; they help the programmer to keep track of what is written to write only registers. Next one important thing is to implement the hold register in [2]; it can hold current data or load new data. Different types of X- filling method was proposed in paper [9], this methods to reduce the transition count and low power. A capture power-aware test compression method is safe limit over capture power by compromising test compression ratio [10]

The decompressor input is directly coupled with the ATE channel is completed through routing logic controller by the first bit of every test pattern. The decompressor architecture consists of three blocks that is parent pattern, control pattern and incremental pattern. The first block is parent pattern with the ring generator1 and x-filling based on XOR network. The second block is control pattern; the control pattern is driven by the ring generator1. The hold register is located among the ring generator1 and phase shifter3, the hold register is to maintain the decompressor outputs unaffected. When the hold register is load enable the corresponding values shifted into the phase shifter3 otherwise it is waiting for new value. If HOLD is set to 1, the content of ring generator 1 reloads the hold register. This operation done before the action of feeding new seed variable to ring generator1.The control pattern is to select the output of the decompressor architecture. The last block is incremental block, this block consist of ring generator2, phase shifter3. The Incremental pattern decoding is done by these parts of decompressor architecture. Incremental pattern features particularly sparse particular bits and it is does not necessary for each and every one variables.

The decompressor input test patterns are directly connected with the ATE channels. The EDT update signal is to be indicating the each and every test pattern of MSB first bit. The EDT update bit is suppose 1 means the parent pattern will select otherwise the incremental pattern will select. Suppose the incremental pattern was selected means the first bit of test pattern values to store in the register. Since the parent pattern was selected the first bit of the test pattern is to store in register and the multiplexer is to place between the decompressor decoder and register. The first mux becoming output is to store in register after three clock pulse only the another multiplexer to operate otherwise the initial values to be circulate and the output of multiplexer and register is depends on the ring generator inputs. ATE is a traditional methodology of passing the test pattern (parent pattern) to scan chain through round buffer for every chip. For BIST concept output of the multiplexer stored.

III. PROPOSED METHOD

X-factor circuitry method will fill defined logic instead of all in-determinant ‘X’ rendering of values present in their neighboring scan element due to of power reduction in shift-in process, which is commonly called as adjacent fill. Filling of one x-bit in test pattern which causes too hefty in test responses which in turn determine the defined logic. In X-filling, the test cubes for industrial contains 97% of X-bits, which are represented by logic values, to increase the fault coverage of circuit under test. For improving fault coverage and power efficiency following algorithm has been implemented in decompressor architecture.

The Pattern generator from ring generator is given to X-factor circuitry. These X-factor circuitry involves two basic function one is filling X-bits with defined logic. The X-filling concept works the flow chart show in fig 1. At first note the generated pattern and position the X-bits, using the concept of Shift-in Transition Probability (SiTP). Calculate SiTP for possible logic and compare the values. If $SiTP_i(1)$ is greater than $SiTP_i(0)$ then the X-bits filled with logic 0, if $SiTP_i(1)$ is lesser than $SiTP_i(0)$ then the X-bits filled with logic 1 and repeat the same process for other X- bits in the pattern.

The filled pattern has undergone the secondary process of X-factor circuitry, i.e. XOR network. The XOR network generates the pattern which required of Parent, Incremental and Control. This detected pattern has less transition compare to the existing decompressor architecture so that the power due to switching of pattern during shift-in process reduced effectively to the scan chain. Modified decompression architecture is shown in fig 2.

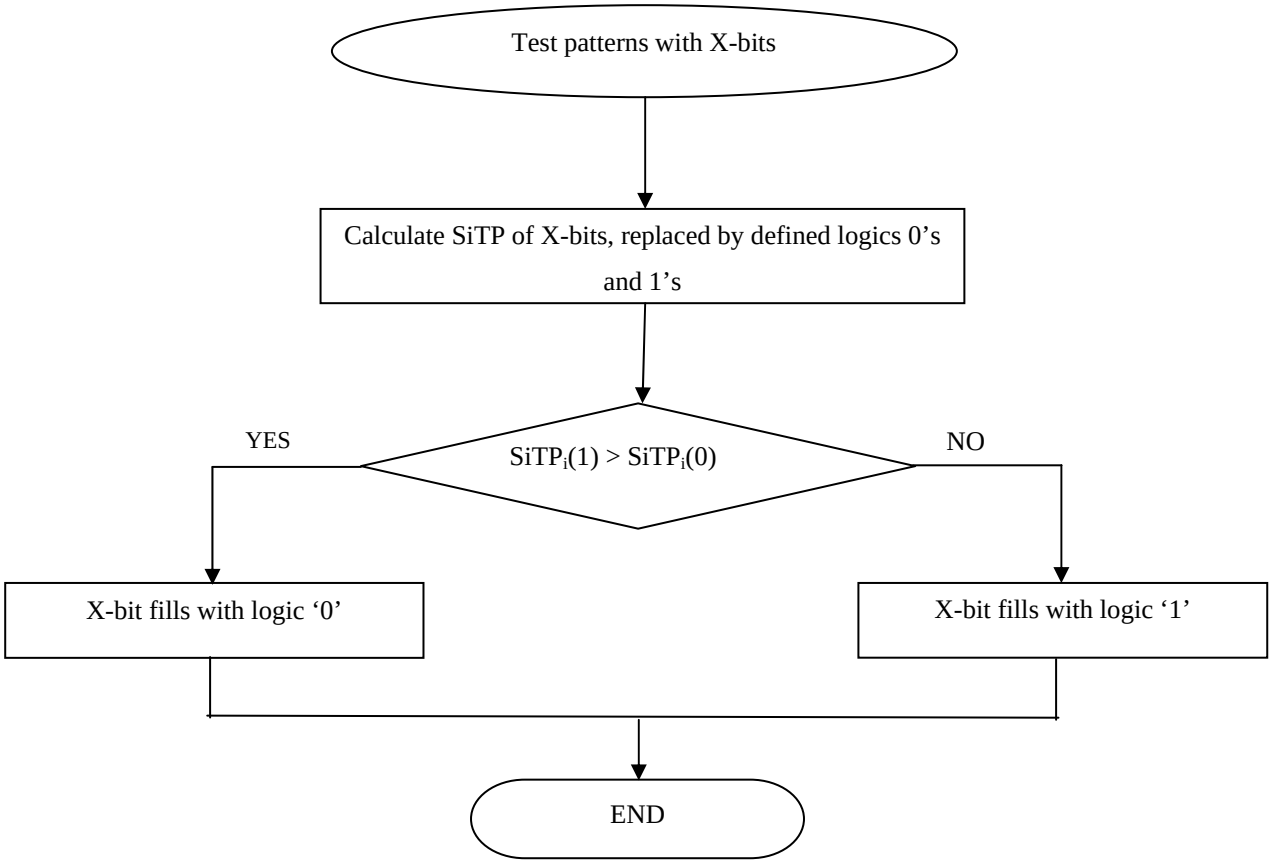

Fig 1: Flow chart for X- filling

IV. EXPERIMENTAL RESULTS

In order to analysis of decompressor architecture and modified decompressor architecture results are verified on cadence RTL compiler using library TMSC 0.25 microns. Fig 3. Shows the proposed method RTL view. The experimental results are tabulated given below in Table 1, this tabulation consist of power, delay and Area. The proposed technique reduces the transition count and power. The Fig.4 shows the comparison chart of existing and proposed technique, the comparison chart based on the 8-bits test pattern differences. These chart comparisons between X-filling with 0, X-filling with 1 and shift-in test probability.

Table 1: Comparison of parameter Analysis

Instance	Power	Delay	Area
Existing	27076660.43nW	1274.9	28134
Proposed	26597930.51nW	1265.2	27414

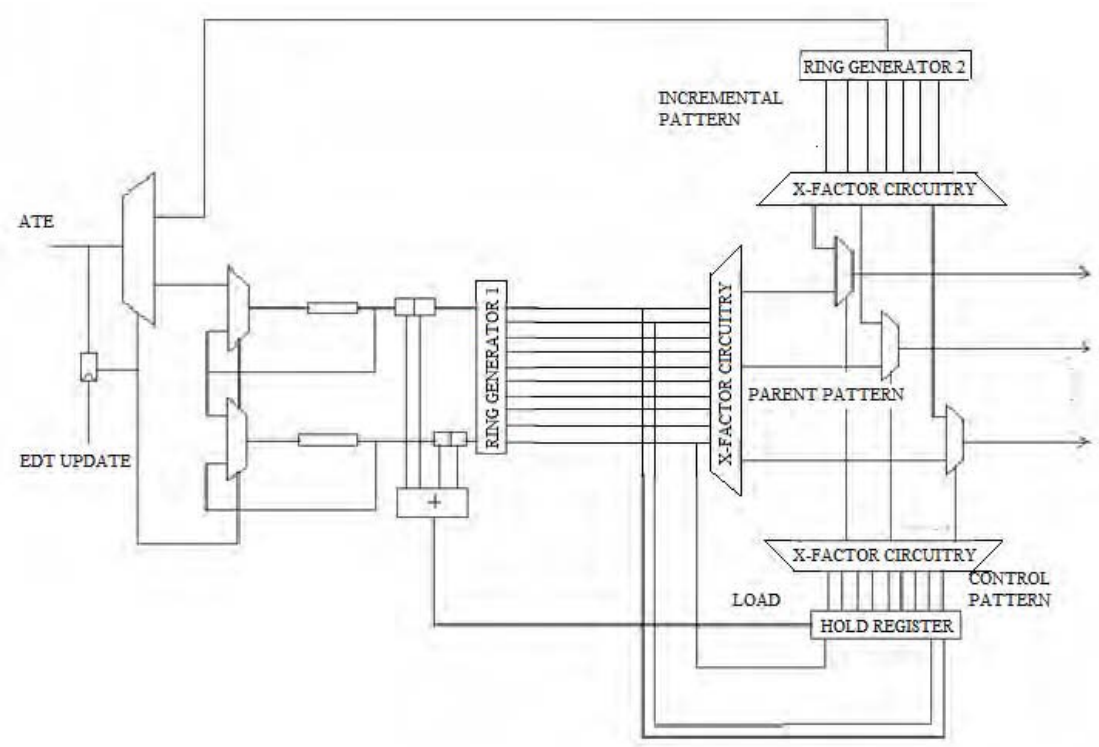

Fig 2: Modified Decompressor Architecture

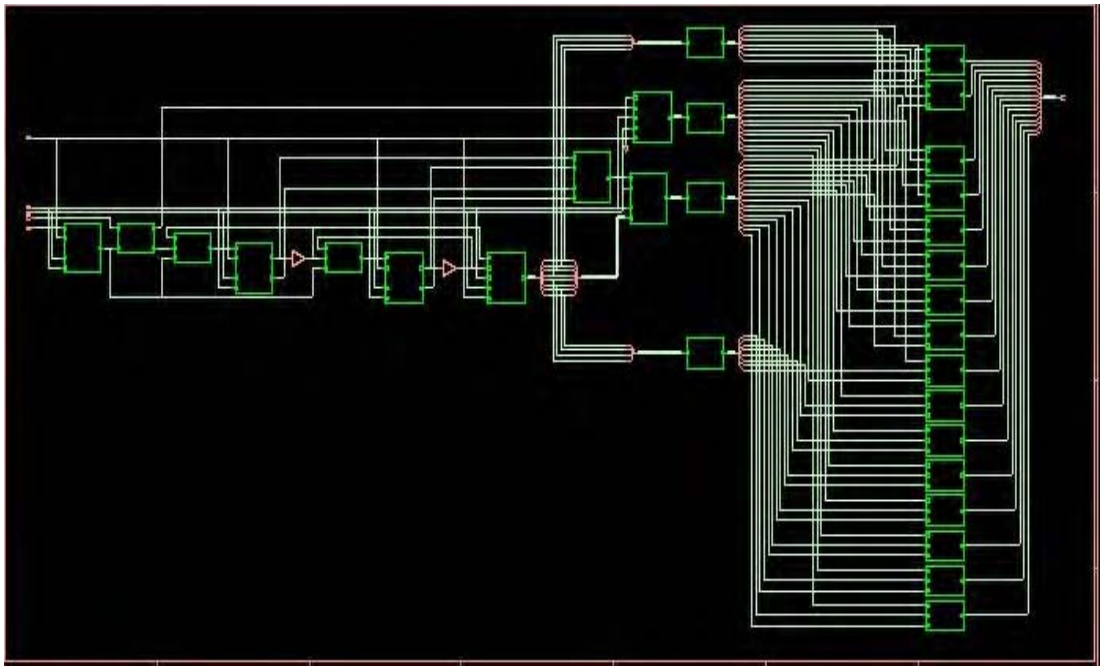

Fig 3: RTL view of proposed method

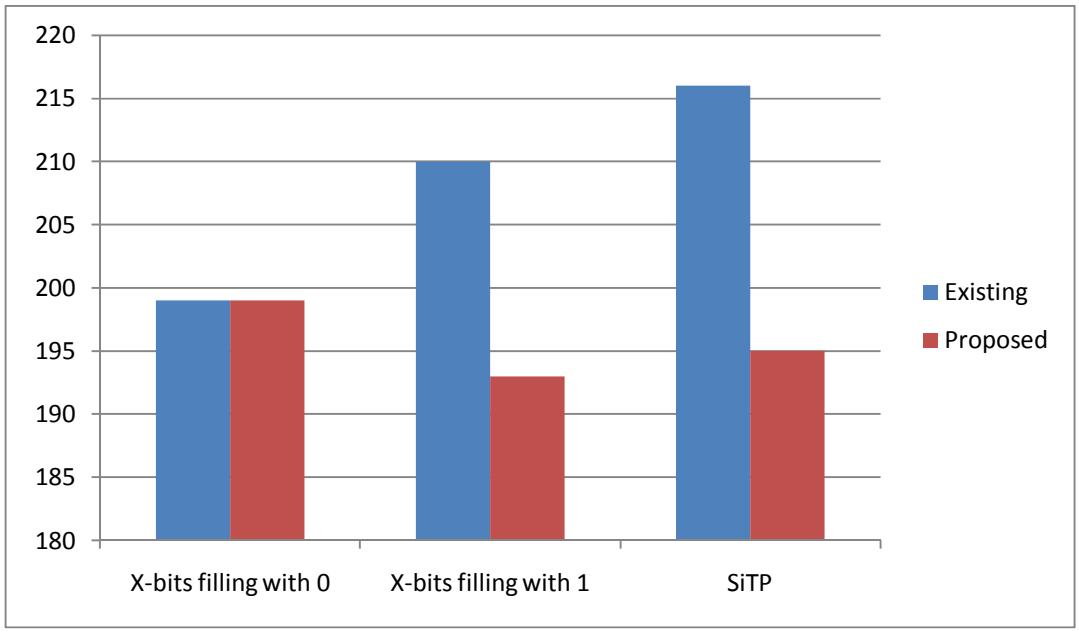

Fig 4: Comparison chart for Existing and Proposed Technique

V. Conclusion

Efficient decompressor architecture has been implemented and design captured using VerilogHDL. Decompressor architecture implemented with X-factor circuitry that helps in the reduction of transition count and improves the fault coverage of circuit under test. Transition in test pattern has been reduced this gives more advantage over power dissipation on shift-in process. Experimental results shown in Table which summarizes the area, power and timing details of Proposed X-factor Decompressor architecture.

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