FPGA IMPLEMENTATION OF HIGH SPEED AND LOW POWER VITERBI ENCODER AND DECODER

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***Abstract*- Implementation of the viterbi decoder in the FPGA plays a dominant role for power and high speed mechanisms. The viterbi decoder is the most efficient decoder. It is commonly used in a wide range of communication and data storage applications. It uses trellis coded modulation (TCM) technique to find the trellis path in the circuit. Here, pre-computation techniques have been adopted for the trellis coded modulation. The main aim of this project is to integrate more number of SOC. The general solution for achieving high speed and low power has been tested with viterbi encoder and decoder and the results are implemented using Xilinx ISim synthesis tool. Implementation results shows that the adapted mechanism plays a dominant role in today's communication system.**

Keywords: Viterbi decoder, viterbi encoder, TCM.

I INTRODUCTION

In many band widths –efficient systems TCM schemes have been utilized. In TCM decoder [1] the VD (viterbi decoder) is the main module in terms of power utilization. The low power methods should be demoralized for the VD in a TCM decoder in order to reduce the computational difficulty as well as power utilization. Trellis code modulation use spread spectrum technique which has wider bandwidth. Trellis code modulation finds the trellis path in the circuit. For example, if we transmit the bits 1001, at the receiver side the output may be in some order (i.e.) 0110. To get the correct output trellis path is used in this technique. By using this technique efficient decoding has been achieved.

The main aim of VLSI is to reduce area, power and to achieve high speed. But in today's real time world when we are reducing the area, the power factor is increasing. Our project aim is to integrate more number of silicon on chip (SOC). In the proposed paper we are implementing viterbi encoder and decoder circuits in field programmable gate array (FPGA). It is a reconfigurable device. Our proposed viterbi decoder occupies less area, since we are going for viterbi encoder the utilization of power is also minimized. By this paper we are achieving the aim of VLSI. Finally the area and power of FPGA based viterbi decoder has been mentioned.

This paper is covered as follows. In segment II discusses viterbi decoder. In segment III, discusses the proposed system i.e., viterbi encoder. Segment IV discusses the results. and Finally, segment V concludes this work.

II VITERBI DECODER

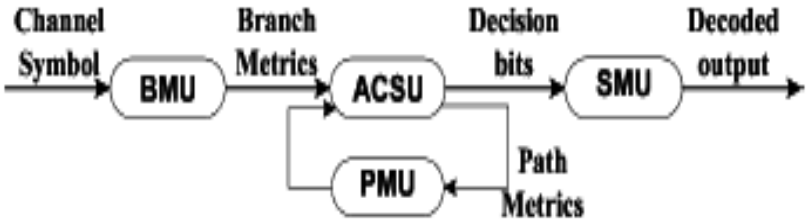

FIG 1: BLOCK DIAGRAM OF VITERBI DECODER

The proposed viterbi decoder design consists of four blocks as shown in figure 1. [1]

- BRANCH METRIC UNIT-BMU
- PATH METRIC UNIT-PMU
- ADD & COMPARE SELECT UNIT-ACSU

- SURVIVOR PATH MEMORY UNIT-SMU [2]

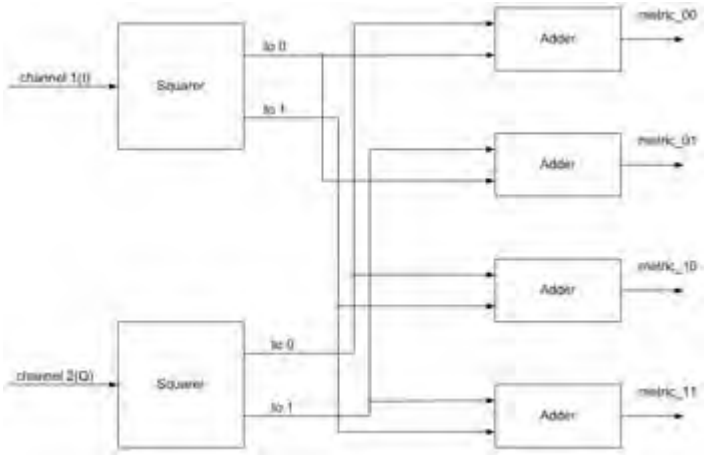

FIG 2: BRANCH METRIC UNIT SAMPLE IMPLEMENTATION

For each transition the above mentioned block computes the branch metric or a hamming distance. Hamming distance is calculated between the expected signal and the received signal. This unit finds the reliable way to encode the data.[3]

PATH METRIC UNIT:

A path metric unit is also called as state metric unit. For each transition in the branch metric unit, it computes the path metric. The major role takes place in add and compare select (ACS) unit is the PMU block. The path metric is calculated by the following formula.

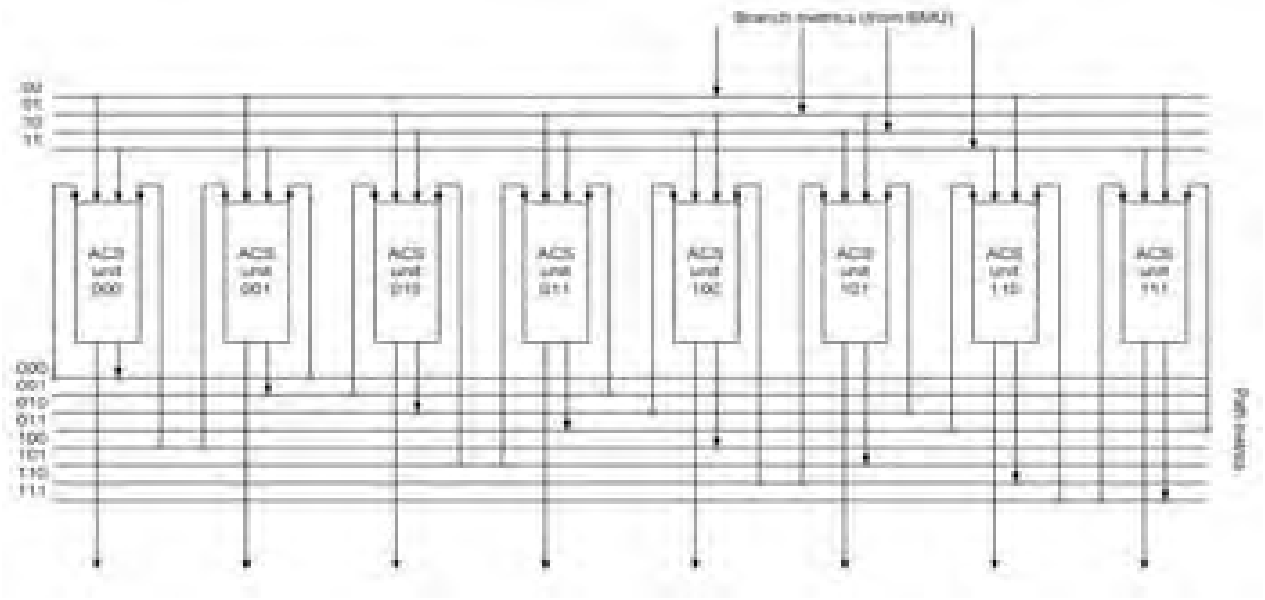

FIG 3: PATH METRIC UNIT IMPLEMENTATION FOR A DECODER

ACS00: $sm1_n = \min (sm1_{n-1} + bm1, sm2_{n-1} + bm4)$ Eq. 1

ACS01: $sm2_n = \min (sm3_{n-1} + bm3, sm4_{n-1} + bm2)$ Eq. 2

ACS10: $sm3_n = \min (sm1_{n-1} + bm4, sm2_{n-1} + bm1)$ Eq. 3

ACS11: $sm4_n = \min (sm3_{n-1} + bm2, sm4_{n-1} + bm3)$ Eq. 4

Where

bm1 = branch metric for state 00

bm2 = branch metric for state 01

bm3 = branch metric for state 10

bm4 = branch metric for state 11

The path metric is calculated by finding the minimum cost of arriving signal into a specific state. A previous time instant of state metric is added with the branch metric and selected the smaller one for each state. In this manner the path metric unit works. Add and compare select unit (ACSU) consists of two storage unit. (i.e.) state metric storage and survivor path storage. The state metric storage stores the partial path metric. The survivor path storage stores the selected path by the add and compare select unit for each state.

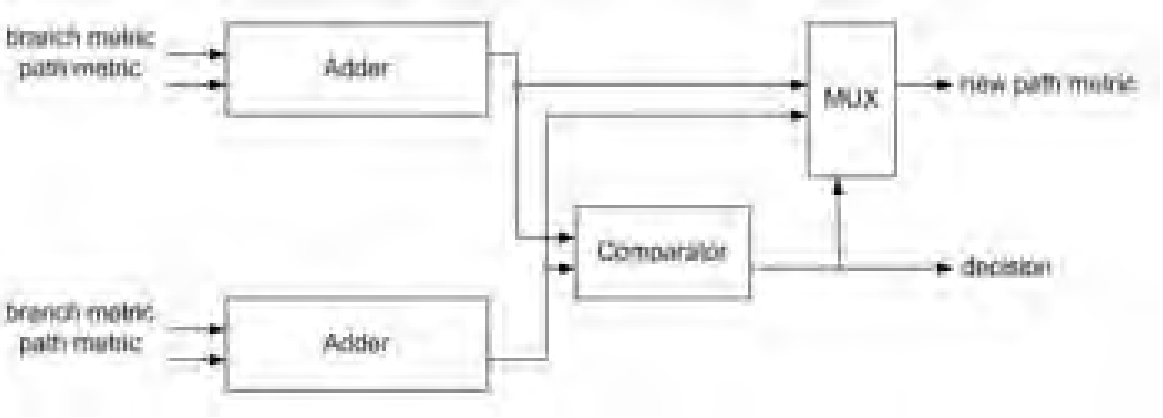

FIG 4: ADD AND COMPARE SELECT UNIT IMPLEMENTATION

III PROPOSED METHOD

VETERBI ENCODER

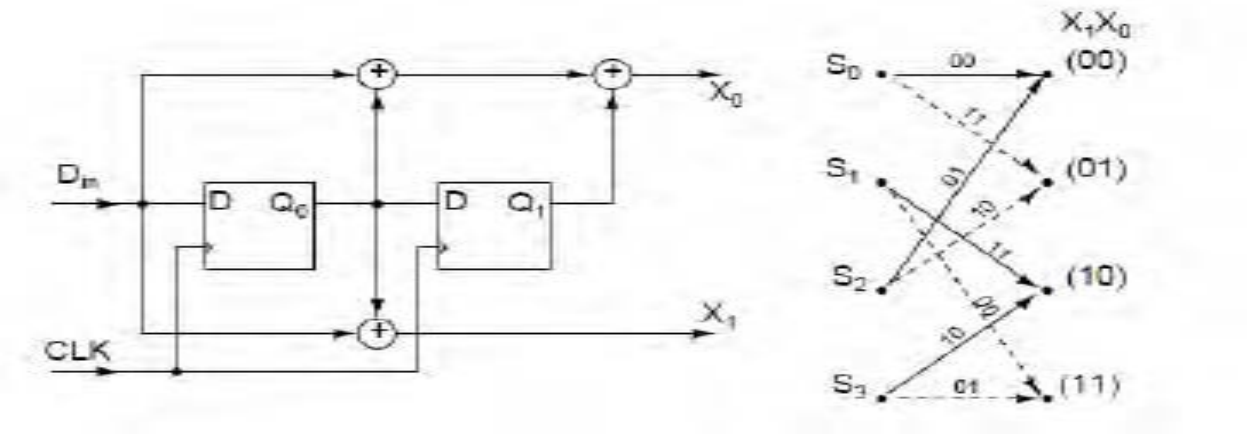

FIG 5: BLOCK DIGRAM OF VETERBI ENCODER

Viterbi Encoders Design with the Parametric path resembles with the Path Length =4. The output obtained from the encoder circuit as shown in above figure 5 i.e., X_1X_0 will act as an input for the decoder circuit which is mentioned in figure 1. Precomputation algorithm has been previously discussed. [4]

IV RESULTS

The below mentioned figure 6 shows better performance analysis compared to previous Theoritical Bit Error Rate. Figure6showstheefficiencyofviterbidecoder.

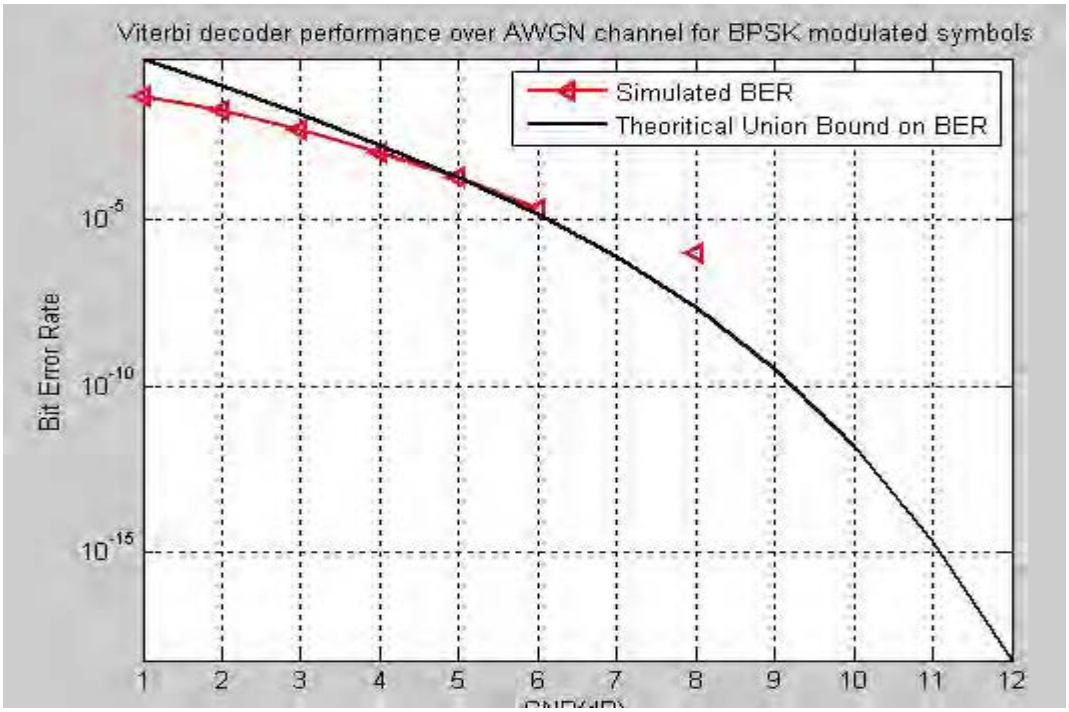

FIG 6: PERFORMANCE ANALYSIS OF VITERBI DECODER

The complete codings are done in verilog and synthesized in XILINX ISIM tool. The RTL view of Viterbi encoder and decoder as shown in figure 7, the technical view and power analysis are shown in figure 8 and 9.

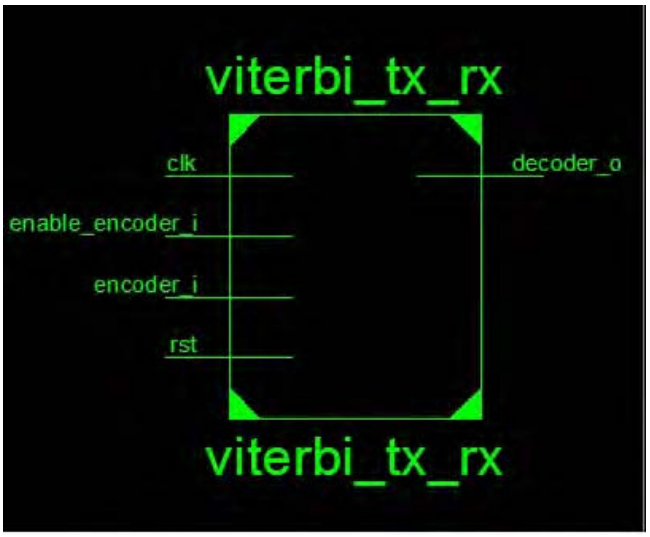

FIG 7: RTL VIEW OF VITERBI ENCODER AND DECODER

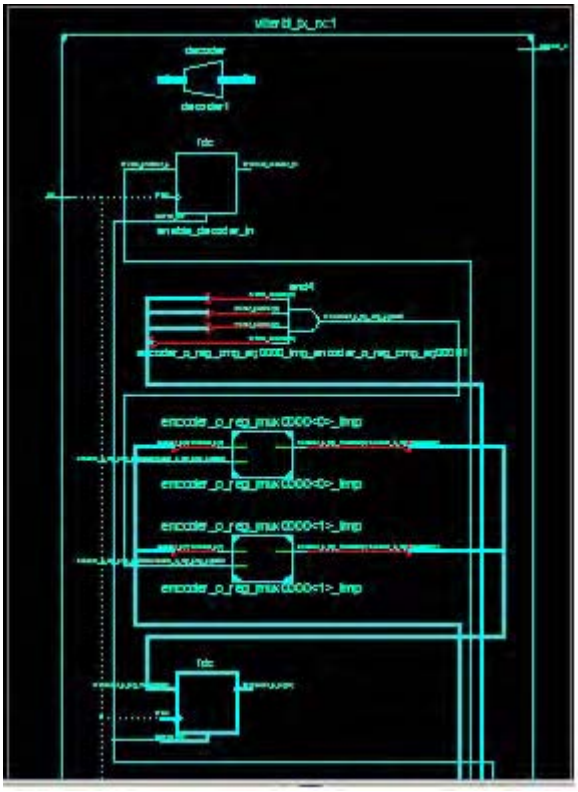

FIG 8: TECHNICAL VIEW OF VITERBI ENCODER AND DECODER

Device	
Family	Virtex5
Part	xc5vlx30
Package	ff324
Grade	Industrial
Process	Typical
Speed Grade	-3

Environment	
Ambient Temp (C)	50.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	250
Heat Sink	Medium Profile
Custom TSA (C/W)	NA
Board Selection	Medium (10"x10")
# of Board Layers	8 to 11
Custom TJB (C/W)	NA
Board Temperature (C)	NA

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.001	1	---	---
Logic	0.000	11	19200	0.1
Signals	0.000	28	---	---
IOs	0.000	4	220	1.8
BRAMs	0.000	1	32	3.1
Leakage	0.379			
Total	0.380			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	2.9	88.9	51.1

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.000	0.282	0.001	0.280
Vccaux	2.500	0.038	0.000	0.038
Vcco25	2.500	0.002	0.000	0.002

	Total	Dynamic	Quiescent
Supply Power (W)	0.380	0.001	0.379

FIG 8: POWER ANALYSIS

V CONCLUSION

In this paper we proposed viterbi encoder design block for TCM systems. The precomputation architecture had been discussed for both encoder and decoder. Since we are going for the viterbi encoder the power consumption is less. T he efficiency analysis of viterbi decoder has been discussed by using matlab tool. The codings done in verilog and synthesized by using XILINX ISIM tool and power analysis are carried out by using POWER ESTIMATORS tool and finally synthesized results are targeted on FPGA devices.

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