IMPLEMENTATION OF MINUTIAE EXTRACTION USING VERILOG HDL

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***Abstract*-Recognition of image signifies the elementary learning of image information. Fingerprint is one of the far most Biometric identification technology used in various application. Designing the hardware for such application is very challenging. This paper focused on designing a modest VLSI architecture for extracting the minutiae components of fingerprint. The architecture is implemented in Verilog and targeted to 0.18 micron Cmos process technology. The design total value is about 1k gate count with the clock speed of 232 MHz. This paper results have shown that efficient hardware architecture.**

Keyword: Fingerprint recognition, Minutiae, Singularities, Bifurcation, Termination

I. INTRODUCTION

Fingerprint Recognition emanated at 18th century, later in the year 1880 Henry Faulds, proposed the first formal research on usage of fingerprint as authentication mechanisms. Archs, Loops, and Whorls are the divisions of fingerprint proposed by Sir Francis Galton. Edward Henry recognized some specific subclasses on Archs and Loops. On the other hand Henry presented the concept of core and delta which are two fingerprint singularities. On the surface of the fingertip, the arrays of ridges are appeared as a fingerprint. Perhaps the biometric characterization is one of the most widespread and unswerving technique which is used for human authentication. Individuality and persistence are the basic properties of the biometric characterization [1]. In fact the fingerprint is distinctive across the individuals and fingers of the identical individuals, while the second property defines, with concern of time the basic characteristics doesn't change. Despite of these motives, fingerprint-based authentication systems have been widely spread in hefty applications [2] where high security levels are needed. Over the world in many law courts as a proof of criminalistics evidences, the fingerprints have been espoused and therefore it is becoming a standard mechanism in forensics. The figure1 and figure 2 shows the basic representation in fingerprint and minutiae.

In two levels of features the fingerprint structure comprises. In global level, the fingerprint features resemble to the arrays of ridges and valleys that appears on the fingerprint. For forming the uniqueness of an

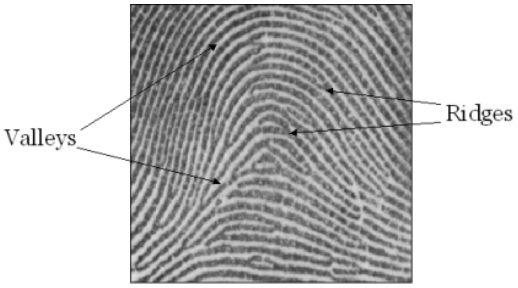

Fig.1 Fingerprint information

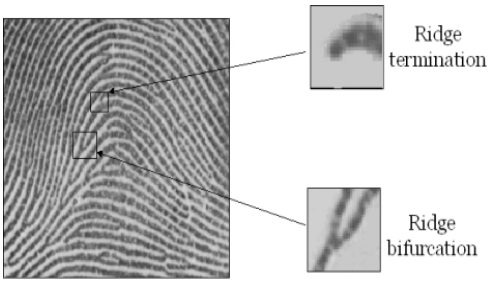

Fig.2 Fingerprint minutiae representation

individual the array of ridges used for fingerprint classification, doesn't have any peculiar property [3]. Those arrays are denominated macro features due to such realities. The dark lines are allied to the ridge patterns, whereas the brighter ones are stated to the valleys in the typical fingerprint image. The fingerprint features are denoted as minutiae at the local level. They resemble to the points where the ridge arrays either terminate tersely (ridge endings) or bifurcate (ridge bifurcations). For establishing the individuality of fingerprints, these features own the property of discriminating.

II. MINUTIAE EXTRACTION

Minutiae is also named as local features of fingerprint, which owns some traditional technique consist of Binarization, thinning and minutiae detection. The conversion of gray scale image into binary image is binarization technique, in which the image intensity can be representing in two values i.e. white and black. White denotes the valleys and background, while black denotes the ridges. A global threshold value is a modest

method. If x,y presently processing with pixel location then P(x,y)=0 if x,y belongs to ridges else if P(x,y)=1 where x,y belongs to valley or background. Next we move on to Thinning technique, in which the main objective is to find the ridges of pixel width. The processes will continue its performance in performing successive erosions until a set of connected lines of unit-width is reached. This line also referred as skeleton. A vital property of thinning is behind in the preservation of the connectivity and topology; however it can leads to generation of small bifurcation artifacts and subsequently to detection of false minutiae. Some procedure which aims the elimination of these artifacts must be performed after the completion of thinning technique. Minutiae detection- The minutiae is detected by using 3x3 pattern masks which is obtained from the binary thinned image. To identify the ridge ending and bifurcation points, Samples of masks are utilized and shown in below figure. Even though the process appears to be modest, it is necessary to consider the riddance of false detected minutiae. After successful extraction of minutiae, they are stored in a template, which may contain the minutiae position (x, y), minutiae direction (angle), minutiae type (bifurcation or termination), and in some case the minutiae quality may be considered. The fingerprint possess the discriminatory information, designing a reliable automatic fingerprint matching hardware is very challenging here the initiative taken [4].

III. PROPOSED ARCHITECTURE

The proposed architecture contains the line memory buffer to load the input pixels. Fig.4 shows the block diagram of architecture for fingerprint minutiae extraction. It consists of 4 blocks along with line memory buffer, I-M, BT-process, BT-memory, and BT-Database. The BT-process block performs combined function of binarization and thinning; both are performed on the basis of thresholding concept. The threshold value is variable it may varies from one fingerprint to another fingerprint. If the fingerprint affected by any noise or disturbance over the image then the minutiae extraction become difficult the result may not guarantee [5].

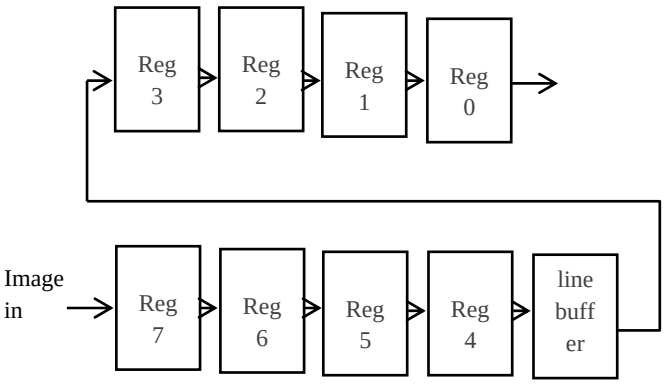

Fig.3 Register bank with line buffer

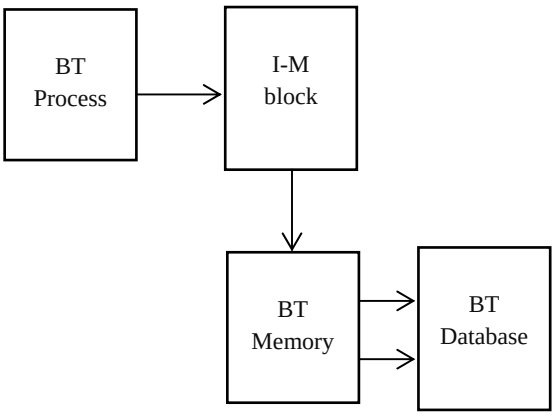

Fig.4 Block diagram of Minutiae Extraction architecture

I-M block denotes Intermediate Memory, which is intermediate memory to hold the digitized pixel value for minutiae extraction process. The threshold values can be fixed based on the image quality and noise ratio. The finger impressions with poor quality or presence of noise make the process difficult. The minutiae extraction process can be done by BT-memory block which contains the pseudo-mask for both bifurcation and termination.

IV. IMPLEMENTATION AND RESULT

The proposed design captured using VerilogHDL. RTL has been verified through functional simulation. The gate level netlist were obtained through RTL Compiler by targeting the design 0.18um Cmos technology process. The pseudo mask generator is designed by optimized logic which generates 12 different masks to detect the minutiae extraction as bifurcation and termination. Some control enable signal was used to reduce the power dissipation by removing clock for unused block which shown in Figure 6.

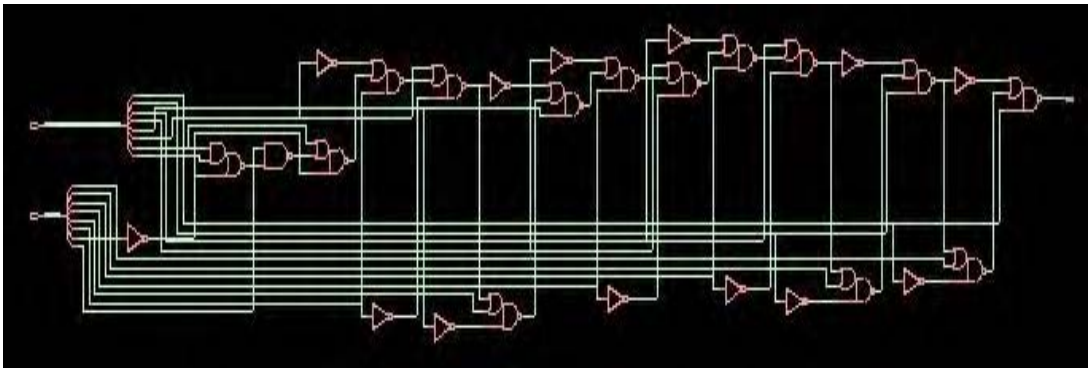

Fig 5 Schematic view of Pseudo mask generator

Table 1 summarizes the Implementation result

Platform	Technology Targeted	Gate Count	Speed
ASIC	0.25 um	1k	232 MHz

Table 1 shows the result of proposed design after performing the synthesize process. The most area of the design occupied by the block IM, which shown in Figure 7. The proposed architecture for Minutiae extraction can be adapted to several systems such as Finding Individuality, Authentication, and Identification of Overlap finger impression and their feature extraction.

V. CONCLUSION

The Fingerprint recognition is one of the most important authentications for proving an individuality of any person. For good quality impression it matches 100% with reference. This paper discussed about hardware design of such imperative process. Fingerprint devices are intuitive and needs to compact to fix anyplace. The proposed design is very effective and simple in structure and can adapt with SoC for fingerprint authentication device. The result was analyzed in terms of both area and delays which summarized in Table1.

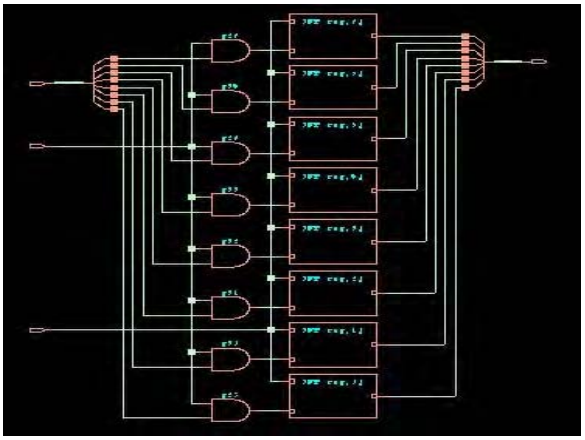

Fig 6 Design with control signal

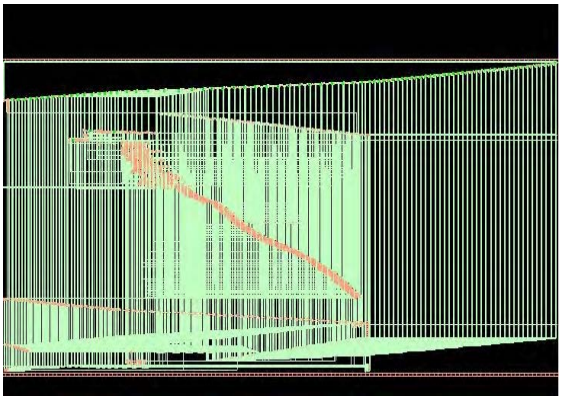

Fig 7 schematic view Minutiae extraction

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